ePIC SVT Disk FPC

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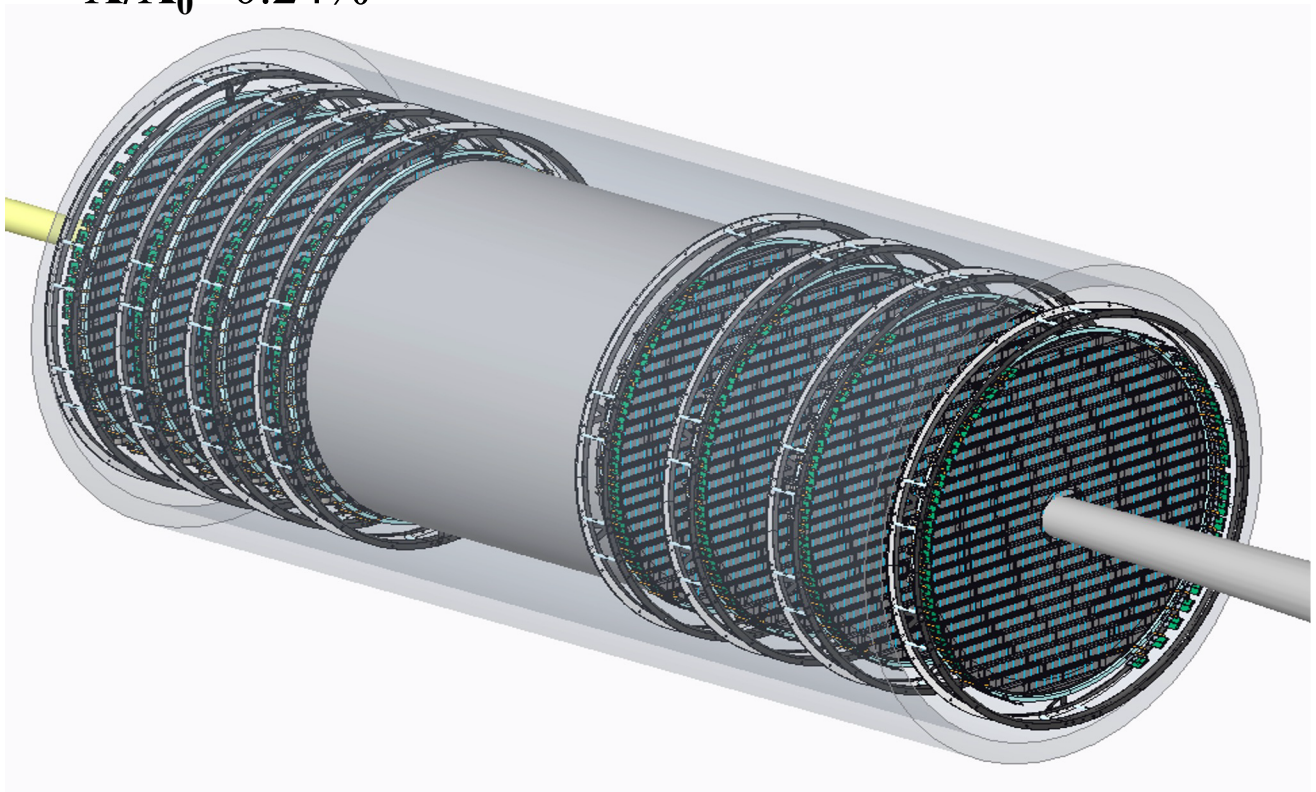
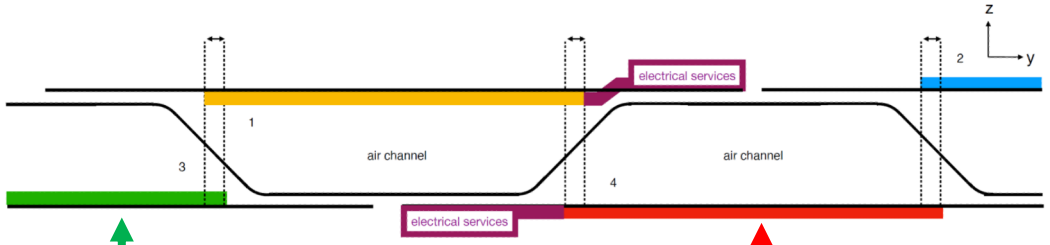
ePIC SVT Disks

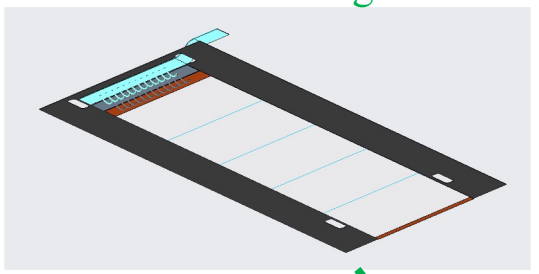
- **EIC Large-Area Sensor** with design based on ITS3 MOSAIX, mounted on low-mass CF support structure with integrated air cooling
- **AncASIC** provide negative sensor bias voltage, serial power and slow control
- **Outer radius** ranging from 24 to 40 cm
- **X/X_0** ~0.24%

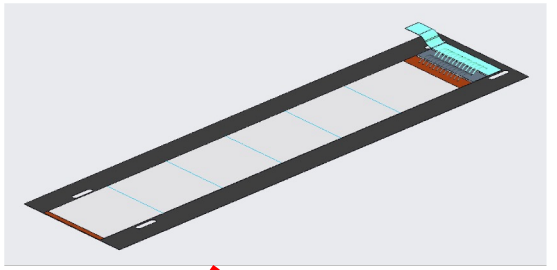


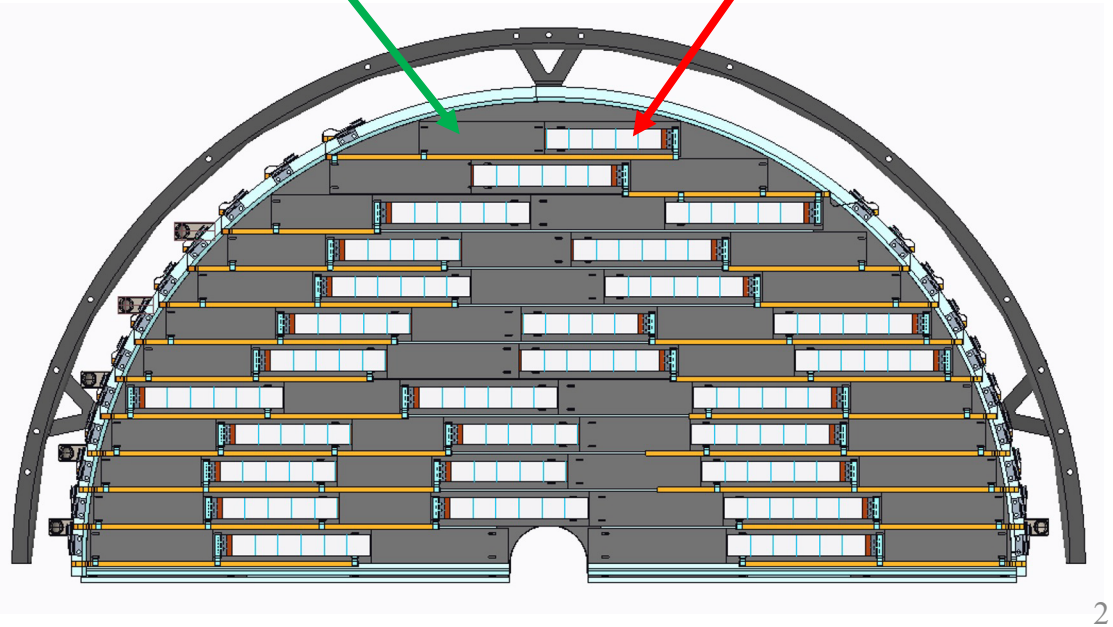


Sensor Inward Facing Module

Sensor Outward Facing Module



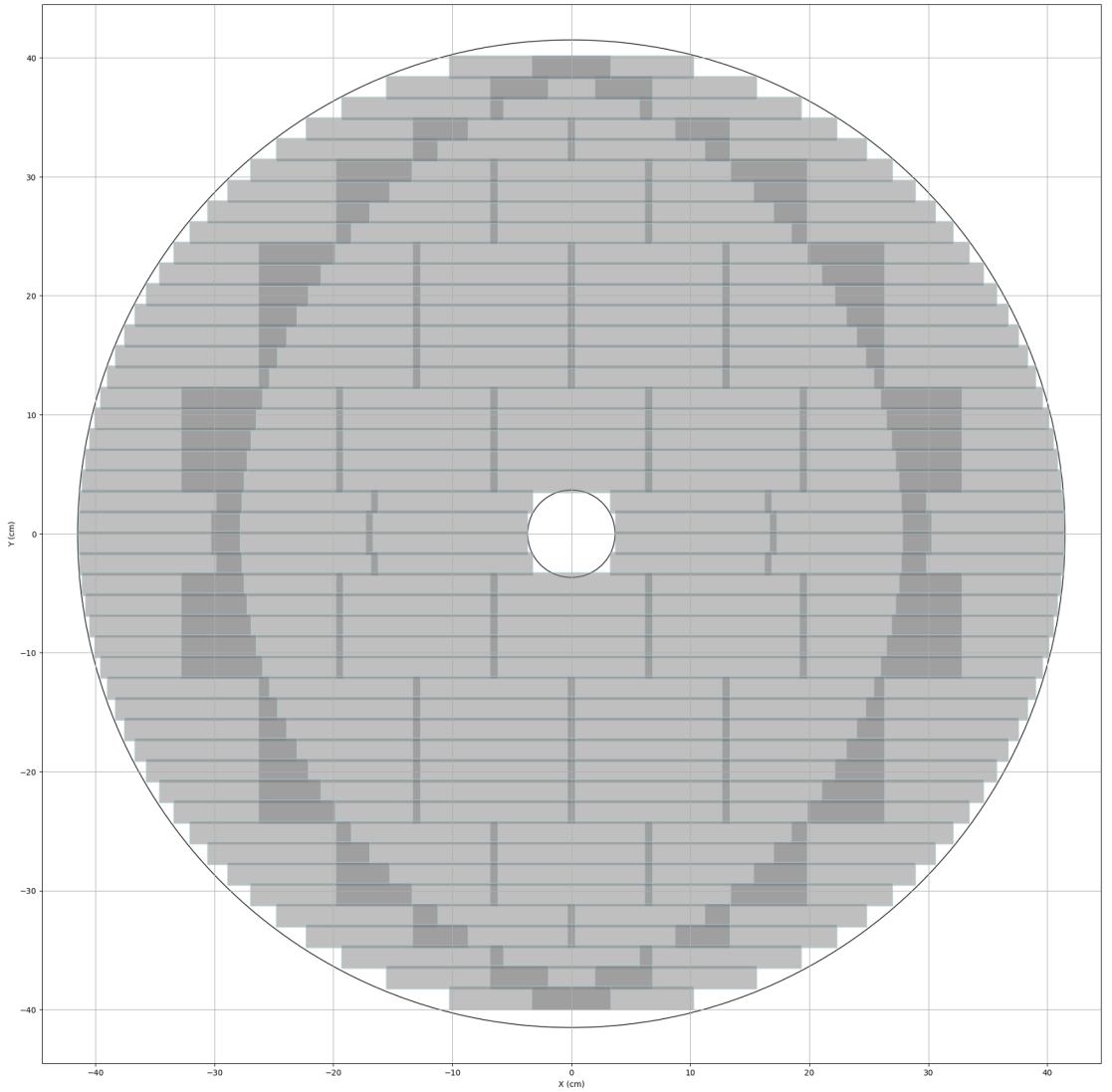




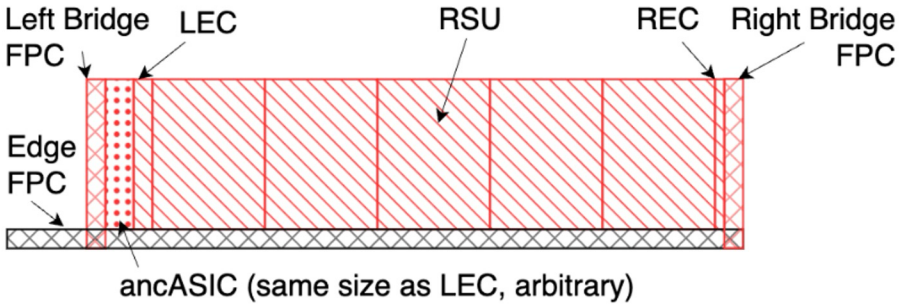
ePIC SVT Disks

Sensor placement strategy for disks: minimum overlap in the inner region, maximum in the outer region; symmetric in x if possible; LEC at larger radius than REC.

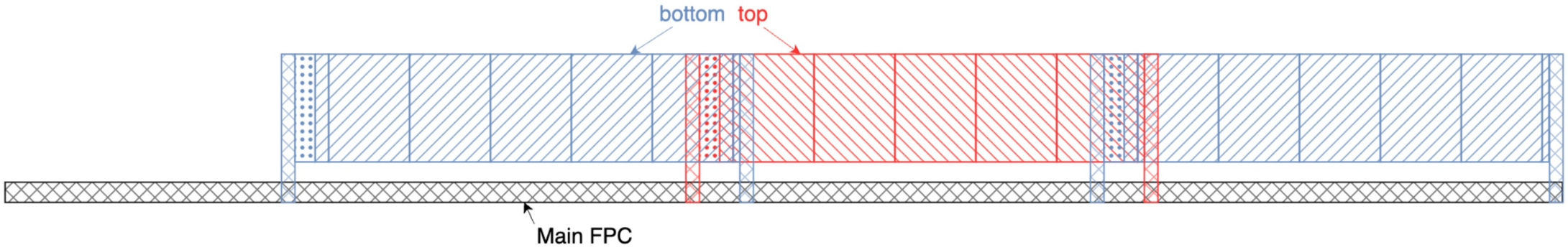
- For rows covered by the beam pipe, start filling the first sensor at $x=\sqrt{R_{in}^2-y^2}$, so that the edge of the sensor is the closest possible to the beam pipe.
- Place the other sensors with an overlap of 6 mm to the previous one to avoid gaps covered by active sensor areas.
- Stop when the last sensor would be outside of the disk. Place the last sensor at $x=\sqrt{[R_{out}^2-(y+\text{sensor height})^2]}$-sensor length, so that the edge of the sensor is at the outer radius of the disk.
- The sensors at the edge of the disks will connect via an edge FPC to the corresponding FPC interface board (FIB). The other sensors will connect via bridge and main FPCs to the FIB (see page 10&11).
- The length of the main FPC may need to vary depending on y.

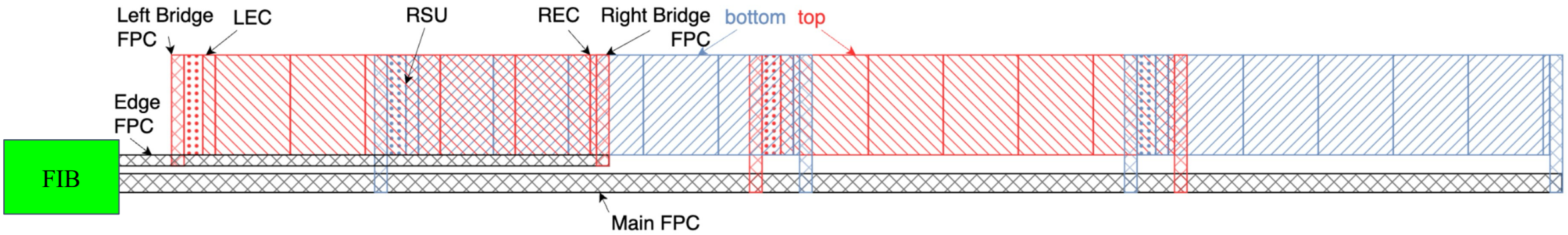


EIC-LAS Assembly for SVT Disks

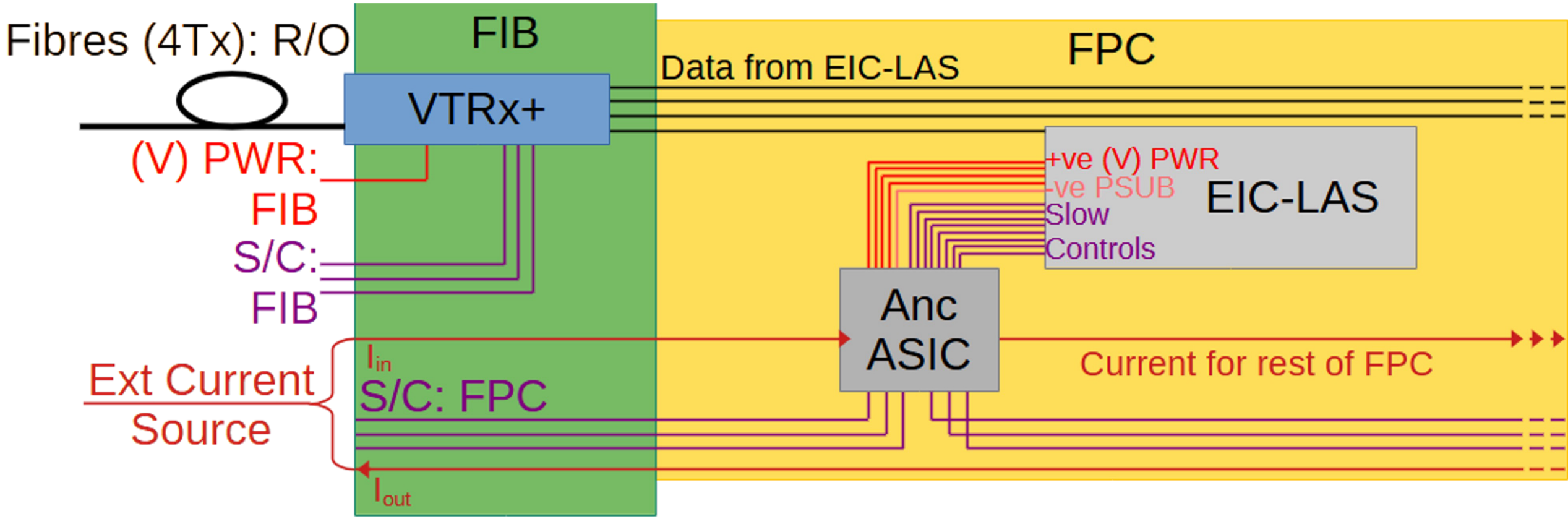


Left bridge FPC will connect to ancASIC and EIC-LAS LEC, while Right bridge FPC will connect to EIC-LAS REC. Both left/right bridge FPCs (could be one piece) will connect to a main or edge FPC, which will connect to FIB to make an assembly with upto four EIC-LAS + AncASIC.





SVT Disks with EIC-LAS+AncASIC



AncASIC on bridge FPC

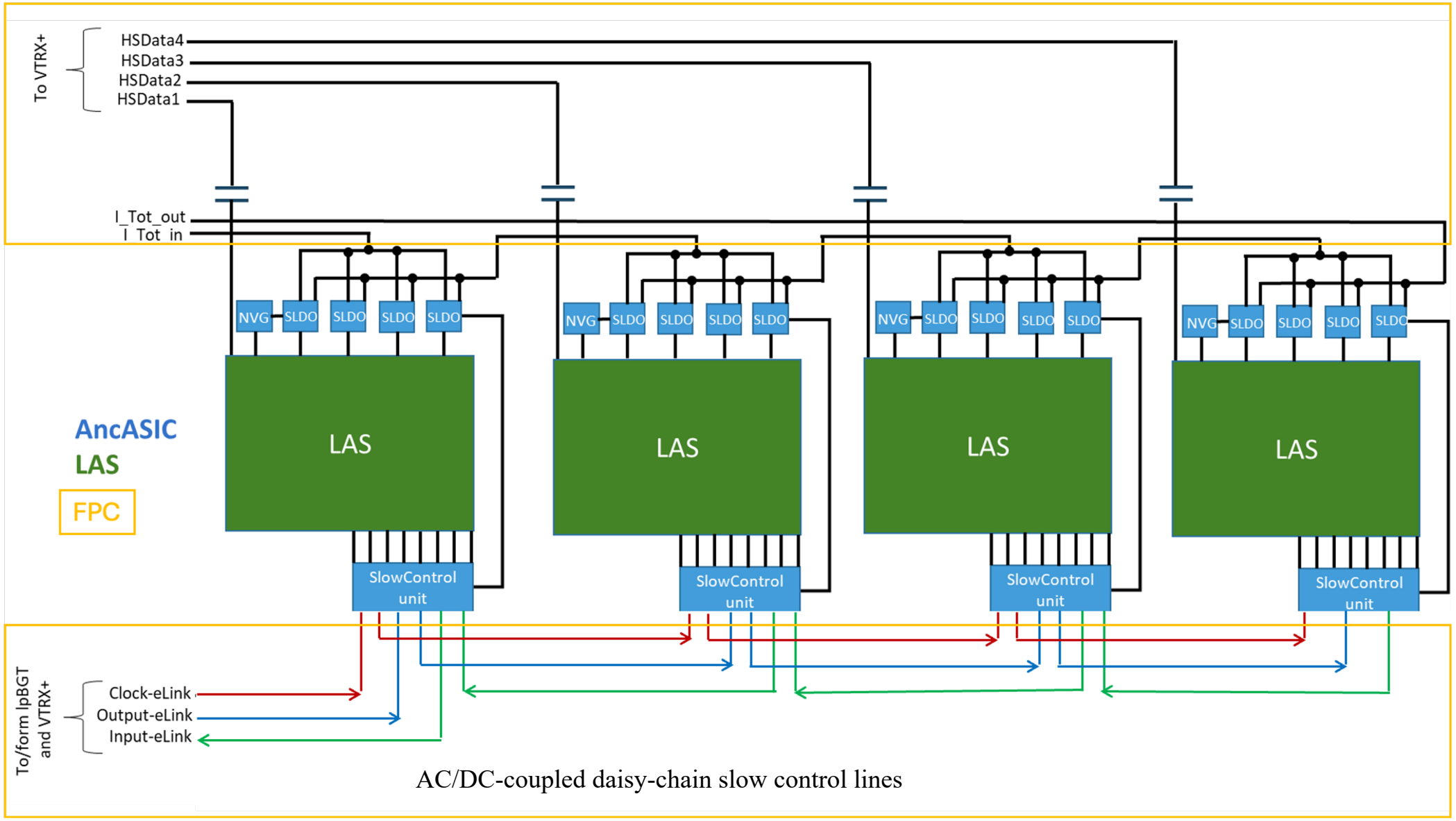
Signal	Rate	Comment	Type	Main FPC	Edge FPC	Bridge FPC
Serial Power Current	N/A	DC power current from FIB to AncASIC	DC	Y	Y	Y
SC_clk	40/160/320 MHz	Clock from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_in	40/160/320 Mbps	SC signals from lpGBT on FIB to AncASIC	AC/DC	Y	Y	Y
SC_out	40/160/320 Mbps	SC signals from AncASIC to lpGBT on FIB	AC/DC	Y	Y	Y
HS data	5.12/10.24 Gbps	HS data from EIC-LAS to VTRX+ on FIB	AC	Y	Y	Y
GCLK	160/320 MHz	Global clock from AncASIC to EIC-LAS	AC/DC	N	N	Y
SYNC GRSTB	N/A	SYNC/RESET from AncASIC to EIC-LAS	AC/DC	N	N	Y
SRVWR/RD SCWR/RD	5-10 Mbps	SC signals from AncASIC to EIC-LAS	AC/DC	N	N	Y
LV for EIC-LAS	N/A	LV from AncASIC to EIC-LAS	DC	N	N	Y

Interconnects with AncASIC on bridge FPC

	FIB	Main/Edge FPC	Bridge FPC	AncASIC	EIC-LAS
FIB					
Main/Edge FPC	**Connector**, Soldering				
Bridge FPC	N/A	**soldering**, wire/TAB-bonding			
AncASIC	N/A	N/A	**wire-bonding**		
EIC-LAS	N/A	N/A	**wire-bonding**	N/A	

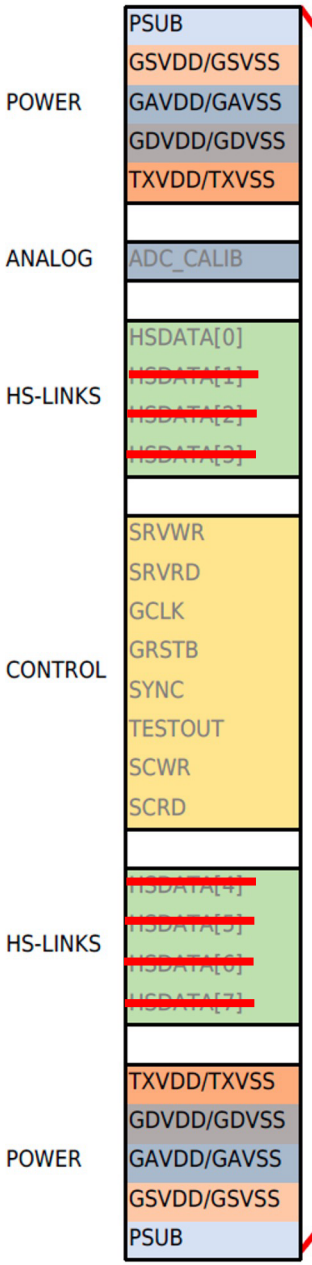
bold: preferred option

SVT Disks with EIC-LAS+AncASIC



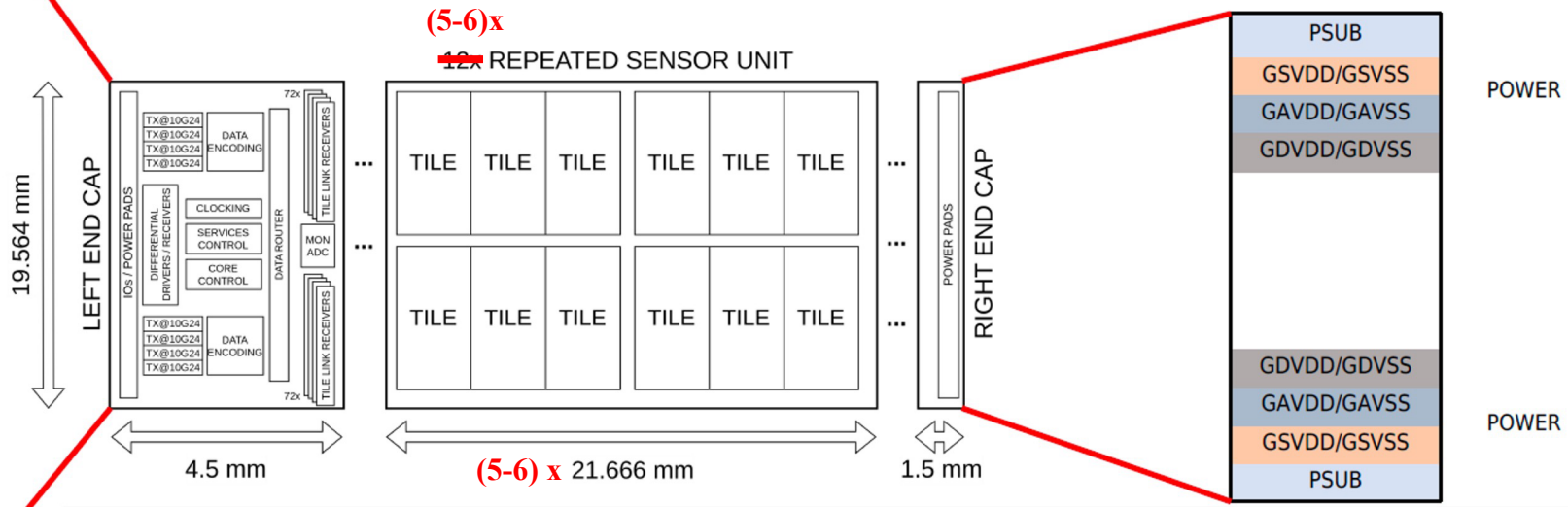
AC/DC-coupled daisy-chain slow control lines

EIC-LAS



Supply	Typical (mA)	Max (mA)
PSUB (-1.2V)		
GSVDD/GSVSS (1.2V/0V)	40	60
GAVDD/GSVSS (1.2V/0V)	170	270
GDVDD/GDVSS (1.2V/0V)	526	816
TXVDD/TXSVSS (1.8V/0V)	200	300

Signal	Frequency
GCLK	40/160/320 MHz
SYNC	N/A
GRSTB	N/A
SRVWR/RD	5-10 Mbps
SCWR/RD	5-10 Mbps
HSDATA0	5.12/10.24 Gbps

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GSVDD/GSVSS  : Global Services domain (1.2V/0V), always-on, used for on-chip services
GAVDD/GAVSS  : Global Analog domain (1.2V/0V)
GDVDD/GDVSS  : Global Digital domain (1.2V/0V)
TXVDD/TXVSS  : Serializer domain (1.8V/0V), only used for serializers
PSUB         : Substrate bias (-1.2V .. 0V), used for substrate biasing
Control pads : Powered by the services domain
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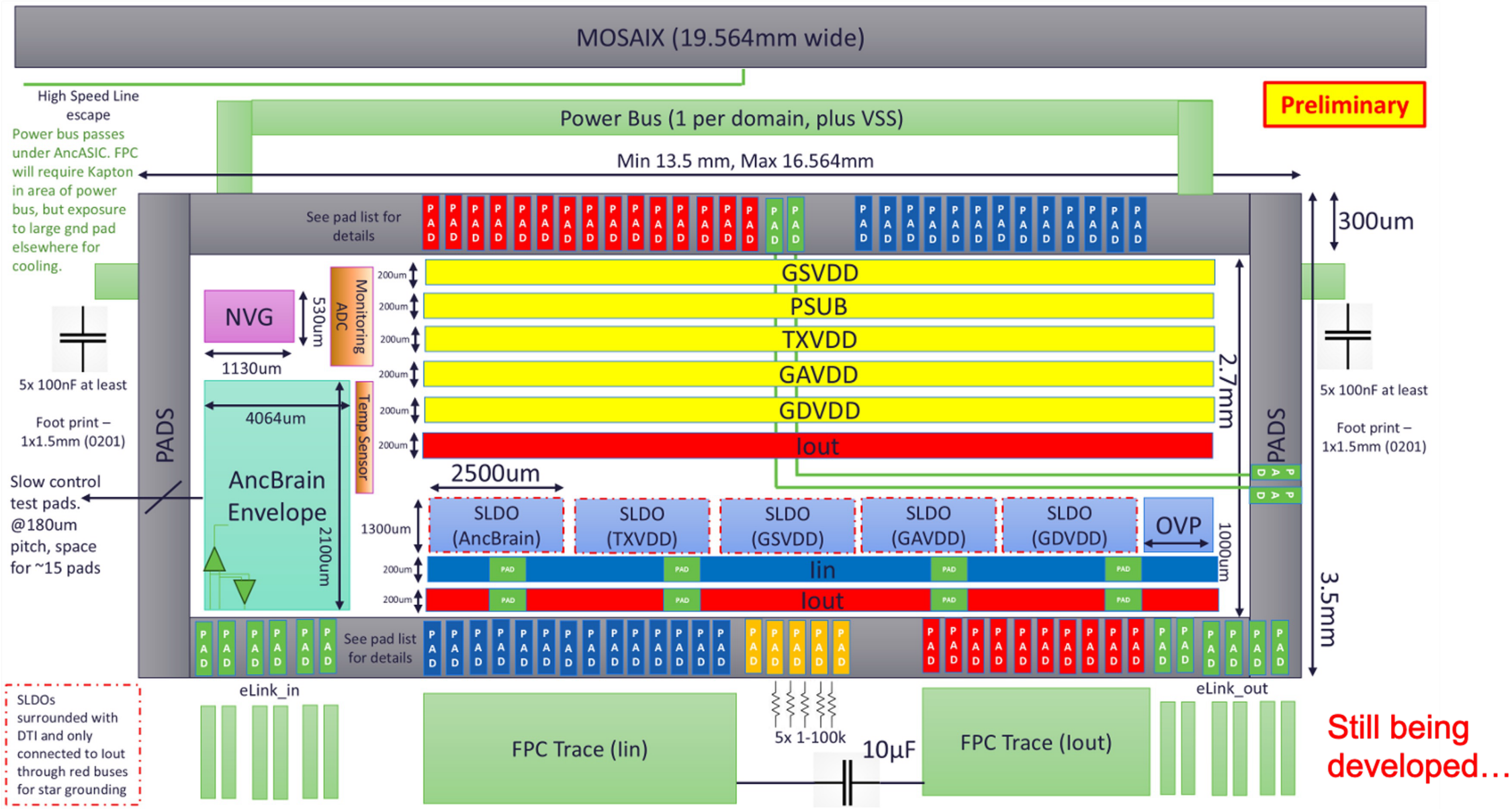
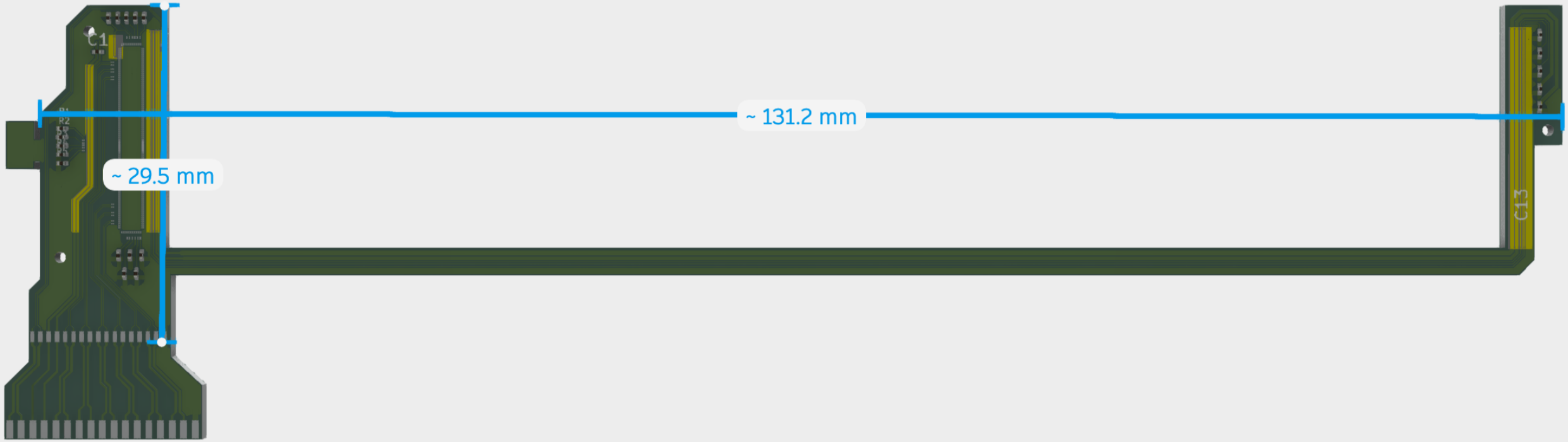
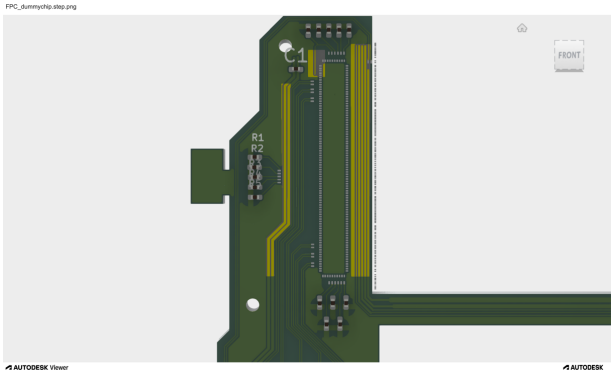
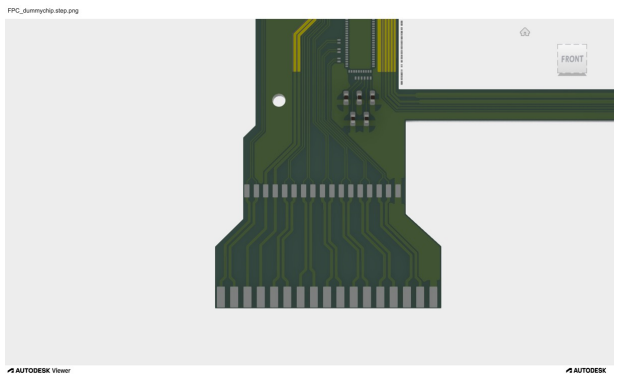
AncASIC

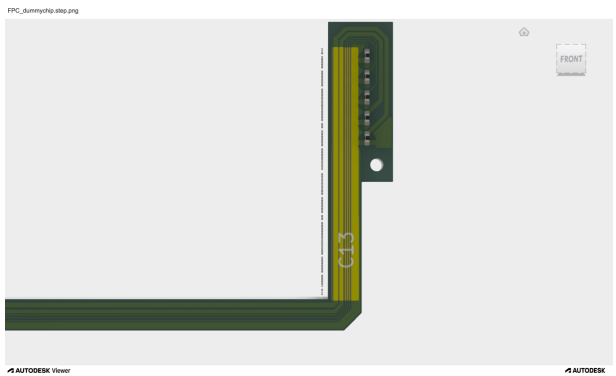

MOSAIX (19.564mm wide)
High Speed Line escape
Power bus passes under AncASIC. FPC will require Kapton in area of power bus, but exposure to large gnd pad elsewhere for cooling.
Power Bus (1 per domain, plus VSS)
Min 13.5 mm, Max 16.564mm
Preliminary
See pad list for details
PADS
300um
5x 100nF at least
Foot print – 1x1.5mm (0201)
NVG
530um
Monitoring ADC
1130um
200um
GSVDD
PSUB
TXVDD
GAVDD
GDVDD
Iout
2.7mm
4064um
Temp Sensor
AncBrain Envelope
2100um
Slow control test pads. @180um pitch, space for ~15 pads
2500um
SLDO (AncBrain)
SLDO (TXVDD)
SLDO (GSVDD)
SLDO (GAVDD)
SLDO (GDVDD)
OVP
1300um
1000um
Iin
Iout
3.5mm
SLDOs surrounded with DTI and only connected to Iout through red buses for star grounding
eLink_in
FPC Trace (Iin)
5x 1-100k
10µF
FPC Trace (Iout)
eLink_out
Still being developed…

Disk FPC Prototype Design (WIP)



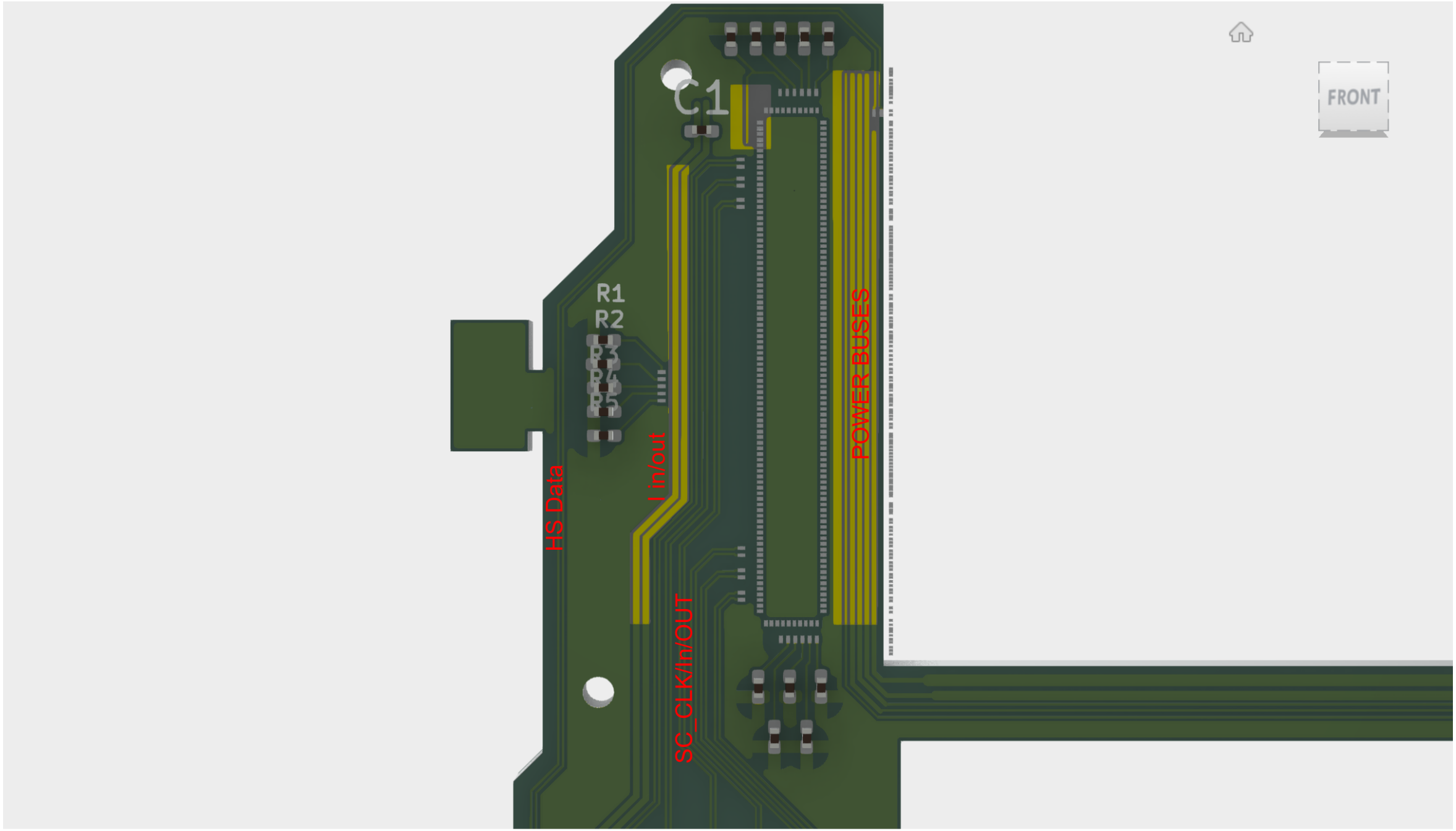






Pros:
Cons:

FPC_dummychip.step.png



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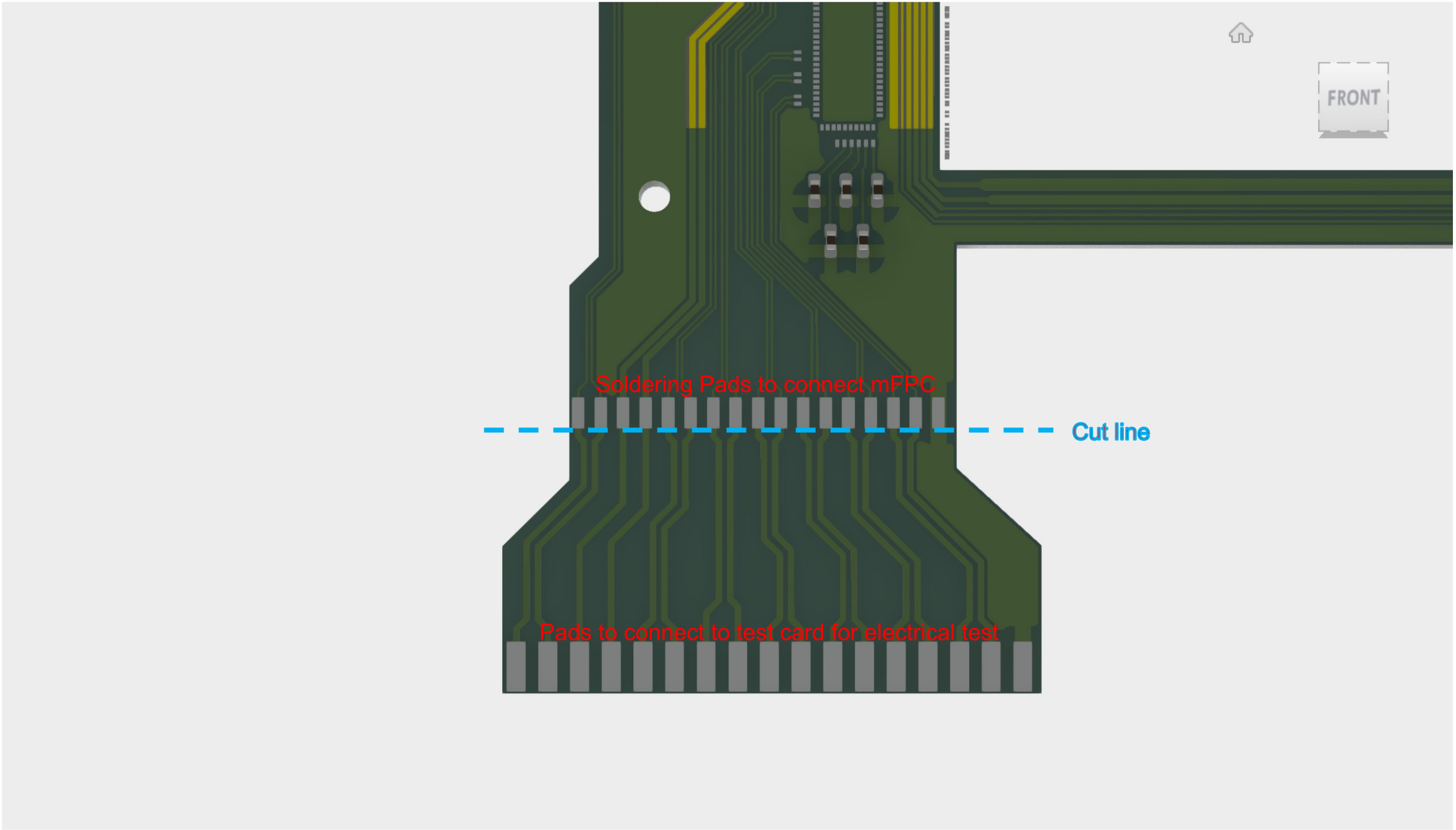
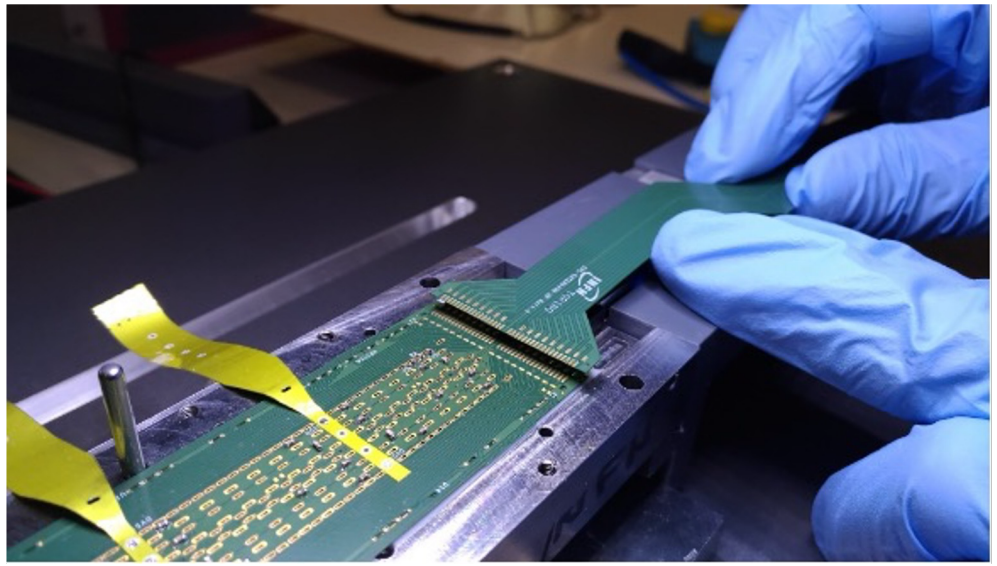
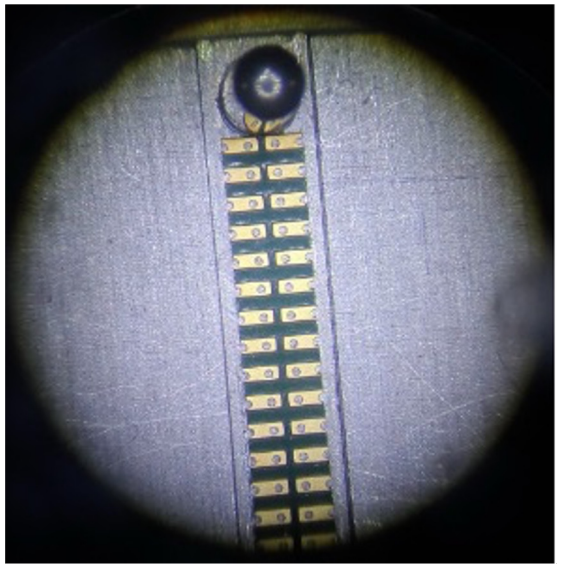
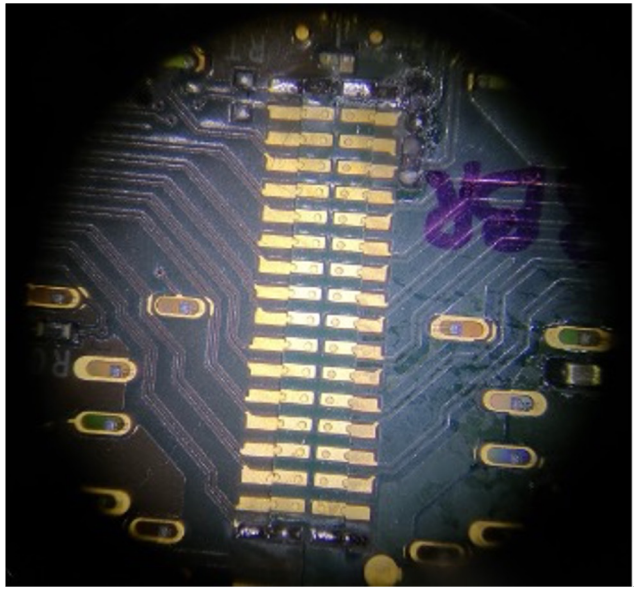
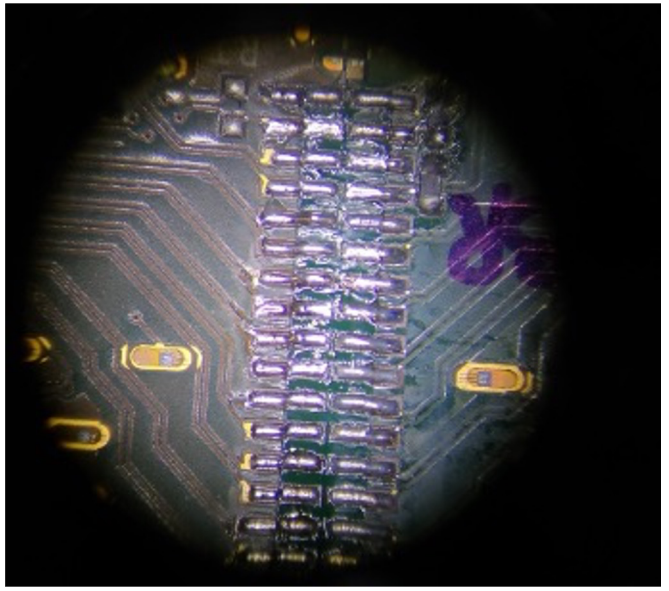


ALICE ITS2 FPC-to-FPC Soldering









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