



FCFD status

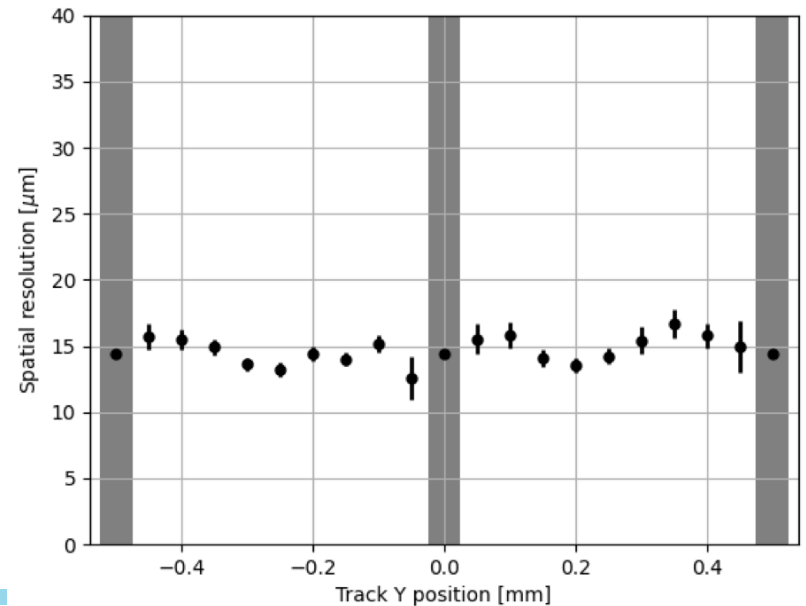
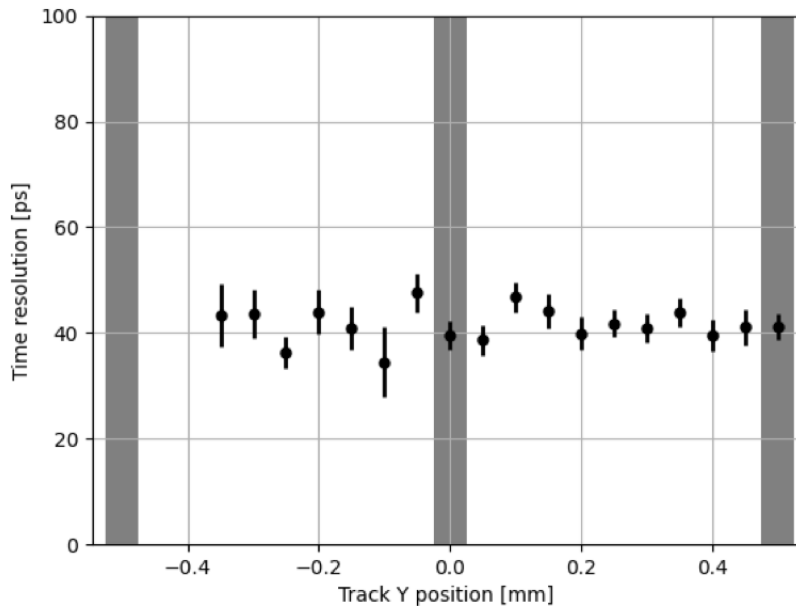
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EPIC Electronics & DAQ WG meeting : eRD109 Monthly Progress Reports

Jan 8, 2026

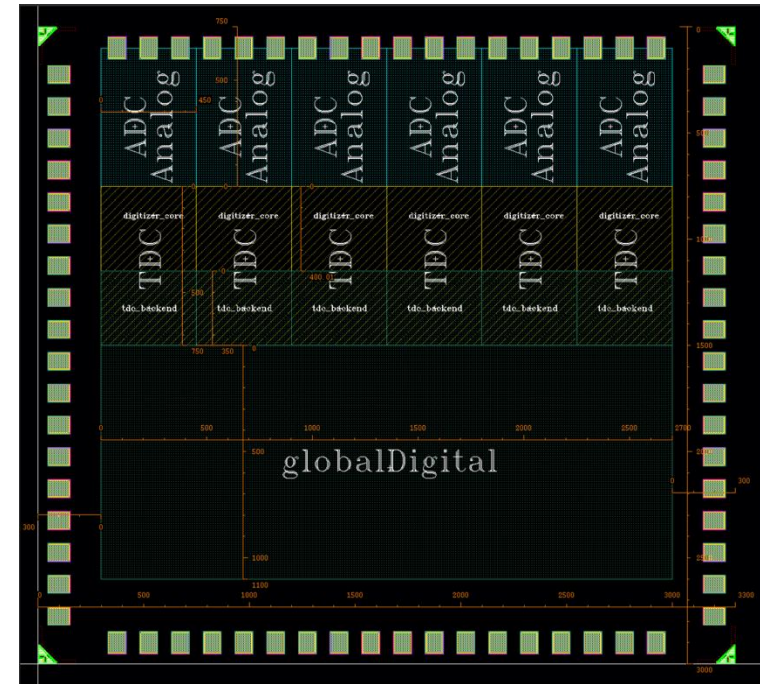
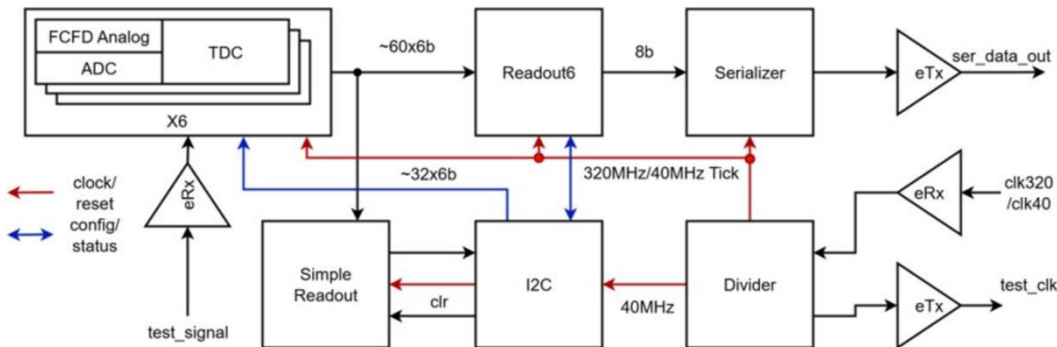
FCFDv1.1

- Summary of results submitted to NIM A: arXiv:2512.19930
 - Measurements of performance in DESY and CERN test beam
 - Measured **time resolution** ~ 40 ps across sensor surface
 - Measured **spatial resolution** ~ 15 - 20 μm
 - Fully efficient across the sensor surface



Design status for FCFD1.2

- FCFD1.2 will implement TDC, ADC, I2C, and simplified readout on a 6-channel chip
- The whole team worked very hard through the holidays
 - All FCFDv1.2 RTL is completed now!
 - RTL is frozen now



Current floorplan and pads

Design status for FCFD1.2

- The Divider module generates the chip-level 40 MHz clocking signals, `clk40` and `tick40_ce`, from the input 320 MHz reference clock.
 - Produces the bunch-crossing counter used by the readout logic.
- The Time-to-Digital Converter (TDC) measures the timing of hits
 - Produces a packed 64-bit output word for downstream readout
 - The design operates with a 320 MHz clock
- The Analog-to-Digital (ADC) measures amplitude: encoded in 5-bits, bin sizes 1.5fC/bin in the low part, going to 3fC/bin at the high end
- The Readout6 (fast readout) module collects TDC hit data, packages them into framed words, and transmits the resulting stream over a serial output link at 320 Mbps
 - Simple Readout performs readout over I2C, and allows triggered readout for initial verification and commissioning

Summary

- Testing of the FCFD1.1 was very successful
 - More testing is being performed now with IR laser in the lab
 - 12 chips were sent to JLab for testing with MCP-PMTs for applications for pfRICH and hpDIRC
- Requested tapeout on mini@six with IMEC in April, dry run in March
 - All effort now is focused on the finalization of the analog integration, pads, PNR, RTL and netlist verification