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# Status report of the eRD109 project on SALSA chip development

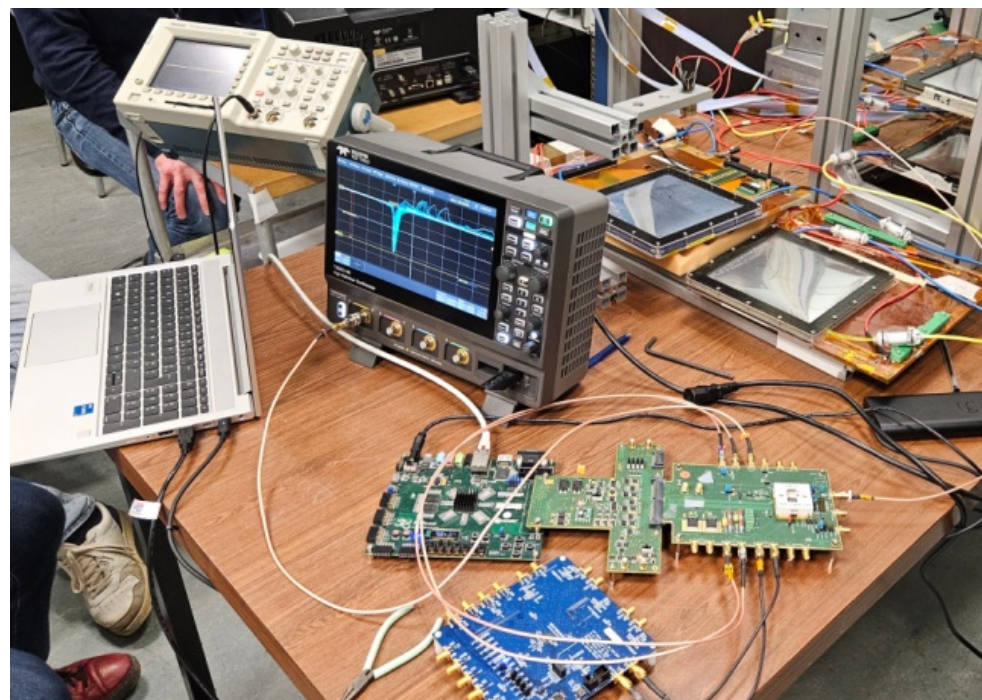
Damien Neyret (CEA Saclay IRFU) for Sao Paulo  
University and CEA IRFU teams  
EPIC DAQ/electronics WG meeting  
8/1/2026

## ■ PRISMEv1 prototype (PLL test chip)

- Used to do tests of high-speed links and CDR decoding (implemented in PLL)
- Radiation tests foreseen in March

## ■ SALSA1 prototype

- Tests ongoing on SALSA1 connected to real MPGDs
- 1 MM strip connected to 1 channel
- Tests with  $^{55}\text{Fe}$  source and cosmics, also some sparks
- Good behavior, with some overshoots with large amplitude signals, to be investigated. More results next time
- Radiation tests foreseen in February



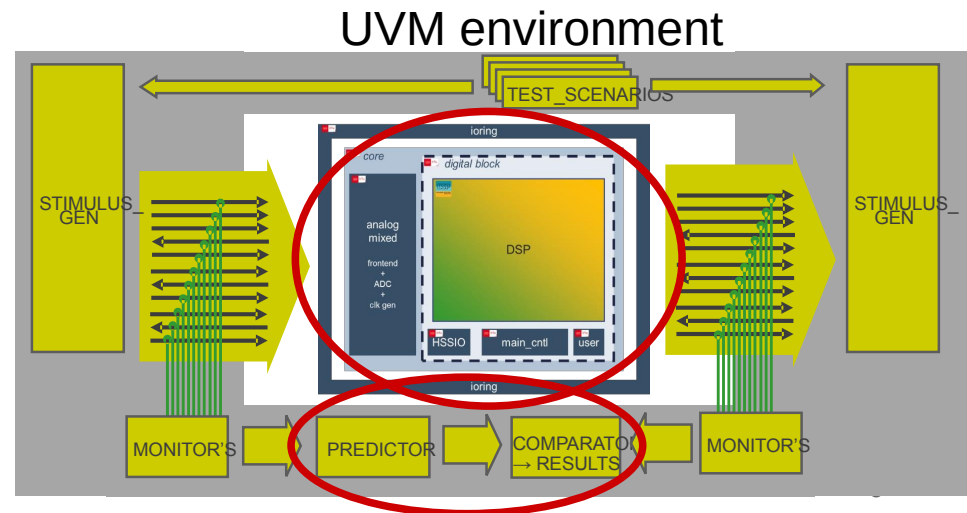


## SALSA2 development status

- DSP verification ongoing, presently based on triangular signals
- Integration in rest of digital environment ongoing
- Study ongoing on precise behaviors of fast synchronous commands. Goal is to be sure that they are managed as expected
- Input link synchronization state machine (trad. link) done and tested on FPGA (cf next slides)
- Some difficulties with clock generator, improved architecture developed, to be validated. Allows to have sampling rates between 1 to 50 MS/s
- Floor plan: integration of analog part ongoing; estimation of size of digital part ongoing, no clear idea of its final size yet. Power consumption could be also larger than expected, to be confirmed
- UVM environment: work ongoing on integration of DSP; integration of test features directly in the code generation

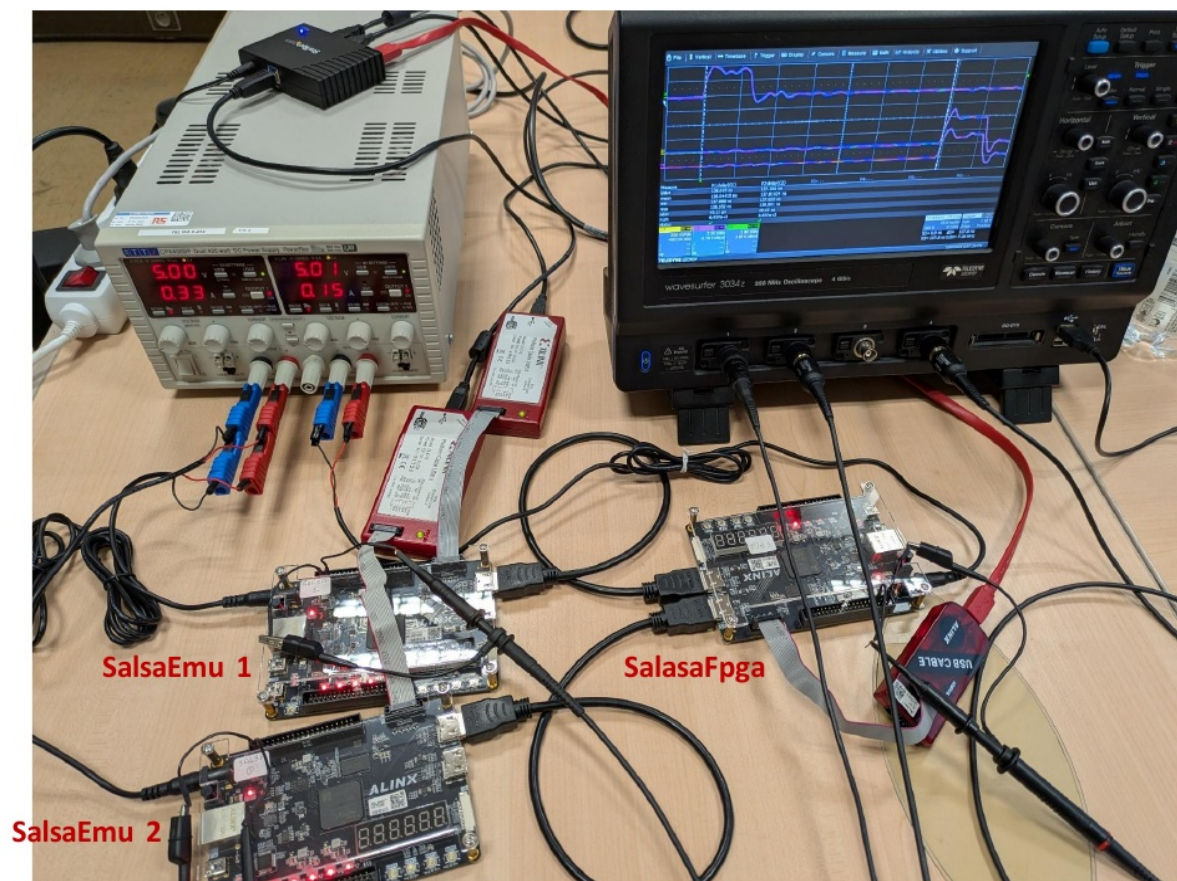
## Timeline

- Still a lot of works ahead:
  - code validation ongoing
  - integration of all modules, validation
  - digital layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen 1<sup>st</sup> semester 2026
- Tests from end of 2026
- Distribution to users in 2027



## Prototyping and validation on FPGAs

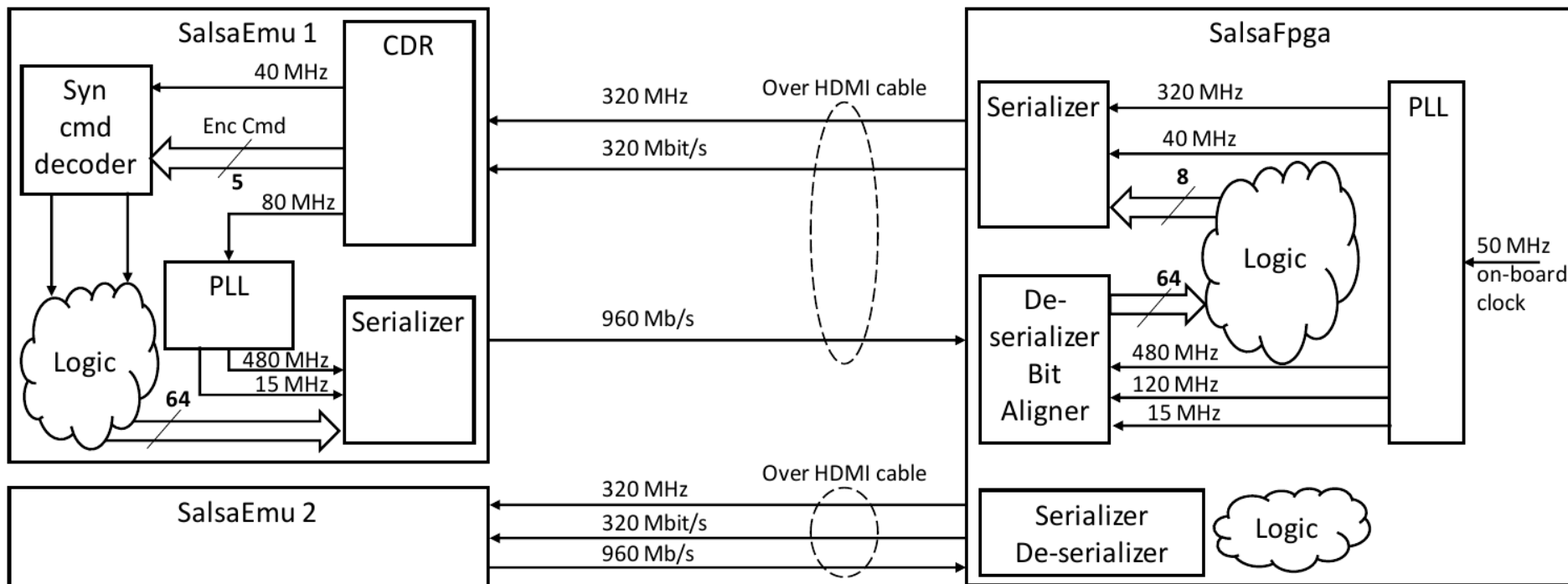
- Current cheap setup
  - Arrix7 boards from Alinx
    - ~100€
- One is running SalsaFpga FW
- Two others SalsaEmu FW



## Tested configuration

- IpGBT like interface

- 320 MHz clock and 320 Mbit/s downlink
- 960 Mbit/s uplink
  - 1.28 Gbit/s is not supported by the Artix7





## ■ eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming 1<sup>st</sup> semester 2026
- Beginning of SALSA2 tests → 2<sup>nd</sup> semester 2026

## ■ eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 1<sup>st</sup> semester 2026
- SALSA3 submission → 1<sup>st</sup> semester 2027
- Performance evaluation → 2<sup>nd</sup> semester 2027 - 1<sup>st</sup> semester 2028

## ■ Very next steps

- SALSA1 tests → Tests on MPGD prototypes, TID tests in February
- PRISMEv1 chip → TID tests in March
- SALSA2 development → in progress