

EICROC - CALOROC status

January 2026

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❑ TSMC will finish EICROC/CALOROC wafers next week (Dec 12): **Done**

❑ Then will start the travel to the packaging

❑ TSMC -> IMEC -> CERN -> OMEGA -> **NCAP** -> OMEGA

❑ Chinese new year Feb 17th – Mar 3rd 2026

❑ EICROC dicing strategy under definition (done for CALOROC)

Wafers already at NCAP

❑ CALOROC substrate approved mid-November

❑ 8 weeks to fabricate: **Available for packaging**

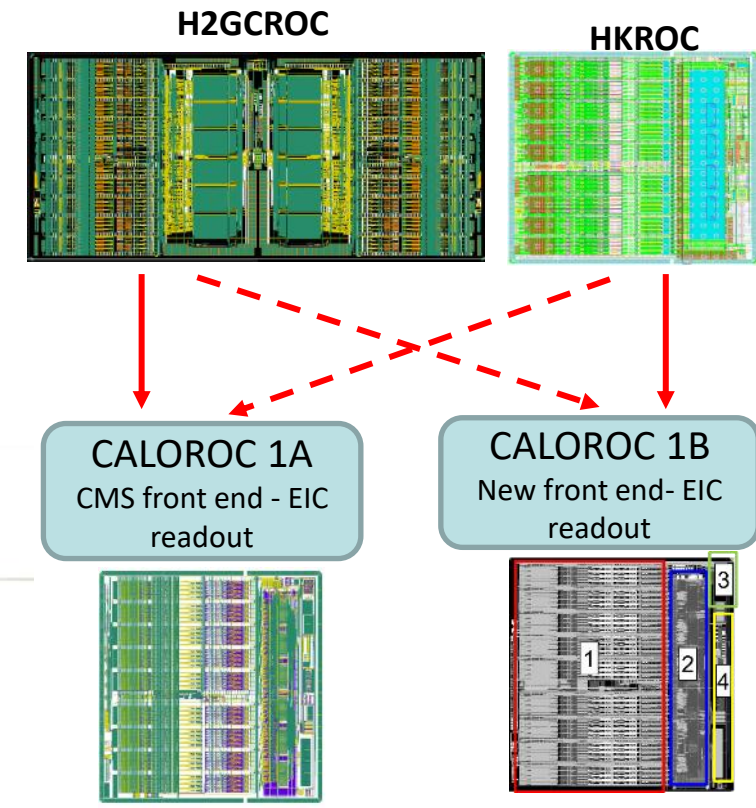
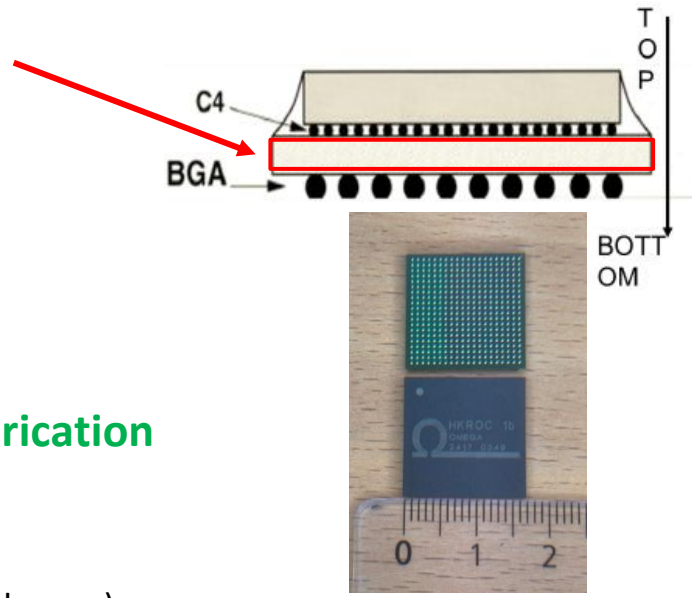
❑ ASICS testboards/PCBs

❑ EICROC 32x32 will go for cabling: **PCB received**

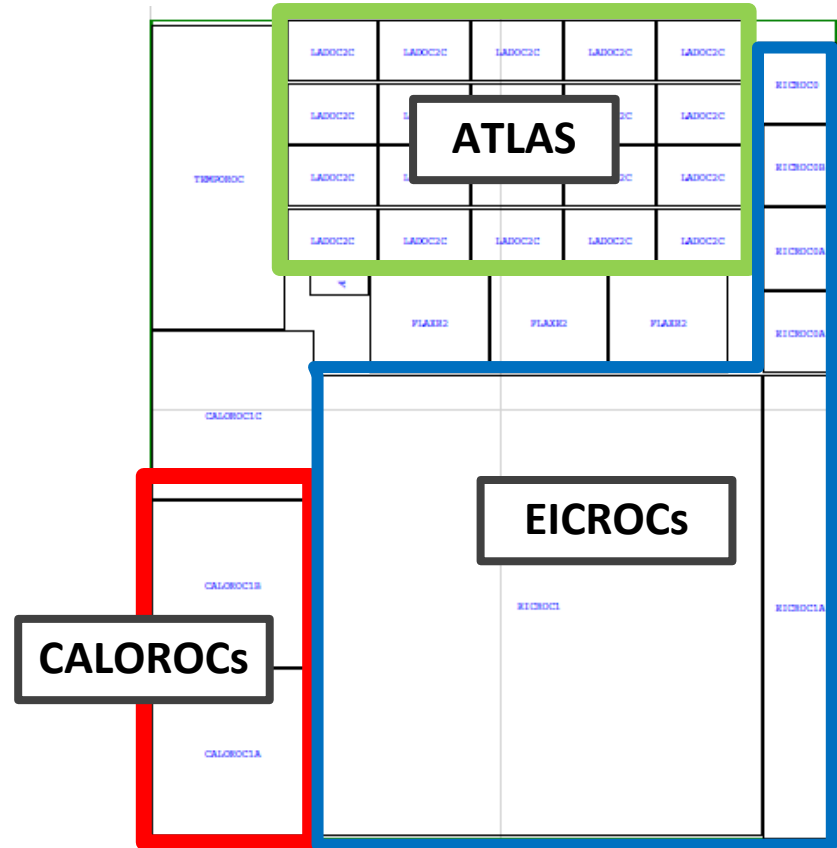
❑ EICROC 4x4 + 4x32 is under PCB fabrication: **PCB fabrication**

❑ CALOROC PCB is under design

- ❑ 1 HKROC testboard available for “first tests”
- ❑ 3 modified-HKROC testboards ordered (ready end of February)
- ❑ 3-5 CALOROC testboards should be available in April-May



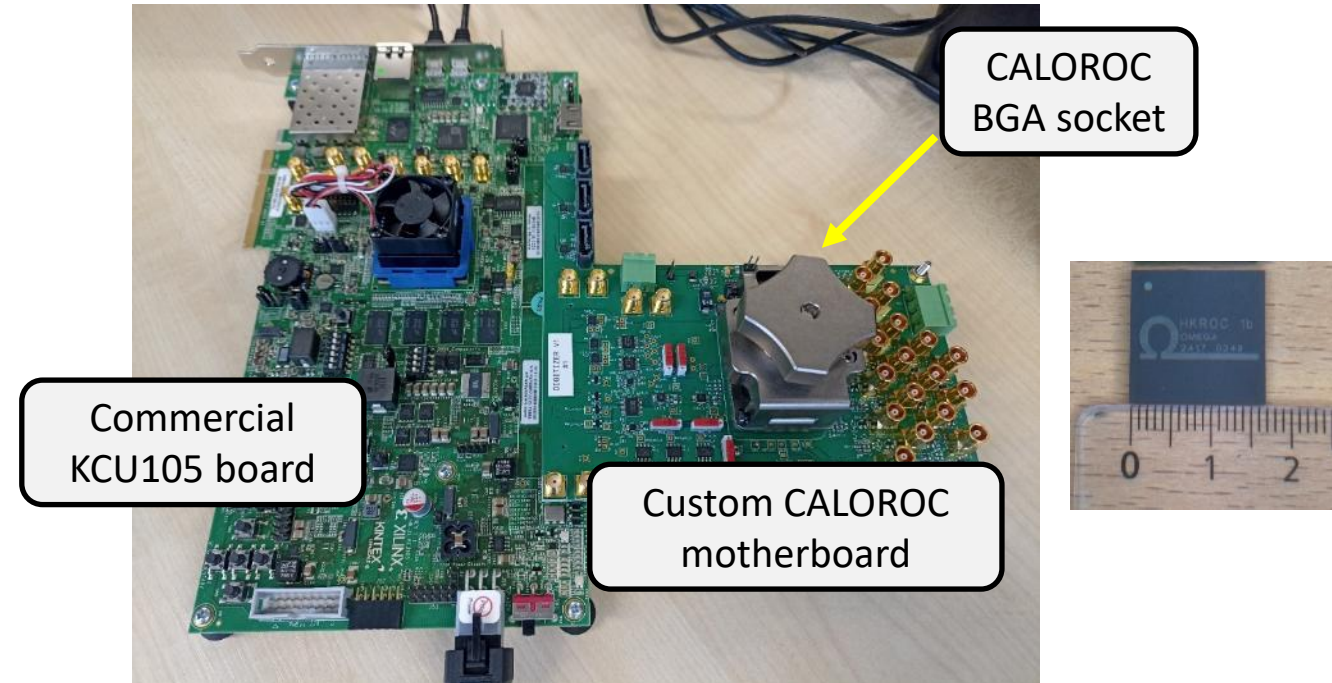
❑ Targeting March for packaged ASIC at OMEGA



- ❑ CALOROC testboard (motherboard) design started in June
 - ❑ Prototypes v1 will be ordered **by the end of 2025**

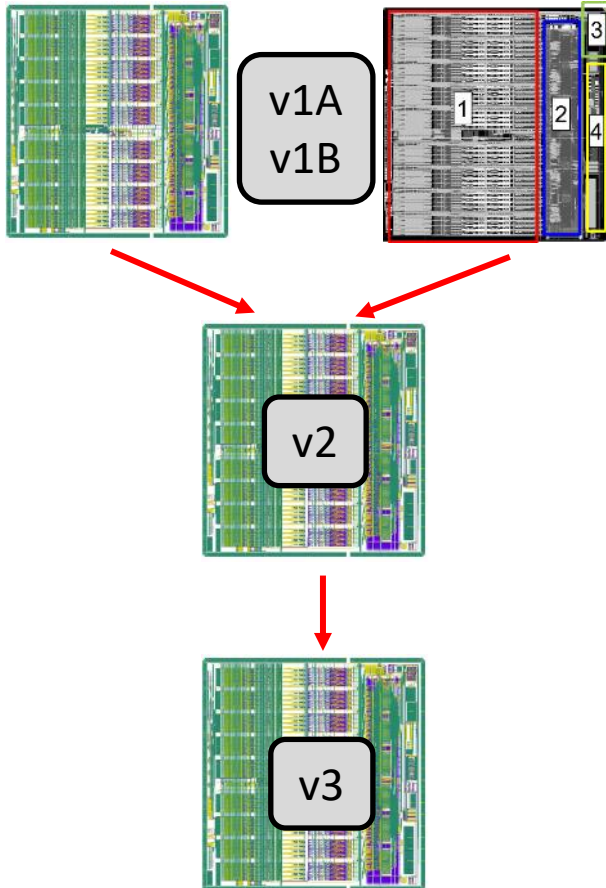
- ❑ 1x CALOROC socket ordered and received (Sept)
 - ❑ 1 will be reused from another project

- ❑ KCU available (now at IJCLAB)





- ❑ Jan 2026: produce and distribute testboards
 - ❑ Characterization (with socket to be ordered)



- ❑ 2026 - Extensive tests and comparison of CALOROCs
 - ❑ End of 2026: selection on performances and system needs
 - ❑ Substrate validation
 - ❑ Same channel count
- ❑ 2027: Submission of selected CALOROC2
 - ❑ If needed new substrate
 - ❑ Substrate validation
 - ❑ Irradiation tests
 - ❑ Robot testboards
- ❑ Q2 2028: Submission of final CALOROC3
 - ❑ To be adjusted with EICROC tech node (130 vs 65 nm)