

eRD109 update: dRICH RDO

P. Antonioli (INFN Bologna) for the RDO team:

Pietro Antonioli, D. Falchieri, Sandro Geminiani, Luigi Rignanese, Giovanni Torromeo

ePIC DAQ meeting
08 January 2026

Updates since 4th December



- no big news given Winter break
- irradiation tests in Trento 12 December
- short term planning + 2026 planning

Irradiation tests

- given pressure due to test beam, we couldn't prepare full scrubbing test
- nevertheless progresses achieved on PolarFire – Artix communication
- irradiation test of new microcontroller candidate (SAMD21 from Microchip)

Radiation Effects on COTS Microcontrollers: Test Methodology, Qualification Results, and Mitigation Strategies

Alessandro Zimmaro
Rudy Ferraro
Salvatore Danzeca
BE-CEM-EPR

06/05/2025

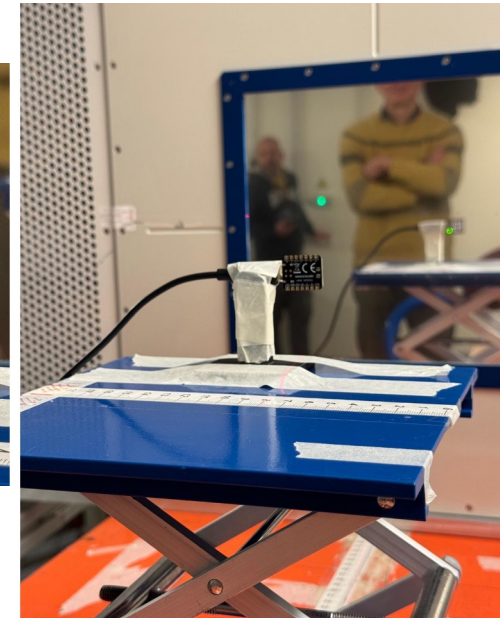
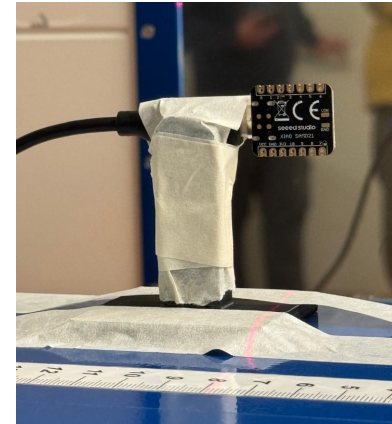
Selected on the basis of [this report](#) from CERN Beams Department

SAMD21 [Datasheet](#)

It has more I/O than previous Attiny uC, which are important to monitor LDO Power Good

Full analysis in progress, however:

- SEU c.s. (RAM) $\sim 3\text{-}4\text{E-}14 \text{ cm}^2/\text{bit}$
- TID \rightarrow worked ok up to 8 krad (~ 16 times TID expected at dRICH)
- failed at very high dozerate (124 rad/s) \rightarrow next run will be tested not powered when at high dozerate



Other news



ePIC dRICH DAQ [talk](#) (PA) at SRO workshop (Catania 10-12 December)



RDO "time ordering"?

BUFFER (1024 x 32 bit): → 1 Mbit full RDO:

- 512 leading words and 512 trailing words
- Leading/trailing edges waiting for matching
- 4.8 MHz : 300 kHz x 8 x 2 + ctrl words

Scheduler:

- Act on the occupancy and the timestamp to select the lane to be read → push data to buffer
- Inspect BUF and build 51bit AWORDs(*)
- Completed 51b words are sent to the DAM via opt links ordered by BC

(*) AWORD = Alcor Word (see next slides)

Take home message* **we aim to send time ordered words (by BC) to the DAM

2026 Challenge: all this needs to be implemented (and validated!) in a "tiny" AU15P FPGA (5.1 Mbit BRAM)

P. Antonioli
INFN- Bologna

ePIC dRICH DAQ
Toward a full data-push architecture

Streaming Readout Workshop SRO-XIII
Catania 9-11 December 2025

24

ALCOR data and ePIC data (II) + link protocol

DISCLAIMER NOTICE: all this is VERY



**Take home message*

RDO "prepares" data reduction
DAM "does" data reduction

50	49	48	47	46	45	39	38	30	29	27	26	24	23	22	21	9	8	0
K CODE	FEB ID	TDC ID	Coarse	Fine	Col. ID	Pixel ID	TDC ID	Coarse (leading)	Fine (leading)									
FLAG	(trailing)	(trailing)	(trailing)	(trailing)			(leading)											

- 51-bit AWORD: leading + trailing
- Bit optimization: EIC orbit / and max ToT

	DF3	DF2	DF1	DF0	DCS (free)	AWORD	AWORD	AWORD	AWORD					
FULL	255	254	253	252	251	204	203	153	152	102	101	51	50	0
lpGBT	223	222	221	220	219	204	203	153	152	102	101	51	50	0

- Protocol over optical link: FULL (256 bits/CLK or lpGBT (224 bits/CLK with FECs))
- if lpGBT, likely used without e-link: "hybrid" mode à la ALICE/GBT
- space for DCS bus (SWT à la ALICE-ITS2)

link protocol operated at **39.4 MHz** CLK (5/2 of EIC clock, close to LHC clock)

- extract BC from bits 21-11
- extract geographic position from RDOID (DAM is link-aware) + FEBID (49-48) + AlcorCh (29-24): geo info → data pattern
- NN decision is reached the DAM must add to the 51-bit word the 11 bits of the RDOID → 62-bit word
- 2 bits added → PCI 64-bit words → dRWORDS (dRICH words)
- dRWORDS out in timeframes to SRO computing

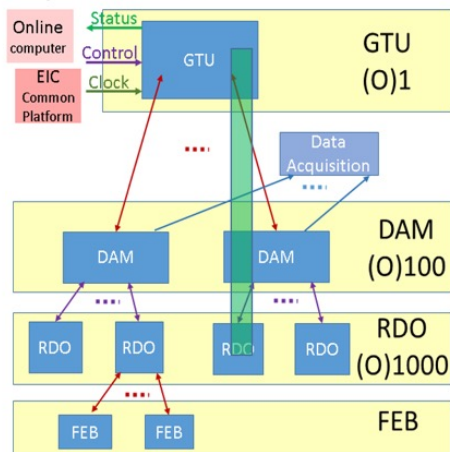
Collaboration with ALICE-DAQ for testing "simple" data transmission on FLX-182

Short term program

- Focus on validate scrubbing model → March in Trento
- Focus on implementing/test IpGBT/FULL protocol using FMC ALINX adaptor provided by Jlab (two cards reached Rome, one will be routed to Bologna) → Thanks David/William!
- two master students assigned for this work (clock/data transmission/data packing)

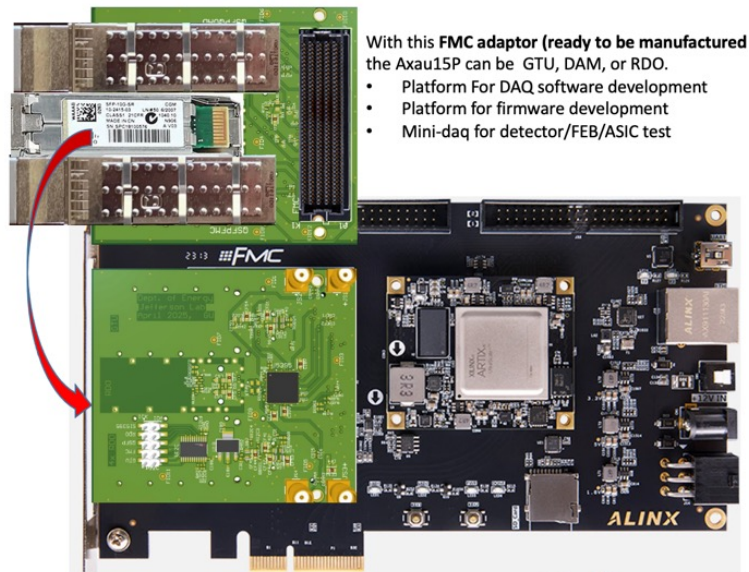
1. The ePIC designs

System Clock: 19.7 MHz (1/5 of BX 98.5MHz)



Mini_DAQ, functionally includes GTU, DAM, and RDO

2. FMC/(Q)SFP adaptor



With this FMC adaptor (ready to be manufactured) the Axau15P can be GTU, DAM, or RDO.

- Platform For DAQ software development
- Platform for firmware development
- Mini-daq for detector/FEB/ASIC test

Jefferson Lab
Thomas Jefferson National Accelerator Facility

This piggy back card is produced (by JLab), this would allow us (BO/RM1) to use a pair of ALINX/AUX15P to mimic a "RDO" and a "FELIX" link

Second step: FLX-182 (Rome1) ↔ RDO (Bo)

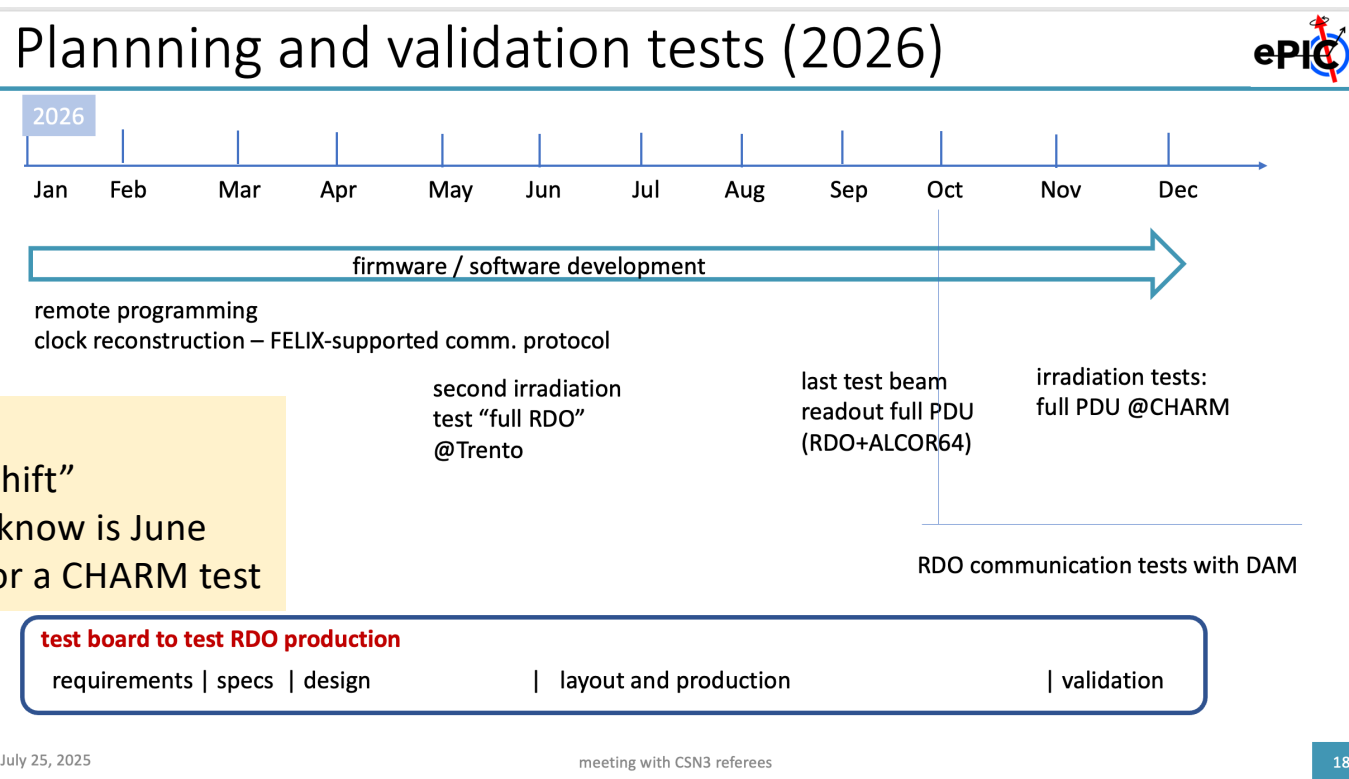
Third step: FLX-155 ↔ RDO

A VLDB+ provided to Rome to practice IpGBT

2026 planning



- dRICH critical test beam now scheduled at CERN for June → focus on ALCOR64 → RDO will be used but still with IPBUS (limited 1 Gbps but Roberto is working on several optimization)
- later in the year integration with “full” readout [IpGBT/FULL] (in the lab, not @ test beam, but reading full prototype)
- comparison IpGBT (FEC5) /FULL under radiation
- plan changes of RDO PCB following lessons learned etc.



This was plan as of July 2025
We might have a 3-months “shift”
but “last test beam” we now know is June
Not clear we will be in time for a CHARM test