KEK Beam Test Updates

2026/1/13

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- H2GCROC
- For the upcoming beam test

Beam Test

- Dec. 1- 10, 2025 @ KEK
  - Using electron beams (1-5 GeV)
  - Validated daisy-chained multi-chip operation under beam conditions
  - Three-layer of v3 quad-chips
    - enabled the definition of coincident events using FPGA timestamps, providing the basis for scaling to large systems with synchronization among and AstroPix layers and between calorimeter and AstroPix layers
  - V4 single chip
    - established critical performance benchmarks for the upcoming v5 sensor.

- Upcoming Beam Test
  - HallD (low energy) by ANL: 2026 March 13 (w1, w2)
    - Run with HGCROC and A-STEP under beam conditions to study the synchronization of two different readouts
    - Run with RCDAQ by Martin
  - KEK by KoBIC
  - HallD (high energy) by ANL : 2026 August 17 (w22, w23)
  - CERN by KoBIC

Beam Test Data Summary

- Assigned beam time for AstroPix ☺: 10 AM, 2025. 12. 9 ~ 5 AM, 2025. 12. 10 (17 hours)

- V3 quad-chip (w112q06)
  - Using parasite beam (4 GeV electron beam; downstream of ITS)

- Three V3 quad-chip stacks (w112q06/w101q04/w101q12)   *chip0 of w101q12 is malfunctional.
  - Using parasite beam (4 GeV electron beam; downstream of ITS)
  - 1 GeV electron beam(~1 kHz): 1 hour 30 mins data-taking ~ Total 5M hits
  - 2 GeV electron beam(2.3-2.4 kHz): 40 mins data-taking ~ Total 5M hits
  - 3 GeV electron beam (1.6-1.7 kHz): 40 mins data-taking ~ Total 5M hits
  - 4 GeV electron beam (~1 kHz): 1 hour 30 mins data-taking ~ Total 6M hits
  - 5 GeV electron beam (~400 Hz): 2 hours data-taking ~ Total 4M hits

- Three V3 quad-chip stacks + two W plates
  - Max buffer. Impossible to save data

- Three V3 quad-chip stacks + one W plate (5 mm thickness = 1 radiation length)
  - W plate Between layer2 and layer3 (w112q06/w101q04/[W plate]/ w101q12)
    - 5 GeV electron beam (438 Hz): 10 mins data-taking
  - W plate Between layer1 and layer2 (w112q06/[W plate]/ w101q04/ w101q12)
    - 5 GeV electron beam (438 Hz): 10 mins data-taking
  - W plate Between layer1 and layer2 (w112q06/[W plate]/ w101q12/w101q04)
    - 5 GeV electron beam (438 Hz): 1 hour data-taking
    - 1 GeV electron beam (1.1-1.2 kHz): 30 mins data-taking

- V4 single chip
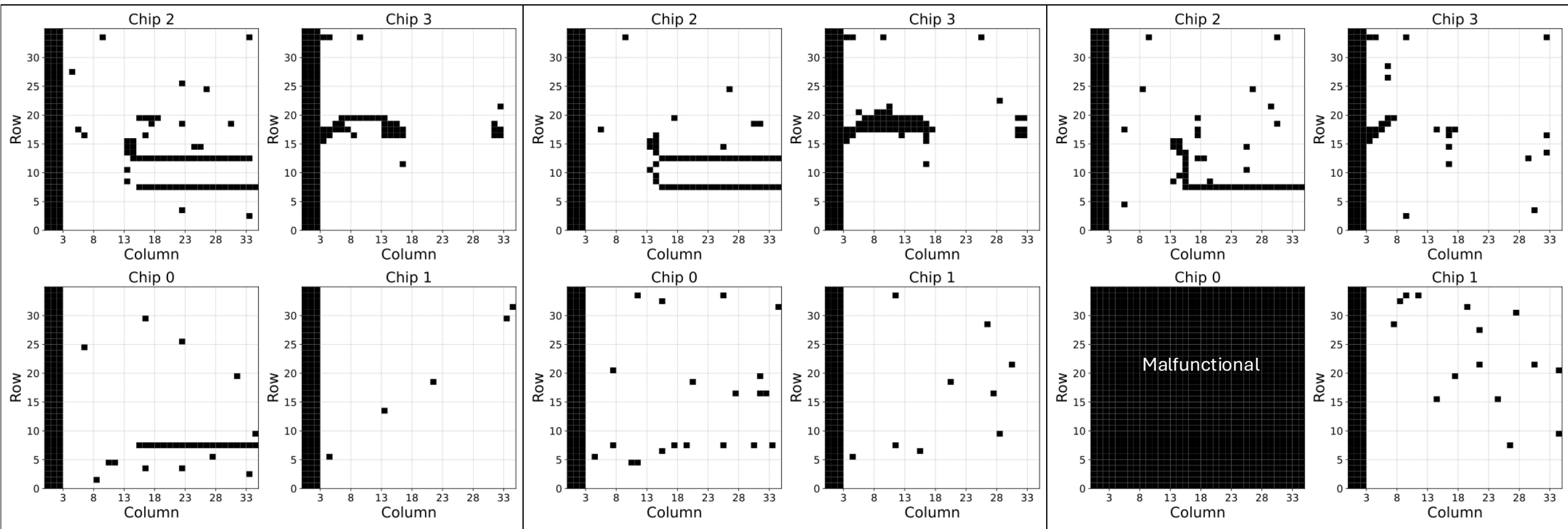 - 3 GeV electron beam (1.6-1.7 kHz)

*During data-taking: 540 mA @5.3V

→ Define one event using FPGA timestamp for synchronization

Mask maps: w112q06/w101q04/w101q12

- Active pixel yield (#. masked pixels)

*Regardless of whether the pixel was enabled or disabled, there was no response on chip0 of w101q12.

Chip 2	86.0 % (172)	Chip 3	88.2 % (145)
Chip 0	88.8 % (137)	Chip 1	91.0 % (110)

Chip 2	86.8 % (162)	Chip 3	86.5 % (165)
Chip 0	89.8 % (125)	Chip 1	90.7 % (114)

Chip 2	87.4 % (154)	Chip 3	89.2 % (132)
Chip 0	0 (1225)	Chip 1	90.2 % (120)

v3 Quad chips: Beam Test Setup

- Parasite beam; 3.5m behind from ITS setup

- 1st v3 quad-chip (w112q06) response under beam environment

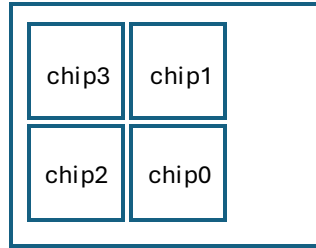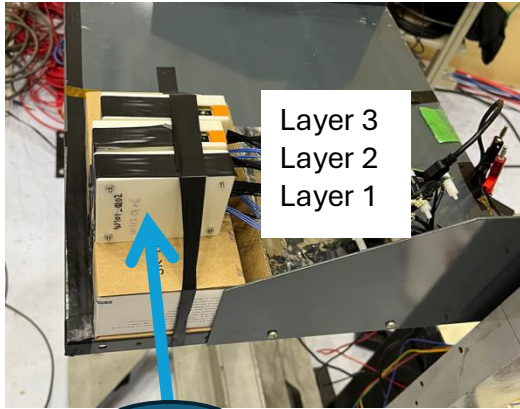- Move vertically and horizontally the beam center
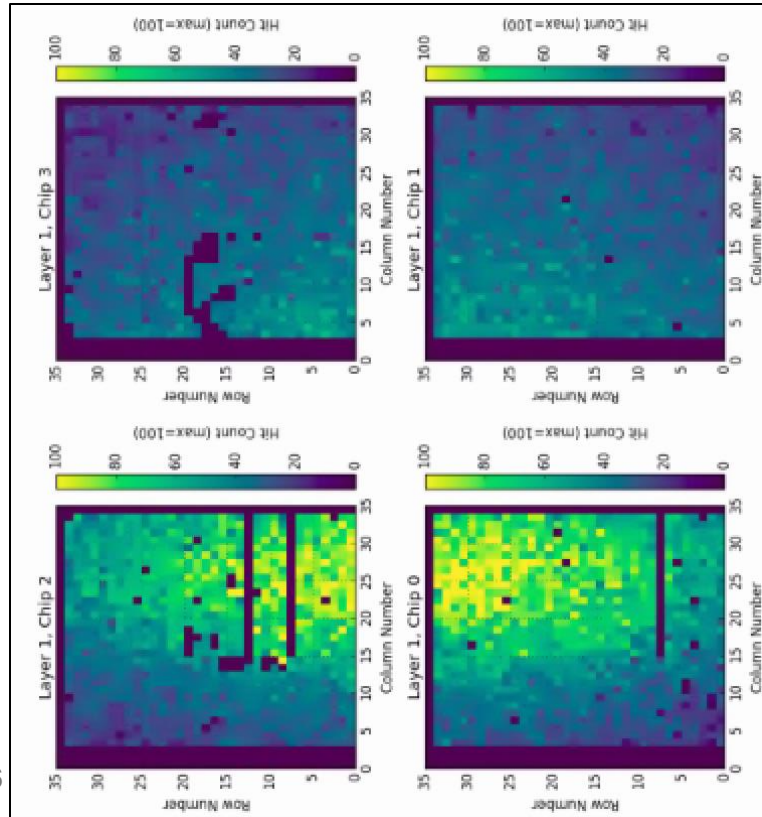
152304 (5 mins run)
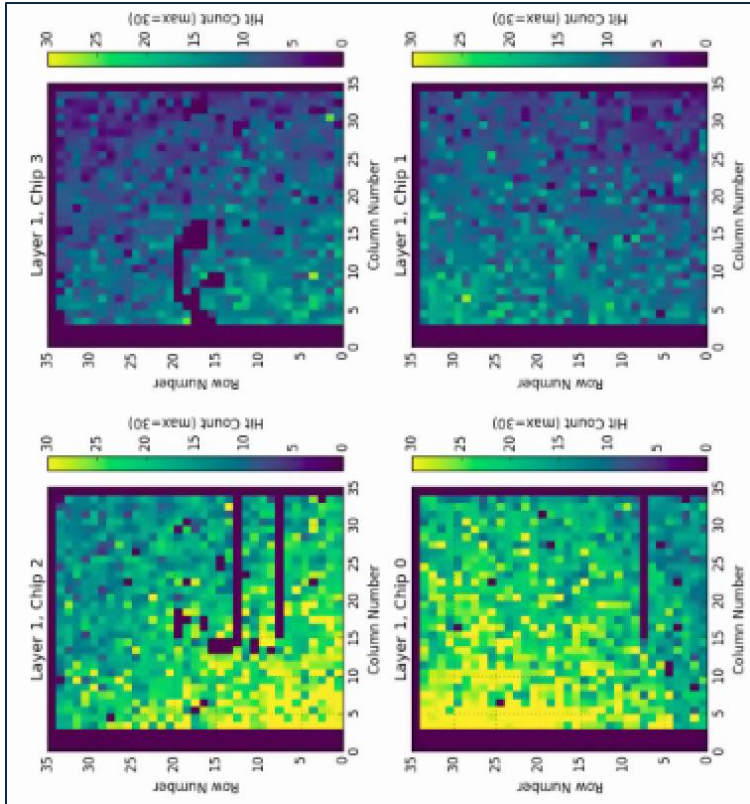
153305 (5 mins run)

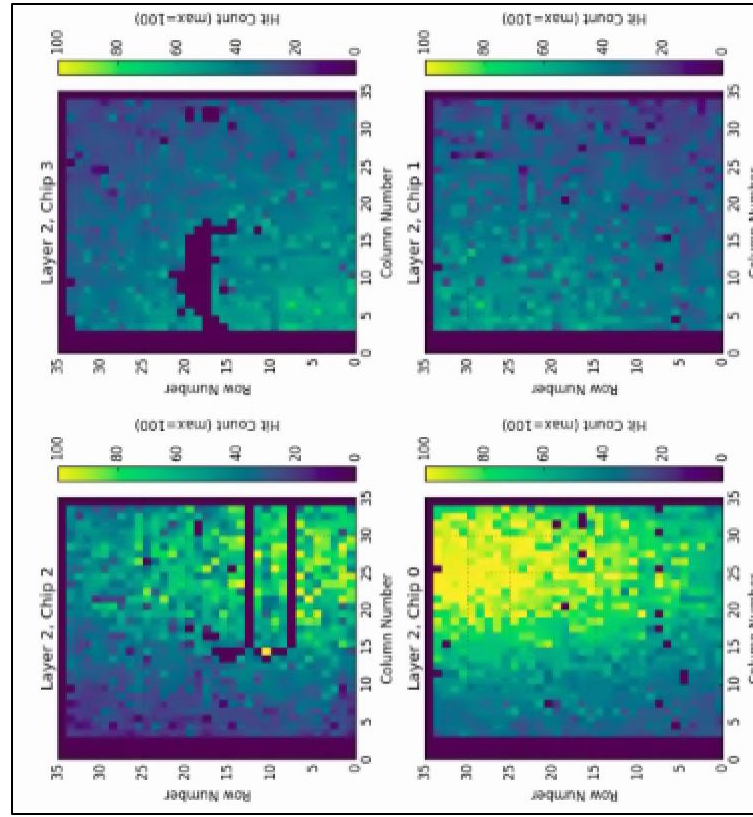# Three v3 Quad chips: Beam Test Setup

Layer 3
Layer 2
Layer 1

beam

| chip3 | chip1 |
| chip2 | chip0 |

- Parasite beam; 3.5m behind from ITS setup
  - 4 GeV electron beam
- 1st three v3 quad-chip stacks response under beam environment
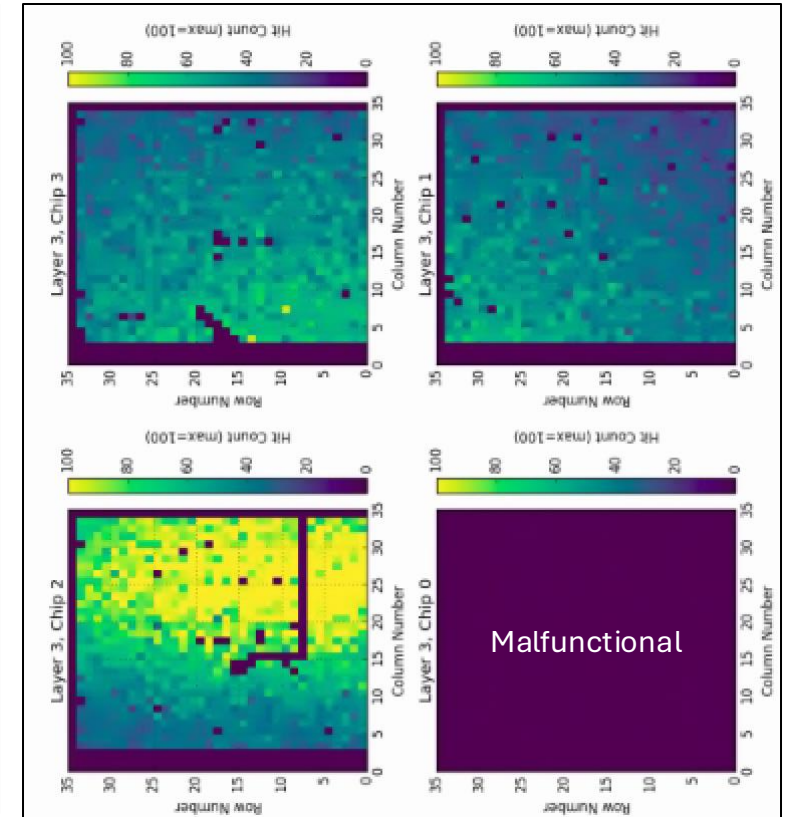- Data-taking rate < 600 (/4096 Max buffer)
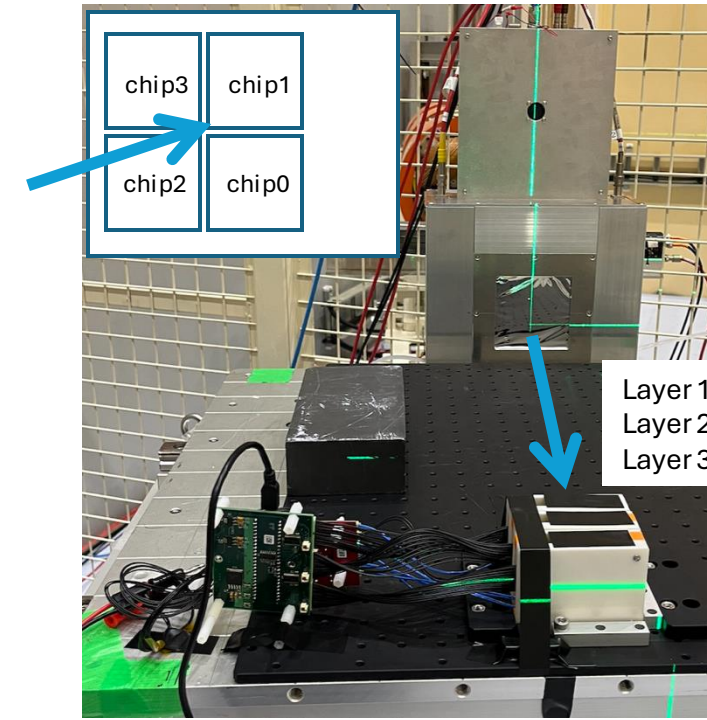
Layer 1 (w112q06)

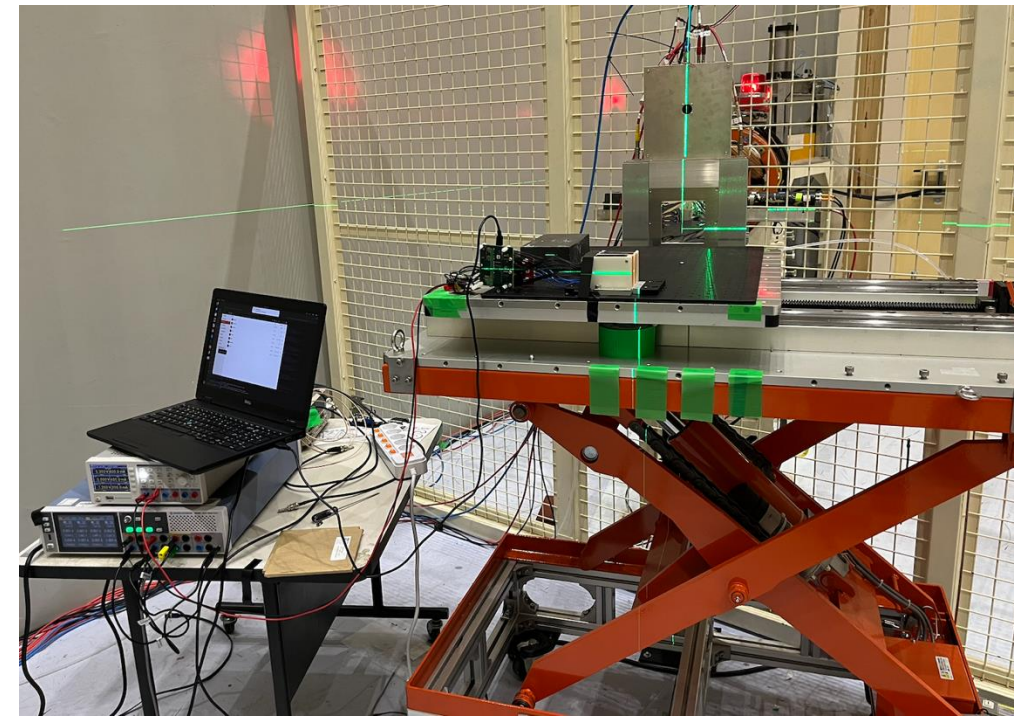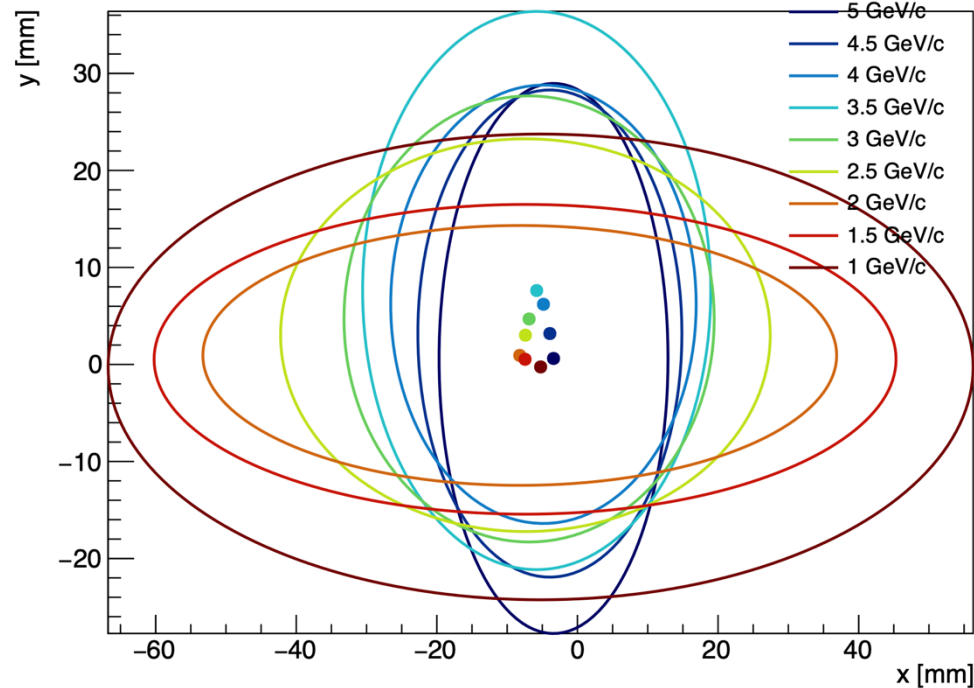### Layer 2 (w101q04)

Layer 3 (w101q12)

Three v3 Quad chips: Beam Test Setup

- 1st three v3 quad-chips stack response under beam environment
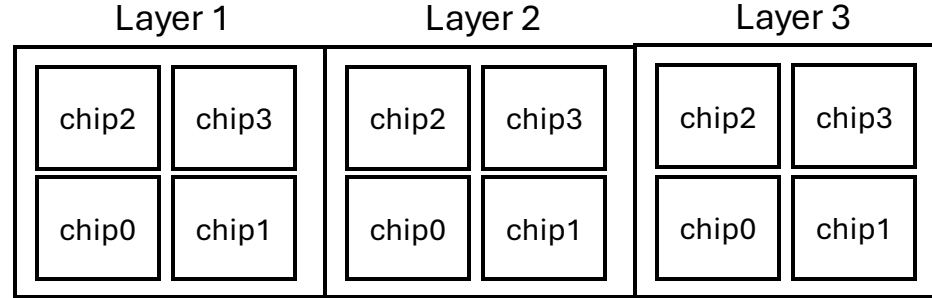- 1, 2, 3, 4, and 5 GeV electron beams → Stable data-taking

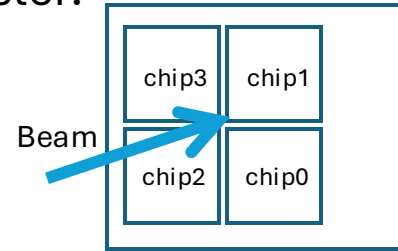| Energy	Beam Rate
1 GeV	1.1 kHz
2 GeV	2.3-2.4 kHz
3 GeV	1.6-1.7 kHz
4 GeV	~1 kHz
5 GeV	400 Hz

Hit Map & ToT Distribution (1/2 GeV electron beams)

Plot:

Layer 1	Layer 2	Layer 3
chip2 chip3	chip2 chip3	chip2 chip3
chip0 chip1	chip0 chip1	chip0 chip1

Detector:
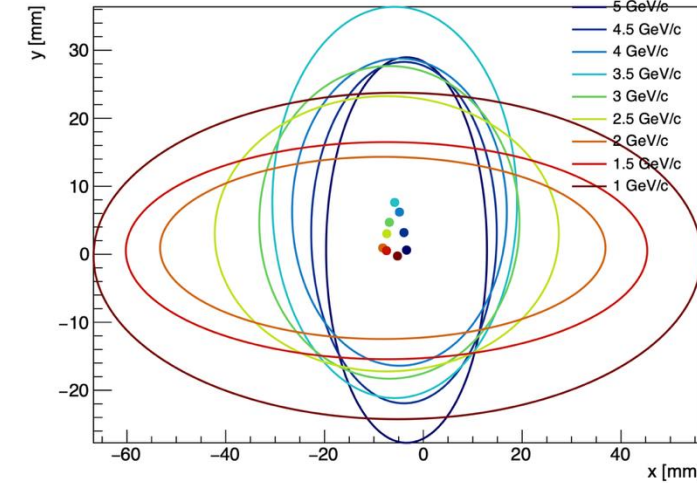
chip3 chip1
Beam →
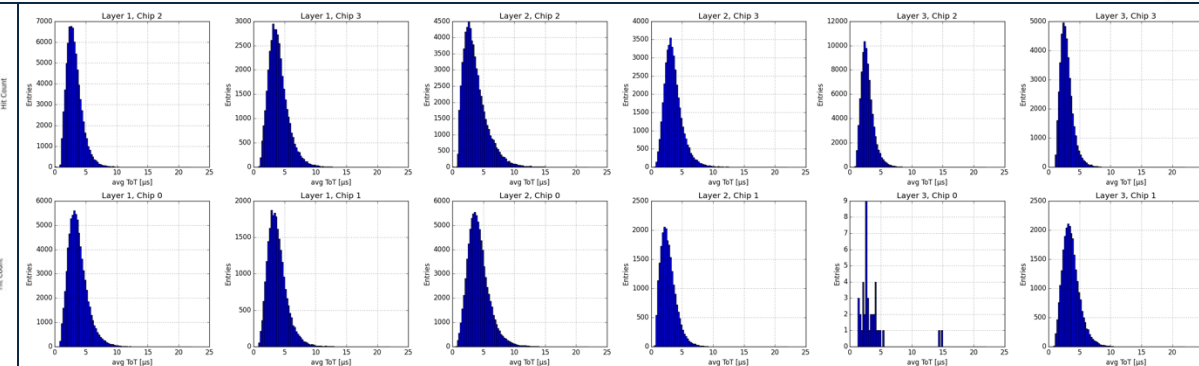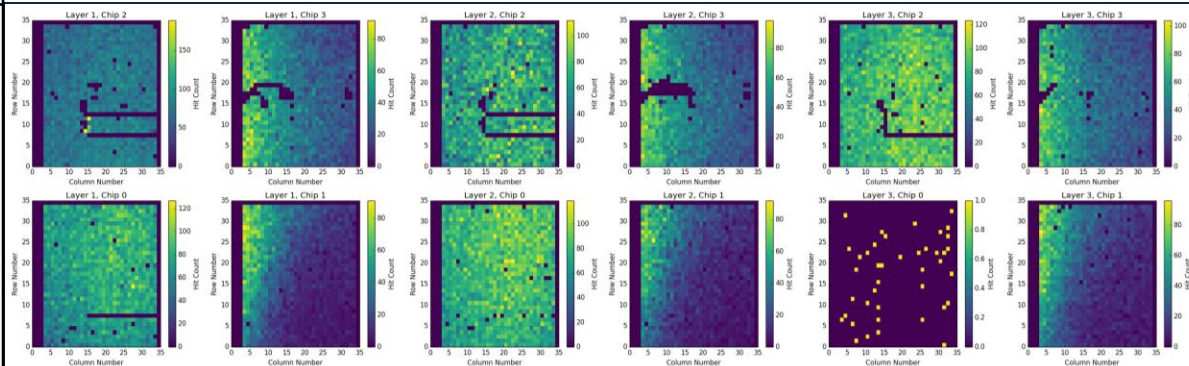chip2 chip0

Beam profile with beam energy change

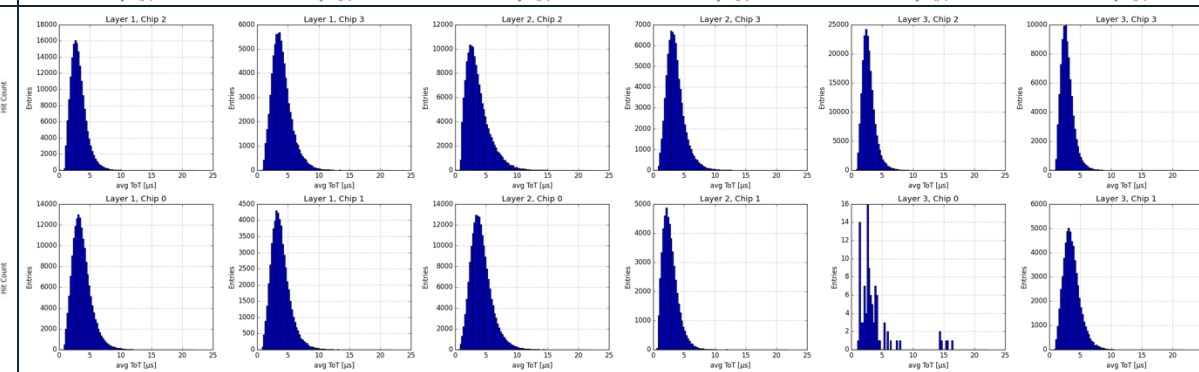*The hit map matches the actual geometry when rotated 90° counterclockwise.

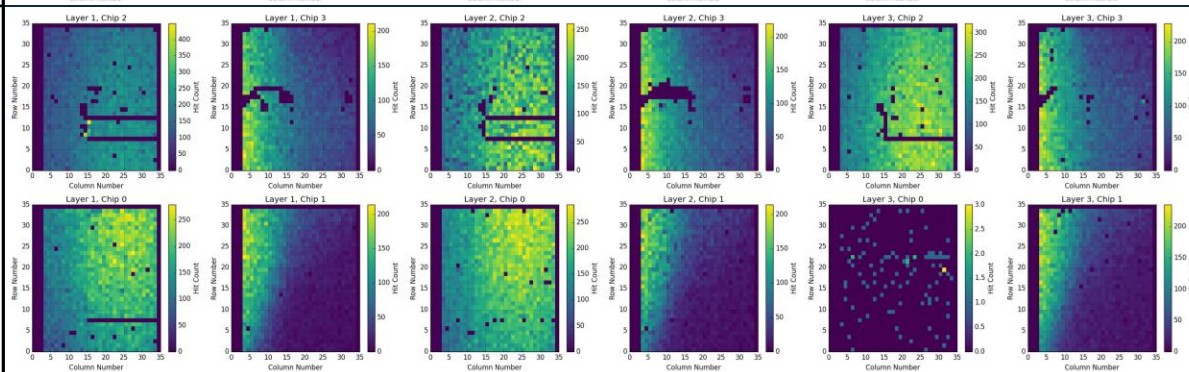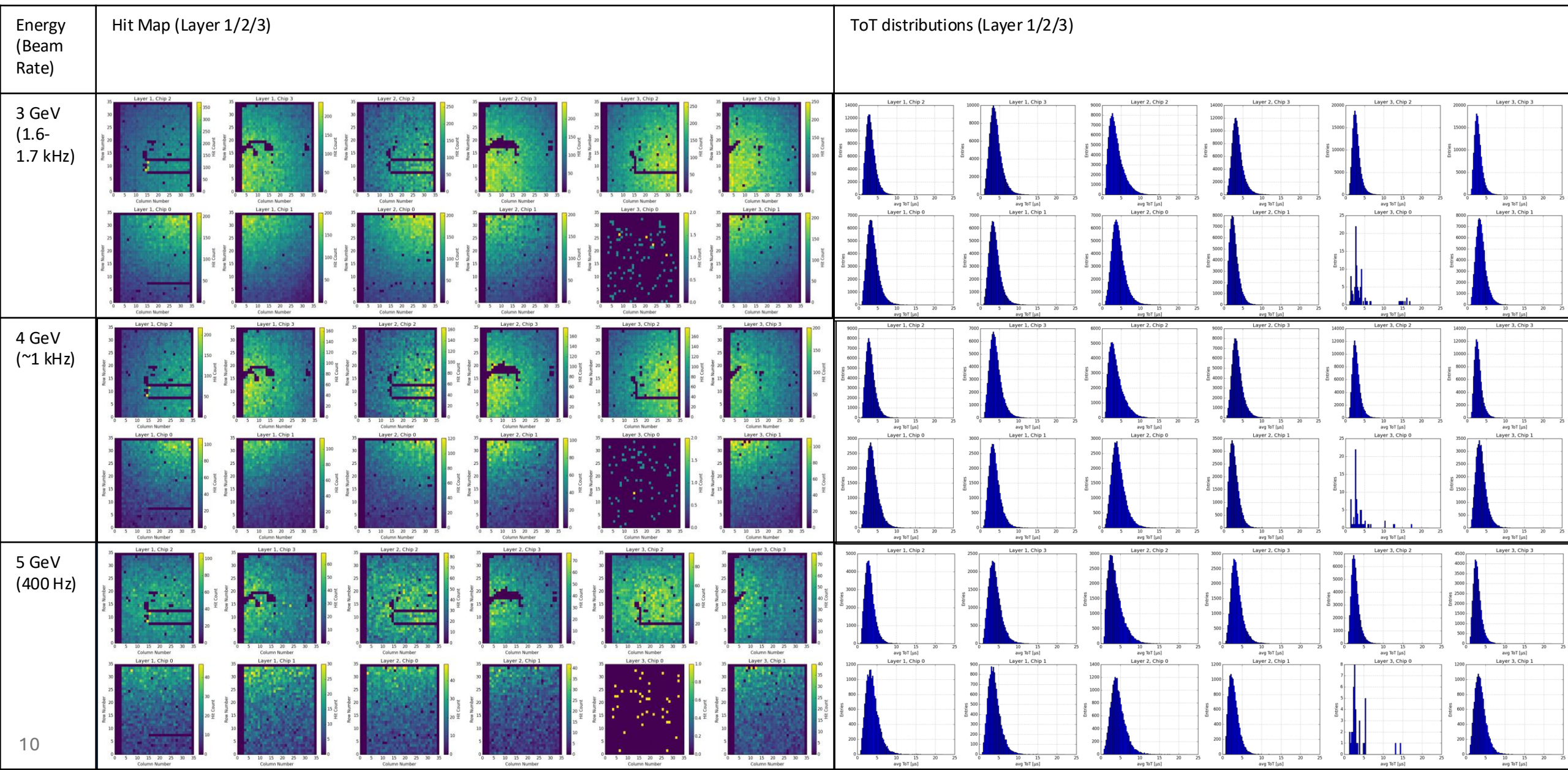| Energy (Beam Rate)		
1 GeV (1.1 kHz)		
2 GeV (2.3 -2.4 kHz)		

Hit Map & ToT Distribution (3/4/5 GeV electron beams)

| Energy (Beam Rate)	Hit Map (Layer 1/2/3)	ToT distributions (Layer 1/2/3)
3 GeV (1.6-1.7 kHz)		
4 GeV (~1 kHz)		
5 GeV (400 Hz)		

Quick check

- Cut applied: require a common timestamp_col across Layers 1–3 (3-layer coincidence)

|	readout	layer		chipID	col	row	timestamp_col		timestamp_row	tot_us_col	tot_us_row	avg_tot_us	fpga_ts_col	fpga_ts_row
2	0	3	2	32	10	217	217	1.035	1.125	1.08	2561612459	2561612417		
3	0	1	3	16	12	216	216	5.175	5.29	5.2325	2561612604	2561612478		
4	0	2	3	11	10	219	219	2.615	2.69	2.6525	2561612608	2561612440		
5	0	1	3	32	13	216	216	8.845	8.945	8.895	2561612730	2561612520		
6	0	2	3	16	12	216	216	5.325	5.42	5.3725000000000005	2561612776	2561612524		
7	0	2	3	17	11	217	217	1.895	2.035	1.965	2561612818	2561612482		
8	0	2	3	32	13	216	216	11.385	11.455	11.42	2561612902	2561612566		
9	0	3	3	14	25	219	219	3.61	3.72	3.665	2561634765	2561634723		
10	0	1	3	3	23	219	219	4.69	4.795	4.7425	2561634771	2561634729		
11	0	2	2	5	24	249	249	3.63	3.695	3.6624999999999996	2561644904	2561644862		
12	0	1	2	11	20	127	127	4.605	4.71	4.657500000000001	2561654513	2561654471		
13	0	1	2	21	15	179	179	3.47	3.575	3.5225	2561666826	2561666784		
14	0	2	2	8	24	32	32	1.345	1.42	1.3824999999999998	2561766719	2561766677		
15	0	1	2	9	24	31	31	3.585	3.675	3.63	2561766731	2561766689		

Readout 38, common TS count=3

TS=205 TS=166 TS=158

Chip 0   Chip 1   Chip 3
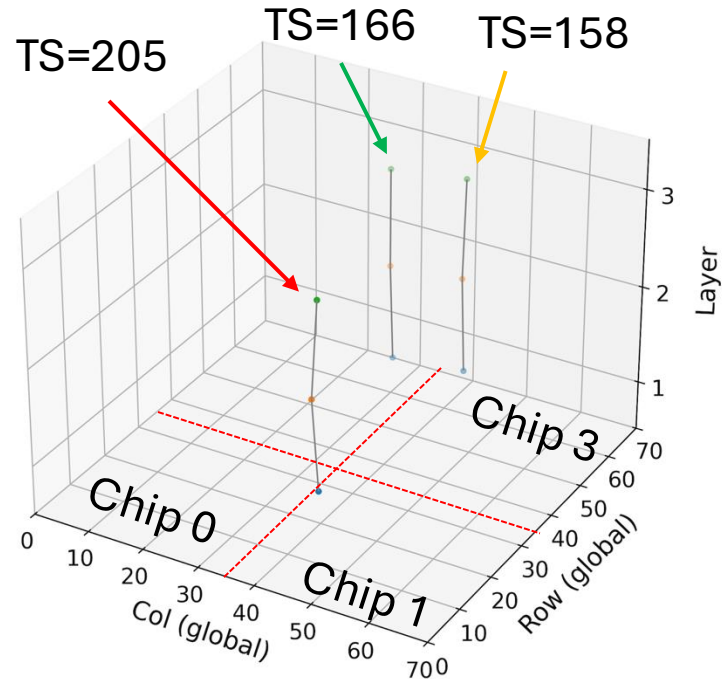
|													
420	38	2	3	3	5	76	76	2.42	2.505	2.4625	2570329353	2570329311	
421	38	2	1	7	14	205	205	1.845	1.93	1.8875	2570371172	2570371130	
422	38	3	1	8	14	205	205	3.5	3.59	3.545	2570371183	2570371141	
423	38	1	1	7	16	205	205	5.79	5.885	5.8375	2570371196	2570371154	
424	38	1	3	9	1	1	1	3.515	3.63	3.5725	2570371401	2570371359	
425	38	3	3	9	24	158	158	2.305	2.415	2.3600000000000003	2570446292	2570446250
426	38	1	3	9	24	158	158	3.835	3.925	3.88	2570446300	2570446258	
427	38	2	3	9	23	158	158	3.14	3.215	3.1775	2570446296	2570446254	
428	38	2	1	4	9	4	4	2.21	2.285	2.2475	2570447854	2570447812	
429	38	3	3	28	29	254	254	2.435	2.55	2.4924999999999997	2570468468	2570468426
430	38	1	2	17	9	40	40	2.905	3.01	2.9574999999999996	2570476620	2570476578
431	38	3	2	32	21	166	166	2.035	2.12	2.0775	2570508025	2570507983	
432	38	1	2	32	22	166	166	4.56	4.655	4.6075	2570508040	2570507998	
433	38	2	2	32	21	166	166	5.71	5.79	5.75	2570508046	2570508004	
434	38	2	2	31	25	58	58	3.12	3.21	3.165	2570536997	2570536955	

Three v3 Quad chips with W plates: Beam Test Setup

- Three v3 quad-chips stack with 5 mm W plate (= 1 radiation length)

- Confirmed the readout capability limitation of the current setup

- **Two W plate between AstroPix layers**
  - under 5 GeV electron (~400 Hz): **Max buffer issue**

- **One W plate** between AstroPix layer (1-2 layer/2-3 layer)
  - 5 GeV electron beam (438 Hz): 1 hour data-taking
  - 1 GeV electron beam (1.1-1.2 kHz): 30 mins data-taking
  - 3 GeV electron beam (1.6-1.7 kHz): **Max buffer issue**

1-2 layer

2-3 layer
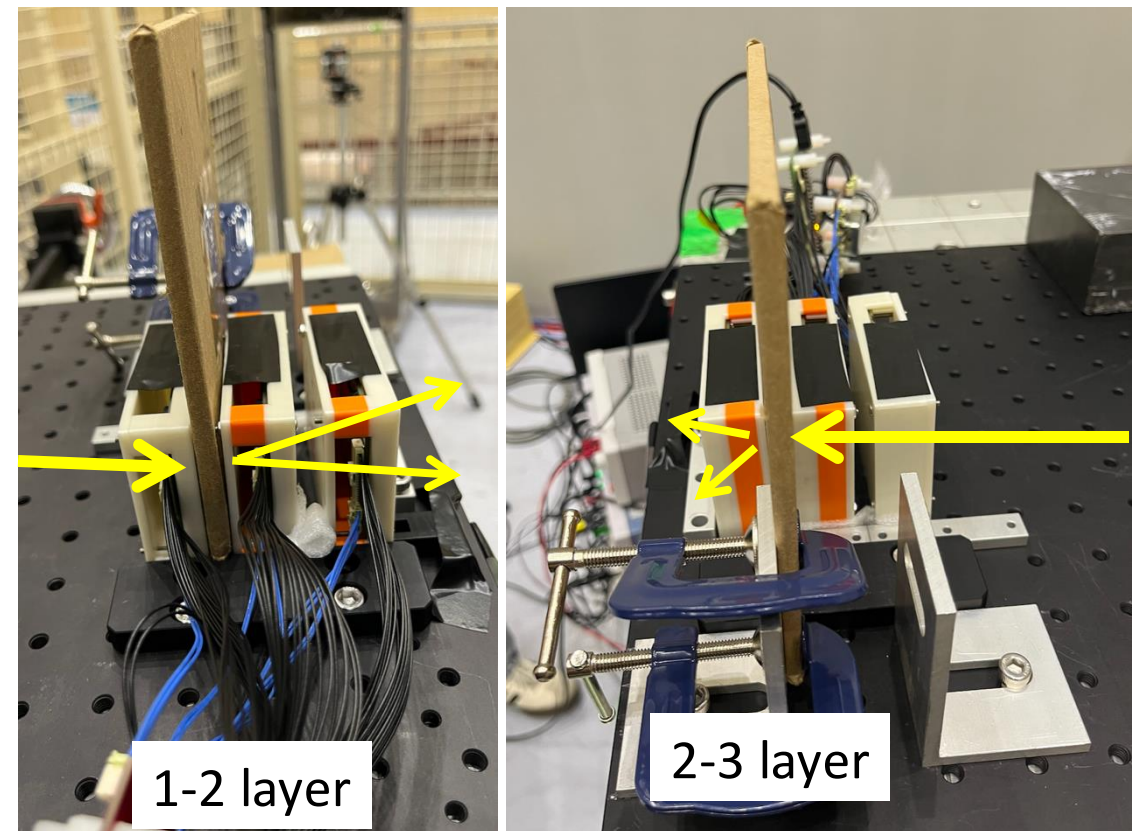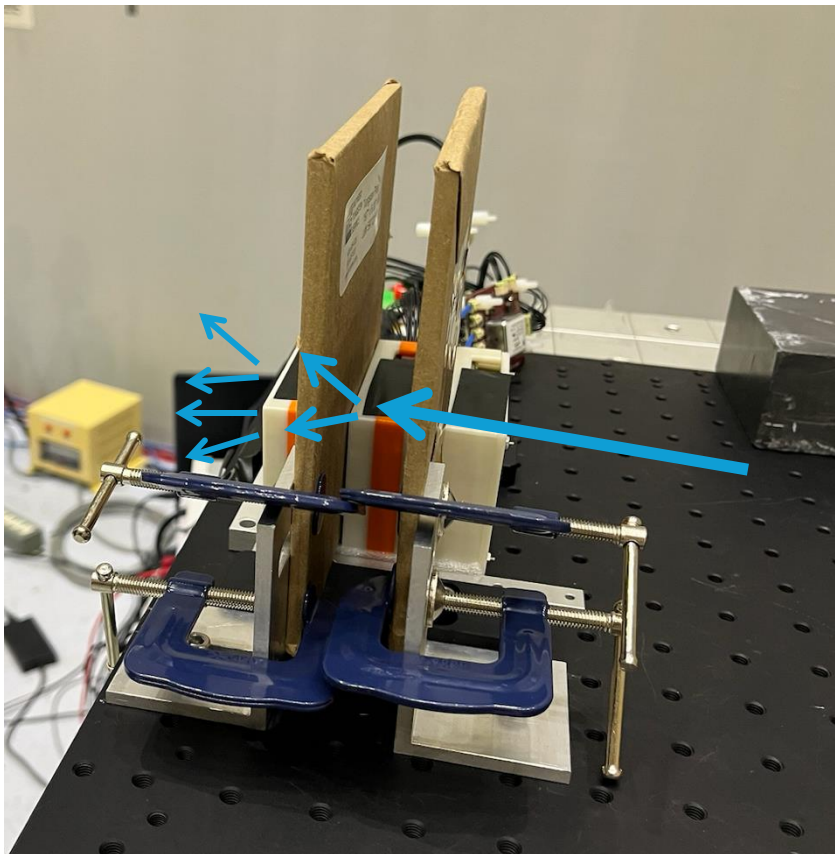
# V4 single chip: Beam Test Setup

- Setup
  - Used same yml file with Grant
  - Bias voltage: -175 V
  - Threshold: 140 mV

- Expected data: 1k events per pixel using 3 GeV electron beam

- Relative calibration
  - Injection curve
  - Am-241/Ba-133 measurement

→ Depletion depth study

→ Last Friday, v4 chip didn't respond to injection voltages
→ Will check it with radiation sources
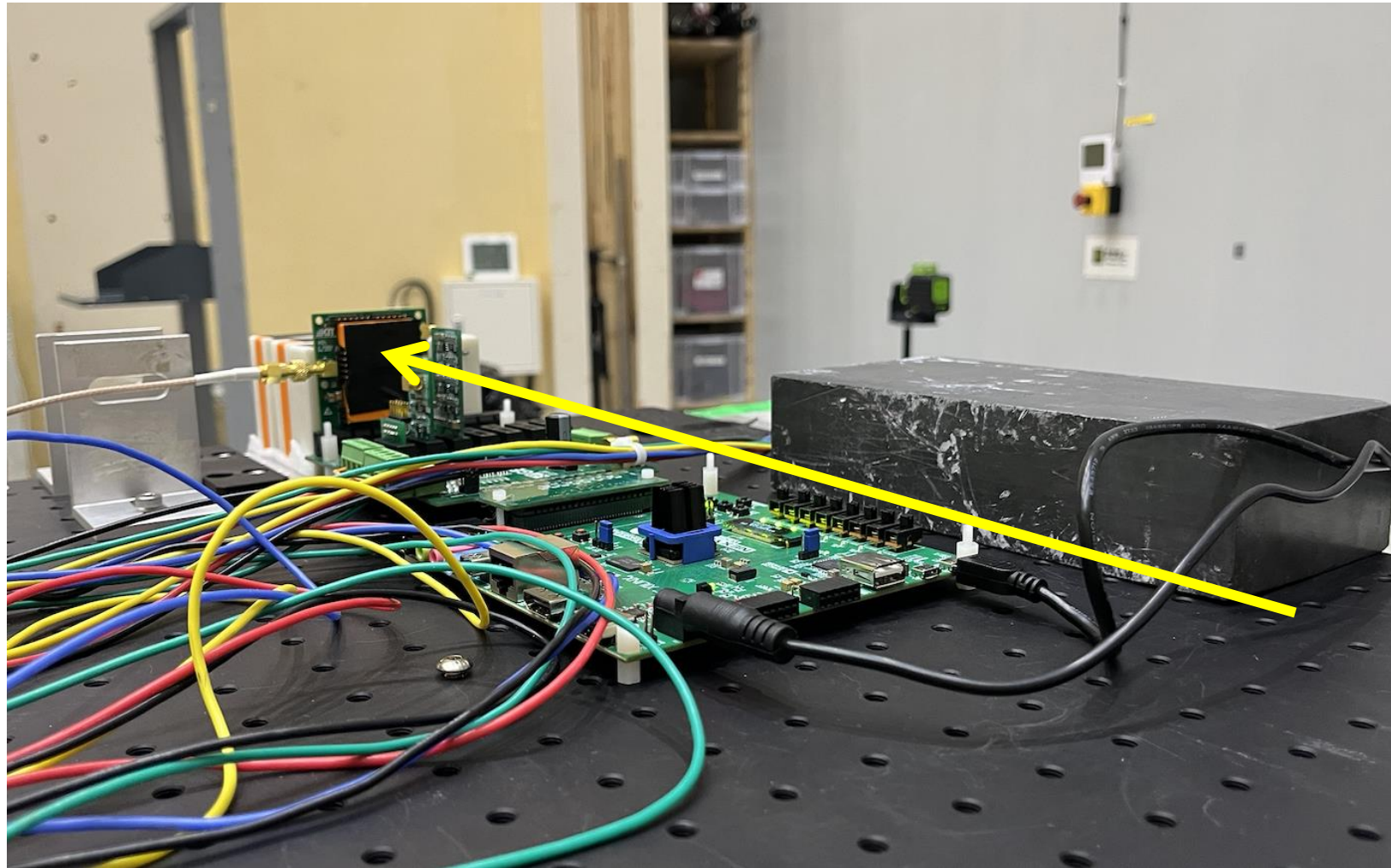
H2GCROC @KNU   (from BoGyeong SEO)

2025 June

2025 Dec.
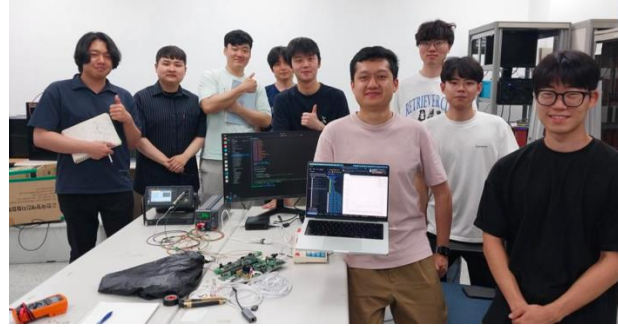
- H2GCROC+KCU105 setup at KNU; same as ANL setup

- SiPM (S14, Hamamatsu; 42 V applied), single channel + SiPM test
  - Using external trigger by function generator for LED power (2V, 20 ns)
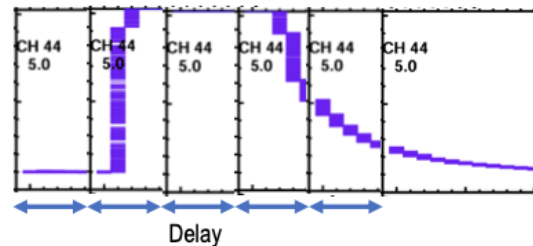 - Run with **different delay** (1 tick = 25 ns)

Run 20 Run 21 Run 22 Run 23 Run 24 Run 25 Run 26 Run 27

CH 44 5.0 (repeated per panel)
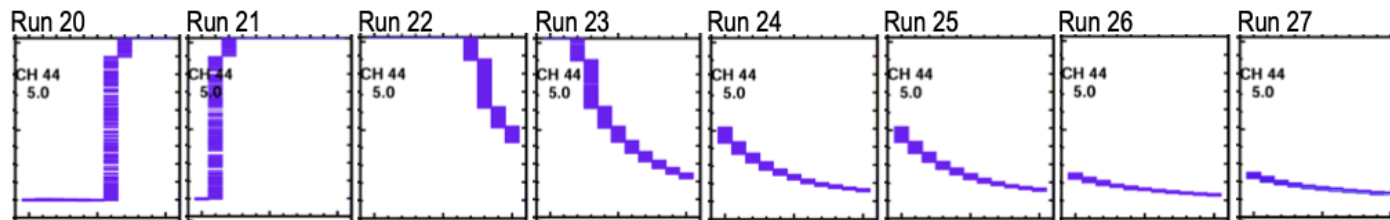
Run with different delay with same signal (same SiPM + LED setup)

```
--- External Trigger ---
Ext Trg En        □
Ext Trg Delay        0   ◇
Ext Trg DeadT        0
```

- Run with **different delay** (1 tick = 25 ns)
- **Same signal** (same SiPM + LED setup)

Waveform reconstruction

CH 44 5.0 (repeated per panel)

Delay

- **New** firmware and UI available from Dec.12, 2025
  - With new firmware and UI, pedestal/ToA/ToT calibration didn't run as expected.

For H2GCROC

- Preamplifier's parameter study
  - to find the best signal-to-noise ratio and a gain adapted to the MIP signal.
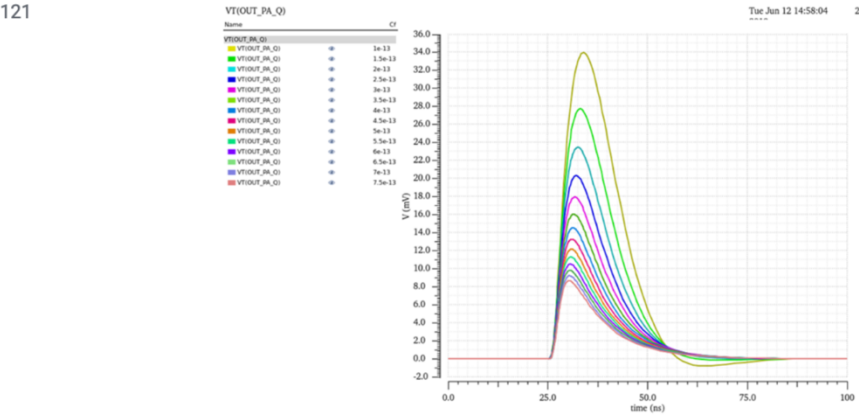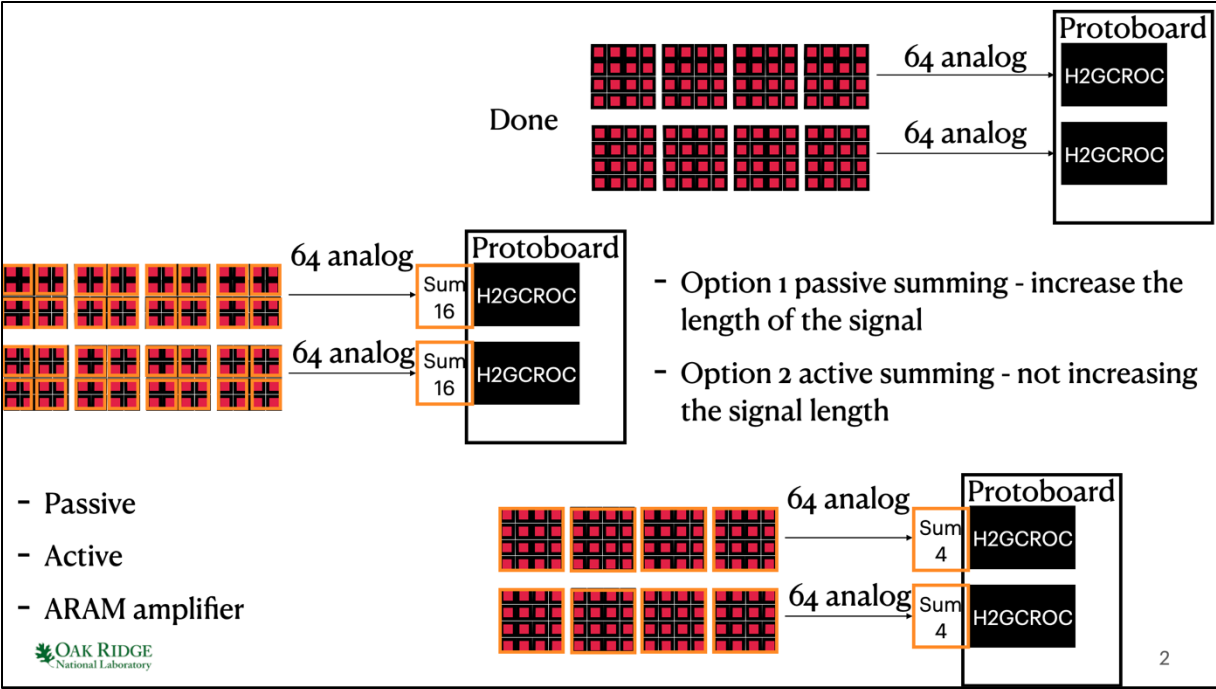 - Using LED as well

Figure 4 Preamplifier response to a 10 fC input charge for different choice of gain.

- Summing boards skim
  - Consider total channels and available HGCROC
  - Readout
    - 16 channels per one SiPM
    - 4 channels per one SiPM
    - 1 channel per one SiPM

For the upcoming beam test

- Hardware for AstroPix
  - Three layers of quad chips
  - 9-chip + quad + quad
  - Three layers of 9-chips
    - Required two more working 9-chip boards
  - 3 9-chips + 3 9-chips + 3 9-chips
    - Required eight more working 9-chip boards
    - Required two more A-STEP

Available now

- Calorimeter
  - One SFIL built by ANL available
  - Two SFIL built by U.Regina available
  - SiPM boards from Norberts: two boards available at ANL

- Software for AstroPix
  - RCDAQ (by Martin)
  - Using common external clock (among A-STEPs and H2GCROC); synchronization event using FPGA timestamp
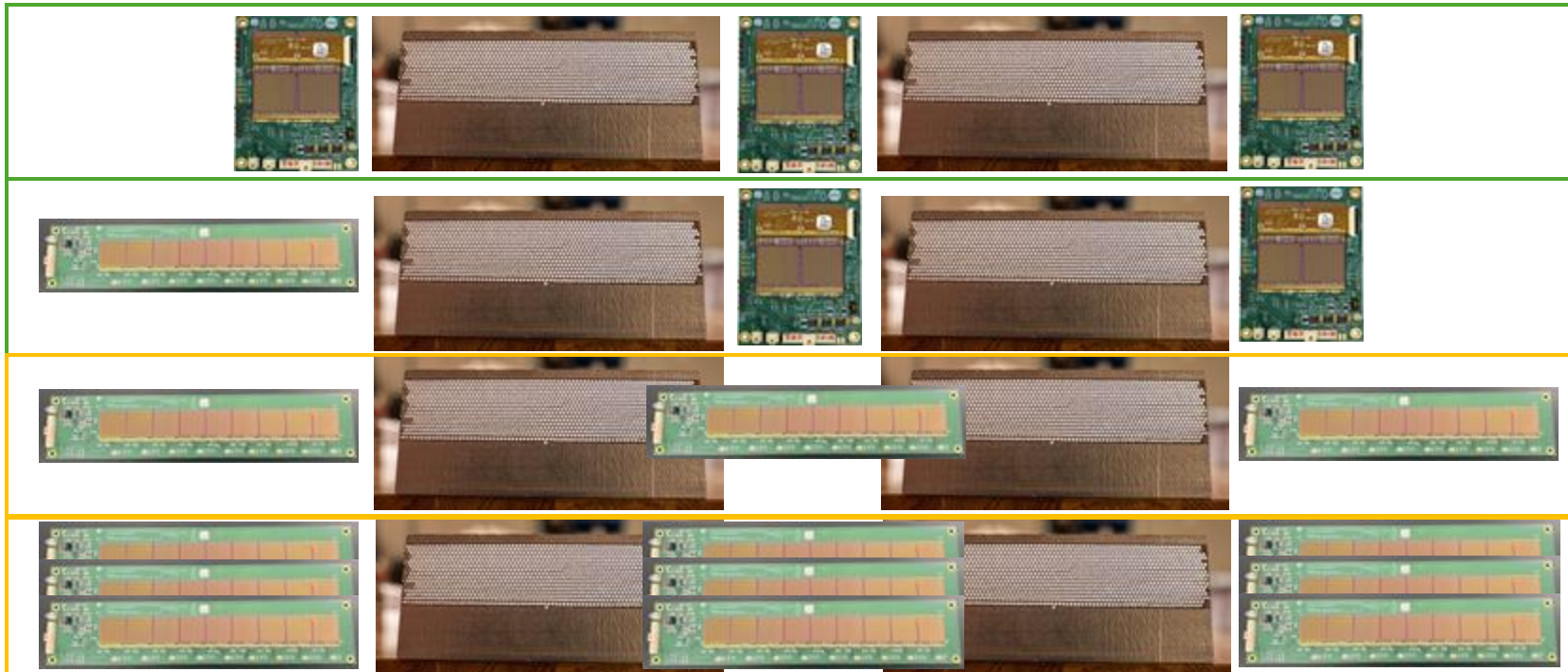
+1 A-STEP

+1 A-STEP

+1 A-STEP

+3 A-STEPs

Depends on
- Available single chips
- Working 9-chip board

Back up