Versatile Link Plus Technical Note

LDQ10 and lpGBT I^{2}C issue

Executive Summary

A functional issue has been identified in the LDQ10 quad laser driver used in the VTRx+ module [1]. A specific I^{2}C bus condition that can occur at reset-time is able to place the LDQ10 into an invalid internal state in which it does not acknowledge I^{2}C transactions, an issue which is deterministic when the triggering condition is met. In systems where the lpGBT is the I^{2}C master, the likelihood of encountering this condition depends on lpGBT startup behaviour, device-to-device variation, and environmental conditions (temperature, supply voltage, radiation dose). It should be noted that even though I^{2}C communication with the LDQ10 is lost, the laser driver remains operational in terms of data transmission with the first channel enabled with its default settings (laser bias and modulation active).

The issue is observed when the LDQ10 is reset while SDA and SCL are both low, followed by a release of SCL before SDA (or when their release happens simultaneously). Recovery is possible by resetting the LDQ10 with at least one I^{2}C line high or by forcing an additional SCL high–low–high sequence while keeping SDA high prior to resuming normal I^{2}C traffic. To minimize risk, the LDQ10 should be released from reset after the lpGBT, e.g., by driving LDQ10 RSTN from lpGBT RSTOUTB or from an lpGBT GPIO to enable remote reset capability. A firmware-based mitigation using only the existing lpGBT I^{2}C master has been developed and validated. The updated firmware has been made available in the GBT-SC gitlab repository.

Prepared by	*Checked by*	*Approved by*
S. Kulis, J. Troska CERN/EP-ESE 1211 Geneva 23 Switzerland *szymon.kulis@cern.ch*	**K. Wyllie, F. Vasey** **S. Baron, S. Biereigel**	—

Document History

Rev. No	Date	Pages	Description of Changes
1.0	21 Jan 2026	All	First Version

Contents

Introduction

User reports and follow-up investigations of the VTRx+ module have revealed a functional issue in the LDQ10 quad laser driver [1]. Under specific conditions in systems where the lpGBT [2] acts as the I^2C master*, this issue causes I^2C communication with the LDQ10 to become non-functional in that the LDQ10 does not acknowledge (or act upon) I^2C transactions. The issue is inherent to the LDQ10 design and is expected to occur deterministically whenever the triggering conditions are met. Whether the issue manifests in a given system depends on the startup behaviour of the lpGBT I^2C master, which can include a stochastic (device-dependent) element. The probability of occurrence of the triggering condition varies between devices and is influenced by environmental conditions such as temperature, supply voltage, and radiation dose. While the occurrence rate cannot be reliably modelled, there is little anecdotal evidence from the user community to suggest that it occurs widely or often. The biggest risk is to systems which do not include a means to remotely reset the VTRX+ module (for example via an lpGBT GPIO or RESETOUTB). It is worth noting that even when I^2C communication with the LDQ10 is disrupted after power-up, the laser driver remains operational in terms of data transfer with the first channel enabled and configured with default settings, i.e., laser bias and modulation remain active. If the issue is triggered after a successful configuration (for reasons outlined later in this document), the LDQ10 remains operational in terms of data transfer and the previously programmed settings persist.

Detailed problem description

The LDQ10 issue is related to the implementation of its I^2C interface, including the use of clock-gating techniques. It has been observed that if the LDQ10 is reset (via the external RSTN pin or its internal power-on reset (POR)) while both I^2C lines (SDA and SCL) are held low, and if SCL is released before or simultaneously with SDA, the LDQ10 internal state machine can become corrupted such that it will not reply to I^2C communication. Recovery is possible either by: resetting the LDQ10 again while at least one I^2C line is high, or forcing an additional SCL high–low–high sequence while keeping SDA high prior to resuming normal I^2C traffic. This malfunction is logical only and does not cause permanent damage or long-term degradation. It should also be noted that this functional issue makes the LDQ10 not fully compliant with the I^2C specification [6]. In particular, I^2C-bus compatible devices are expected to reset their bus logic upon receipt of a START or repeated START condition such that they anticipate the subsequent target address phase, even if START conditions are not positioned according to the proper format. This behavior is not always correctly implemented by the LDQ10 under the conditions described above. Although the issue was discovered in the context of power-up, the analysis, simulations, and experimental validation that have been carried out indicate that the LDQ10 can be brought into the same non-responsive state even after an initially successful reset sequence. One example is simultaneously pulling both SDA and SCL low for a prolonged interval (on the order of hundreds of nanoseconds or longer). While the lpGBT master is not expected to generate invalid I^2C sequences, the susceptibility to external disturbances (e.g., EMC-related and/or radiation-induced single events) should be carefully assessed at the system level and means of recovery from this situation should be foreseen.

A contributing factor is that some functional blocks within the lpGBT I^2C master controller do not have an asynchronous reset and may therefore power up in a nondeterministic state. As a result, the lpGBT may temporarily pull SDA and/or SCL low during its reset sequence before releasing both lines when initialization completes.

In summary, the problematic case requires the following sequence:

1. the lpGBT starts up with both SDA and SCL pulled low,

2. the LDQ10 reset is released while both lines are low, and

3. during lpGBT initialization completion, SCL is released before (or simultaneously with) SDA is released.

---

*Other I^2C masters could conceivably cause the same problem, so far the issue has only been observed with the lpGBT

Exposure and mitigation

Systems that externally enforce reset sequencing such that the lpGBT exits reset and releases the I^{2}C lines before the LDQ10 is released from reset are not expected to be affected. In systems where both devices are reset simultaneously, or where the lpGBT is released from reset later than the LDQ10, the issue may occur with a probability driven by the chance that both I^{2}C lines are low at the time of the LDQ10 reset being released. In systems relying solely on the internal POR circuits (i.e., without external reset control) and assuming identical power-supply rise times for the VTRX+ module and the lpGBT (they share the same supply rail), the issue is generally not expected because under the same environmental conditions the LDQ10 POR pulse is longer than the lpGBT POR pulse, which tends to release the lpGBT from reset first. However, due to device-to-device variation, this behavior cannot be guaranteed nor reliably quantified for arbitrary device pairs.

To ensure reliable operation of I^{2}C communication in Versatile Link+ systems, it is recommended to enforce a reset sequence in which the LDQ10 is released from reset later than the lpGBT. This can be achieved by connecting the LDQ10 RSTN pin to the lpGBT RSTOUTB pin. As an alternative, the LDQ10 RSTN pin may be driven by an lpGBT general-purpose I/O to provide remote reset capability.

For systems where the reset sequence cannot be guaranteed and PCB modifications are not feasible, a mitigation that relies solely on the existing lpGBT I^{2}C master and uses the lpGBT-FPGA [3] and GBT-SC [4] cores has been developed, validated, and documented in [5]. The approach requires a specific sequence of IC transactions with tightly controlled timing; therefore, a firmware-based change is proposed to ensure the required timing behavior. In the proposed solution, a new module named `ic_top_with_vtrx_i2c_recovery` is provided. It wraps the existing `ic_top` module and is intended as a drop-in replacement, with the only functional difference being the exposure of two additional control signals: `vtrx_i2c_recovery_i2c_master_id` and `vtrx_i2c_recovery_trigger`. These signals are used to indicate which lpGBT I^{2}C master the VTRx+ module is connected to and trigger the recovery sequence, respectively. In addition, a `vtrx_i2c_recovery_busy` signal is provided to indicate that the recovery sequence is in progress. This solution removes the need for the user system to implement precise timing control for the recovery sequence. However, in systems that already provide a mechanism to generate precisely timed IC transactions, there is no need to adopt the new wrapper module; users are encouraged instead to implement the recovery sequence documented in the MR [5].

Wider impact

Due to widespread design re-use of the I2C block implementations (both slave and master), all ASIC design teams using the affected blocks have been informed of the potential issue and should assess any impact on their ASICs and systems. The design teams of other ASICs implementing I^{2}C slaves are invited to check their logic test coverage for this particular issue.

Conclusion

The functional issue recently identified in the implementation of the I^{2}C block of the LDQ10 has been investigated and reproduced in functional testing and chip simulation. The lock-up of the I^{2}C slave as a response to certain bus states can be mitigated at the system design level using the design guidelines outlined above. A means of in-system mitigation is provided through an update of the GBT-SC core.

Acknowledgements

References

[1] Jan Troska, "Versatile Link Plus Technical Specification, part 2.1.3: Quad Laser Driver". Available: `https://edms.cern.ch/ui/file/1719330/1/VLplus_quadLDD_spec_v1.5.pdf`

[2] P. Moreira, et all. "lpGBT manual" 2021. Available: `https://cern.ch/lpgbt/`

[3] "lpGBT-FPGA Core". Available: `https://gitlab.cern.ch/gbt-fpga/lpgbt-fpga`

[4] "GBT-SC module for FPGA". Available: `https://gitlab.cern.ch/gbtsc-fpga-support/gbt-sc/`

[5] "Add VTRx+ I2C recovery sequencer" Merge Request 11 to GBT-SC core. Available: `https://gitlab.cern.ch/gbtsc-fpga-support/gbt-sc/-/merge_requests/11`

[6] NXP Semiconductors, *UM10204: I2C-bus specification and user manual*, Rev. 7, Oct. 2021.