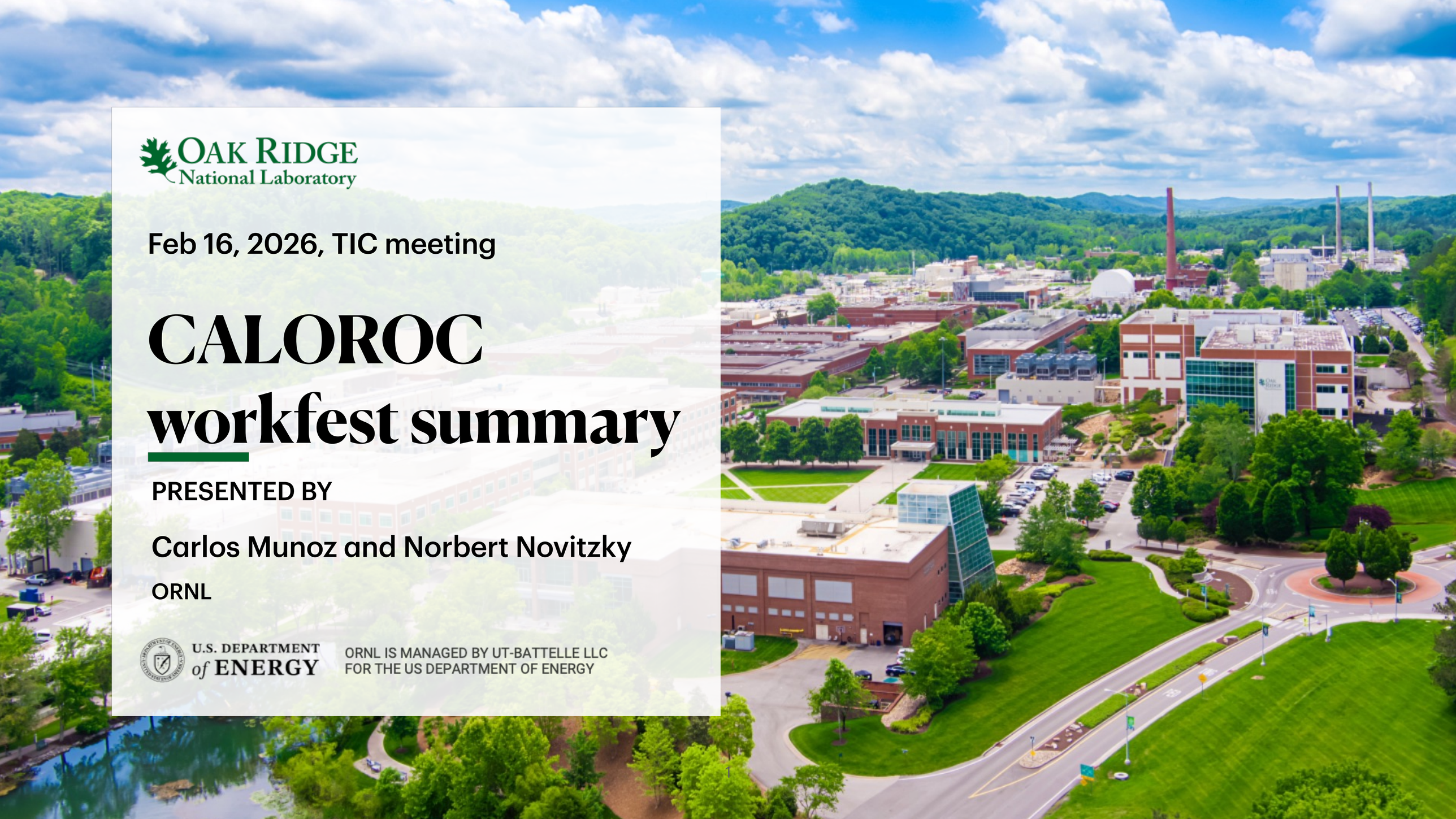


OAK RIDGE National Laboratory

Feb 16, 2026, TIC meeting

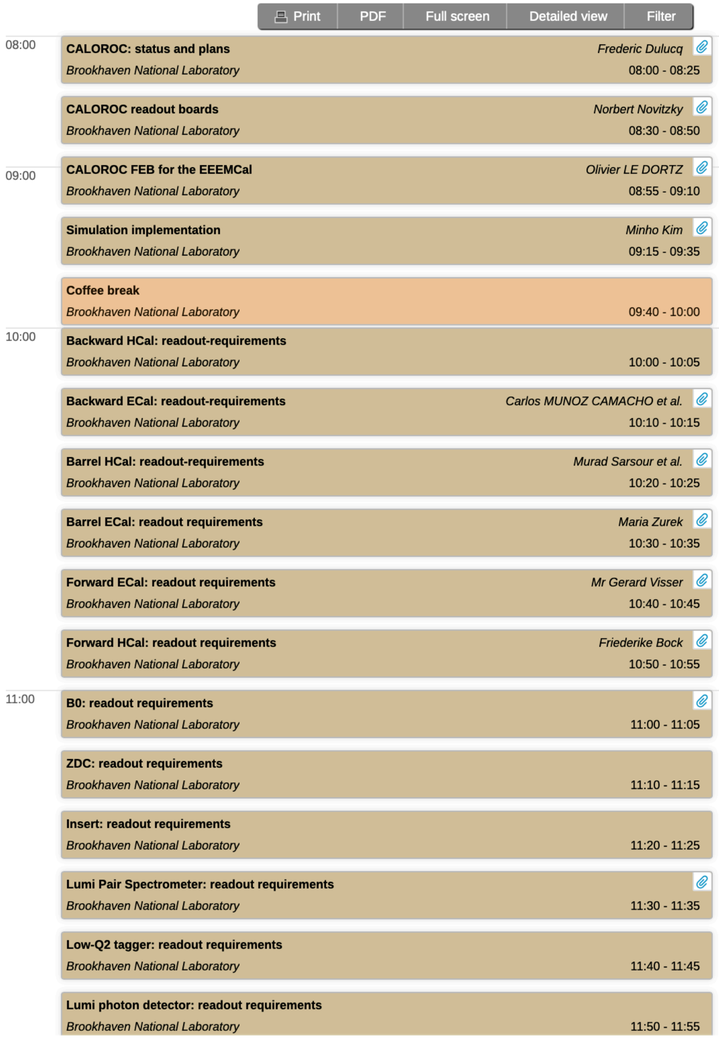
CALOROC workfest summary

PRESENTED BY

Carlos Munoz and Norbert Novitzky

ORNL

First CALOROC workfest on ePIC



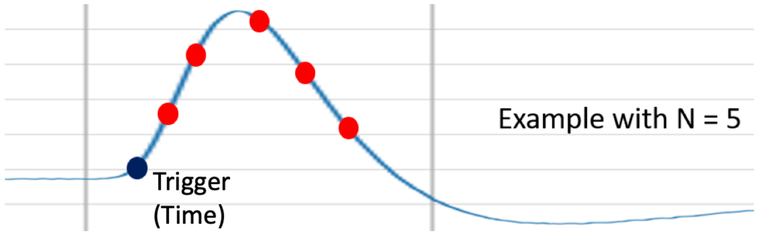
Goal was to inform every calorimeter on the CALOROC development, readout electronics and plans for the next year(s).

Second goal was to update each calorimeter with the requirements using the new updated simulation, testing with H2GCROC.

- Include also the far-forward detectors in case we could apply the chip to their detectors too

CALOROC waveform digitizer with auto-trigger

- CALOROC is a waveform digitizer working @ 39.4 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)



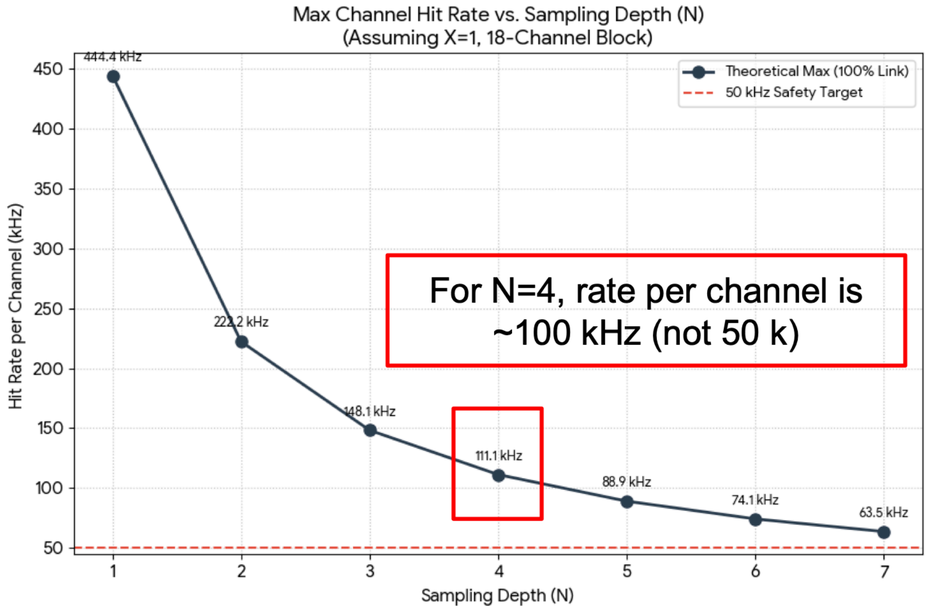
Based on the H2GCROC, using 39.4 MHz sampling

Auto-triggering on the TOA > 0

CALOROC can accept ~ 50 kHz rate per channel (worst case)
Internal HKROC memory writing is without dead time
Hit-rate is only limited by serial link bandwidth (average values above)

There was a follow-up on the ePIC DAQ meeting about the readout speed:

- With 4 samples it looks more like 100 kHZ readout now.



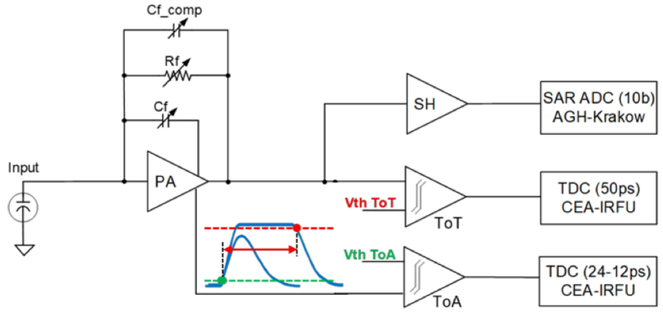
Frederic Dulucq - Omega

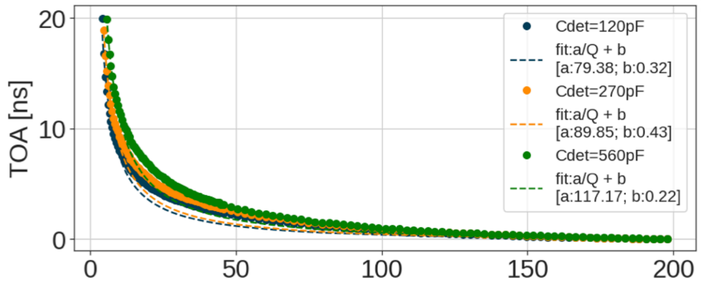
CALOROC1A - same analog part as H2GCROC

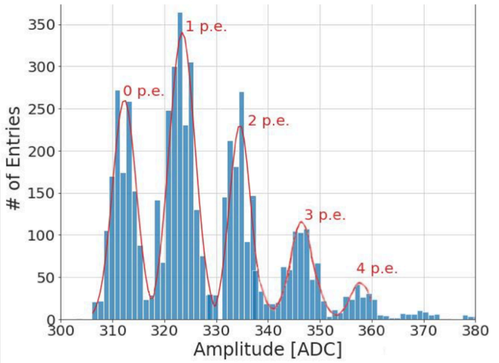
Frederic Dulucq - Omega

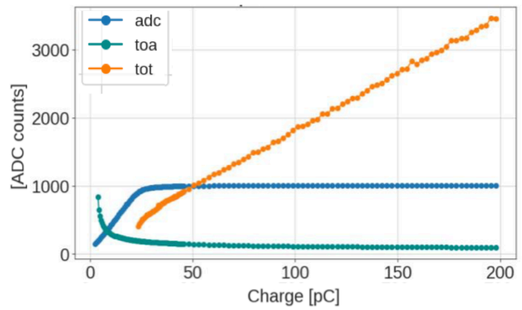
CALOROC1A (based on H2GCROC)

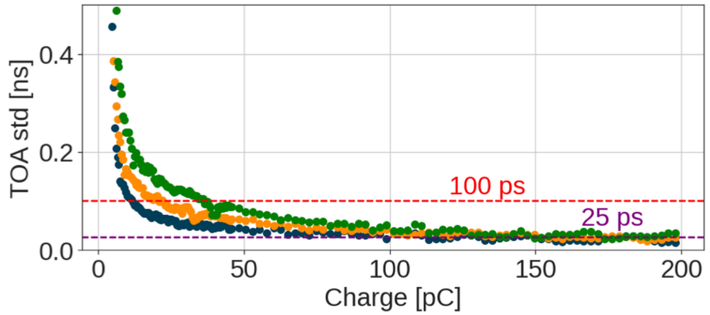
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM range 100-600 pF

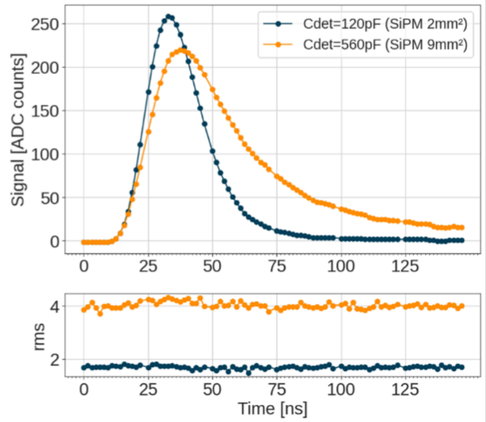












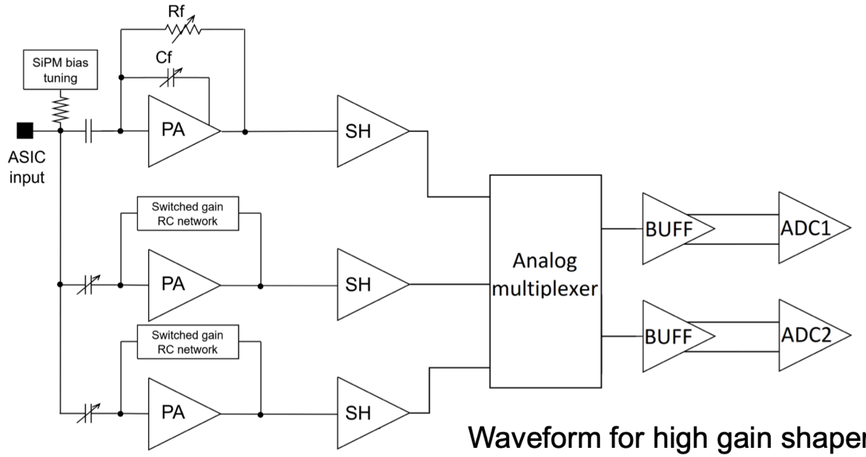
- CALOROC1A will only update its back-end to be EIC compatible

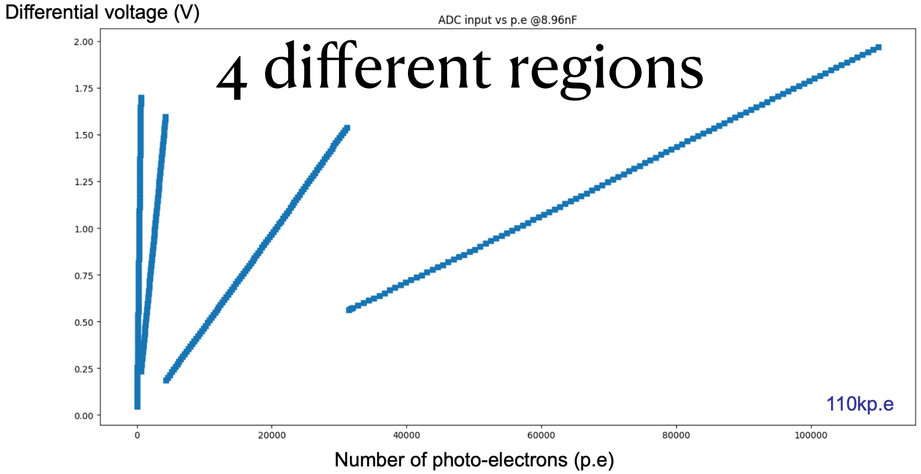
* TWEPP 2023 ➔ https://doi.org/10.1088/1748-0221/19/04/C04005

CALOROC1B - switch gain

CALOROC1B: Channel Architecture

- New dynamic frontend with switched gain:
  - 1 high gain preamplifier
  - 2x low power preamplifier
  - 1 analog multiplexer
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 560 pF to 2.24 – 8.96 nF
  - ~ 10-15 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad

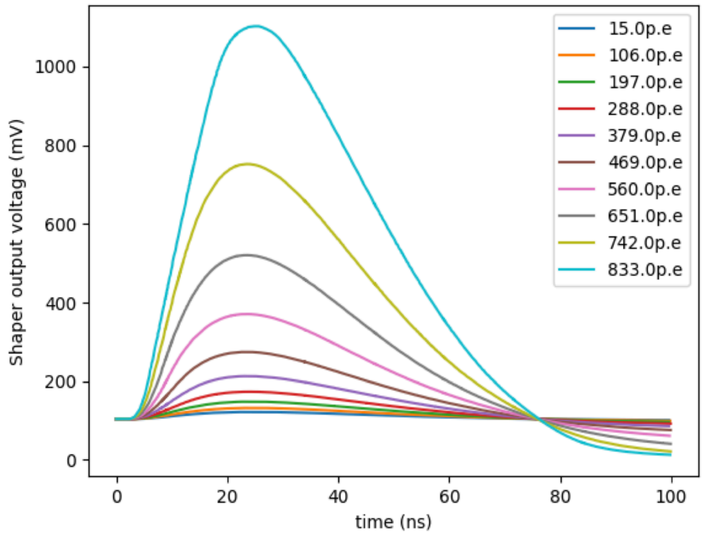




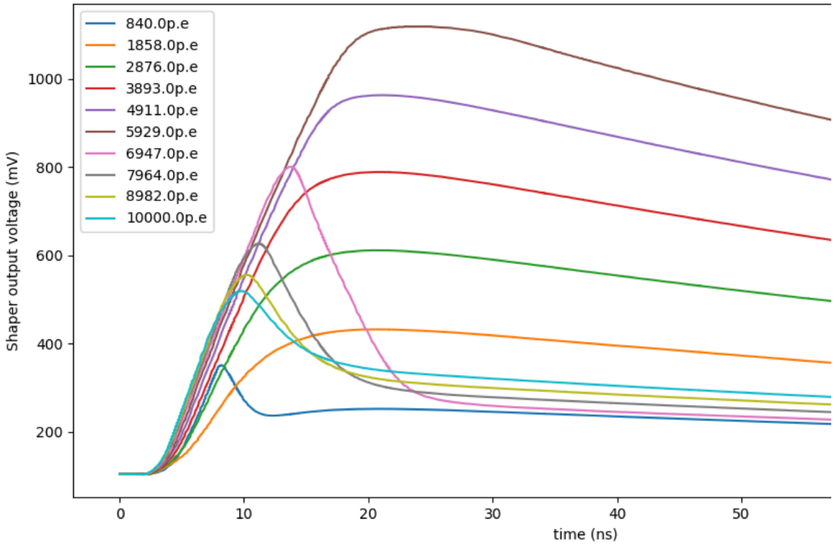
EIC 2026

The switch gain will be adjusting the path according to the incoming signal

Waveform for high gain shaper @8.96nf configuration



Waveform for medium gain shaper @8.96nf configuration



CALOROC Signal to Noise

Operation modes	1 SiPM of 560pF Caloroc1B	4 SiPMs of 560pF Caloroc1B	16 SiPMs of 560pF Caloroc1B	1 SiPM of 560pF Caloroc1A
Cin	560pF	2.24nF	8.96nF	560pF
Dynamic range in charge (Noise - Max)	3.2fC-190pC	11fC-790pC	45fC-3.17nC	20fC-320pC
Input time constant (occupancy related)	112ns	450ns	450ns	10ns
Jitter @ MIP (≈400fC)	42ps	130ps	520ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	9	2.6	0.64	1.44

Frederic Dulucq - Omega

CALOROC readout frames

CALOROC: Readout Frames

Omega

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

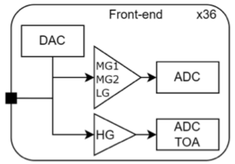
CALOROCA (CMS-like)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map
Tc	Tp	10b ADC-1	10b ADC or TOT (Tc = 1)	10b TOA
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
⋮				
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
CRC				
Idle/Sync Header	28b default IDLE Pattern			

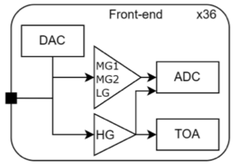
CALOROCB – 2 ADCs or 1 ADC (4 gains)

4b-data Header	2b Mode	Dh Ts	1 - 6b evt counter - 0 - 16b Timestamp	1
4b-hit Header	8b 0	Dh Hm	Dh Ch	18 channels Hit map
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
⋮				
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
CRC				
Idle/Sync Header	28b default IDLE Pattern			

CALOROCB (2 ADCs)

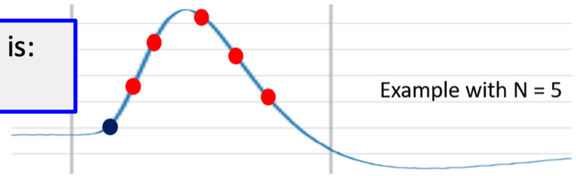


CALOROCB (1 ADCs)



In ZS mode, for X (1-18) hit channels and N samples, number of 32-bit words is:
N x (2Headers + X + 2Trailers)

In characterization mode, forced TcTp, ADC, TOT, TOA for all channels



EIC 2026

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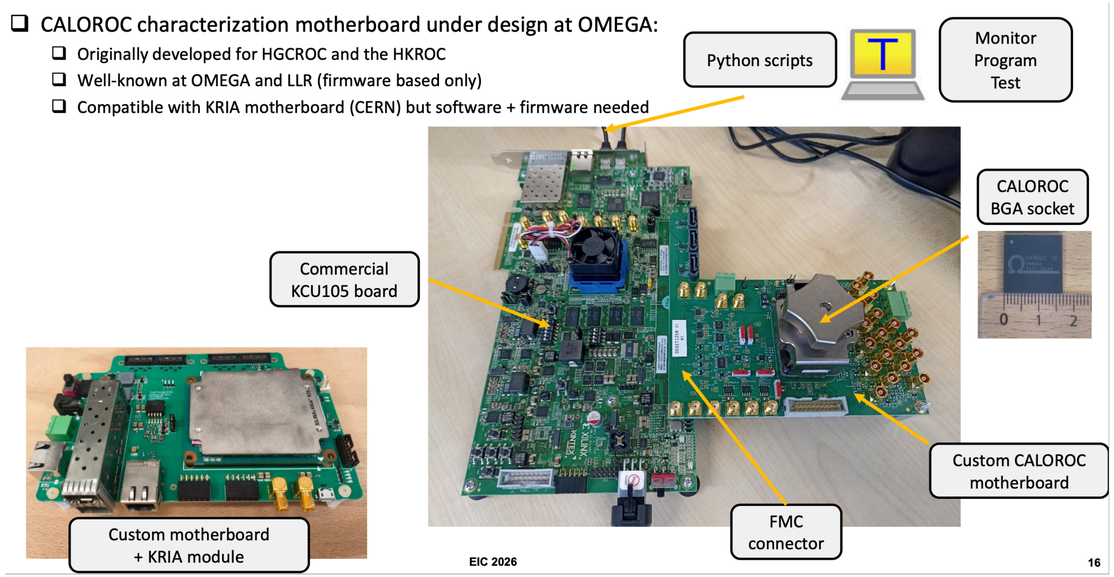
Summary of the readout data obtained from both CALOROCs

- Header with counter
- Hitmap for 18 channels (for the zero suppression)
- Data
- CRC for data integrity check
- Idle (will be suppressed by readout)

Frederic Dulucq - Omega

First tests

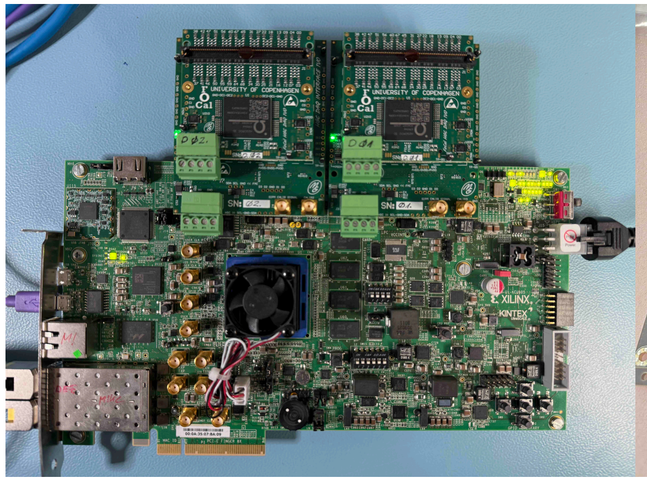


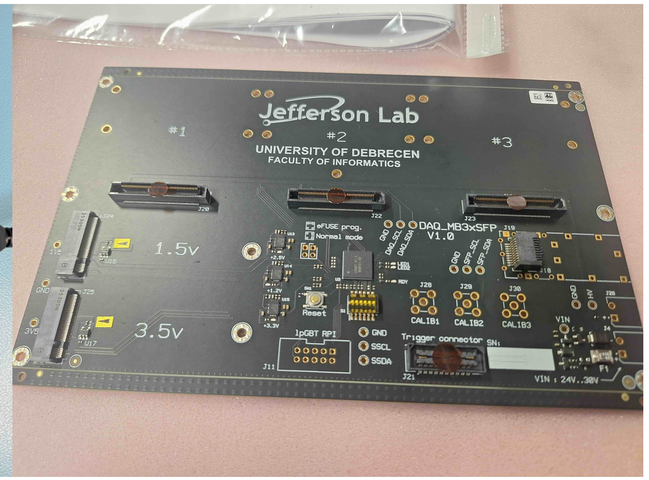
First chip test will be performed at Omega:

- Checking the connections, data stream, etc
- They have the capability from the H2GCROC, this provides the fastest first checks
- Then provide chips for everyone to test

Frederic Dulucq- Omega

For readout plans 2026-2027



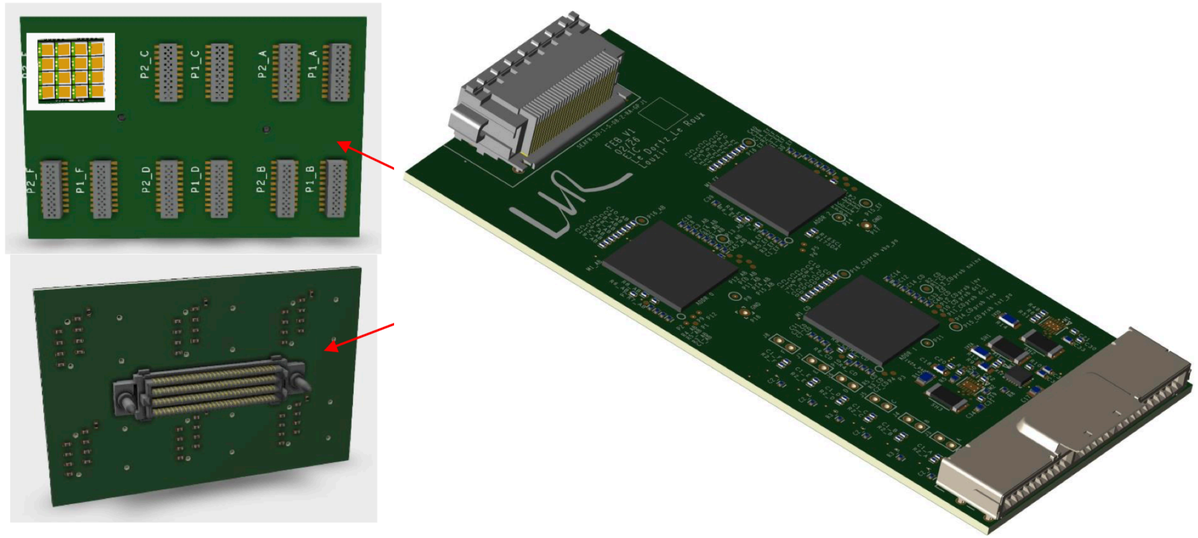


At ORNL (Norbert):

- Option 1 - small scale testing with FPGA board. Currently KCU105, but we will produce the gRDO soon
- Option 2 - first test article for FEB (LpGBT, DCDC), fiber in/out, LV and bias voltage

At LLR (Olivier):

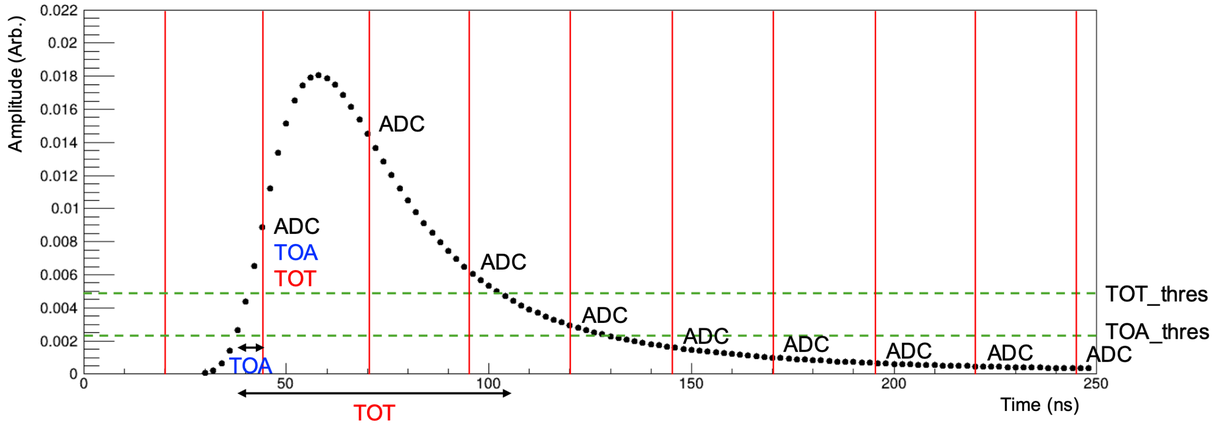
- Special readout electronics for EEEMCal SiPM arrays
- First test article, later it can be upgraded with LpGBT, etc.



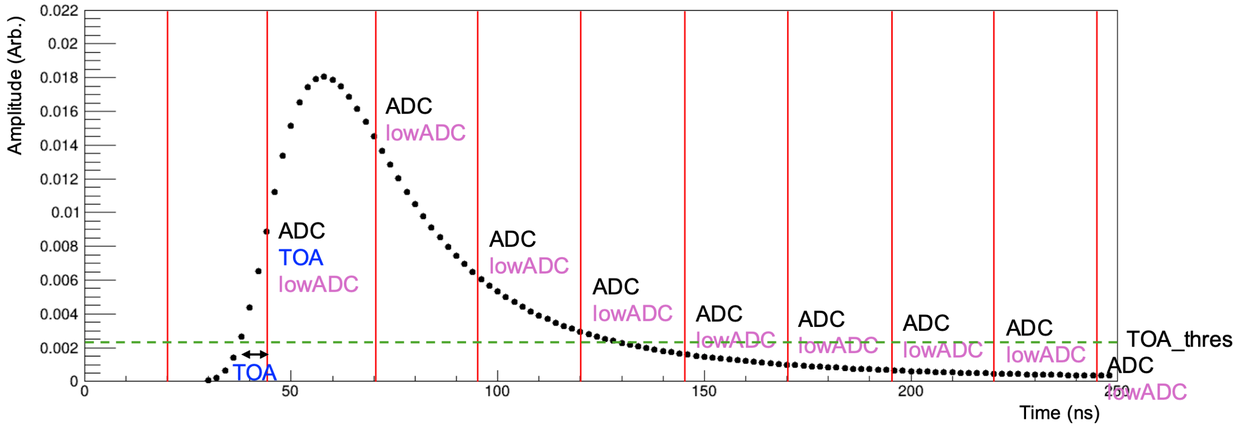
Simulation

Minho Kim

CALOROC A



CALOROC B



Both CALOROCs are implemented in the simulation:

- The switch gain still has to be updated in the CALOROC B, but there is ongoing work
- PR is waiting for approval
- Need to limit the samples up to 7

```
edm4eic::RawCALOROCHit:
  Description: "Raw hit from a CALOROC1A/B chip"

  Members:
    - uint64_t cellID
    - int32_t  samplePhase
    - int32_t  timeStamp
  VectorMembers:
    - edm4eic::CALOROC1ASample aSamples
    - edm4eic::CALOROC1BSample bSamples
```

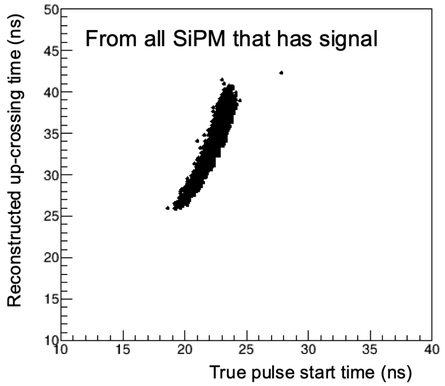
```
edm4eic::CALOROC1ASample:
  Members:
    - uint16_t ADC
    - uint16_t timeOfArrival
    - uint16_t timeOverThreshold

edm4eic::CALOROC1BSample:
  Members:
    - uint16_t lowGainADC
    - uint16_t highGainADC
    - uint16_t timeOfArrival
```

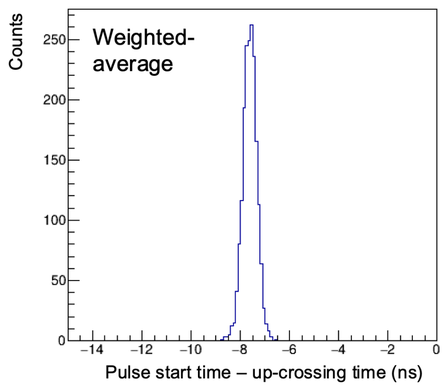
Simulation checks

Sanity checks (TOA)

5 GeV γ at η = 0

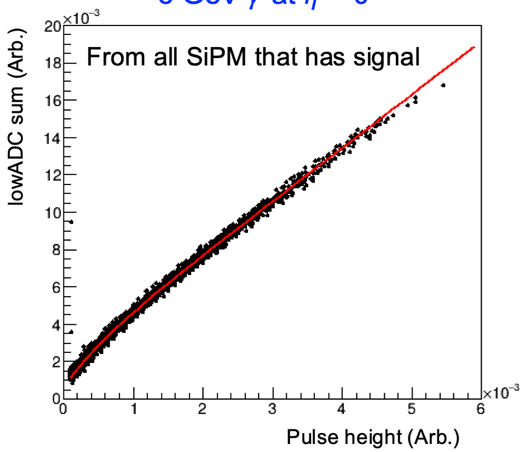


5 GeV γ at η = 0

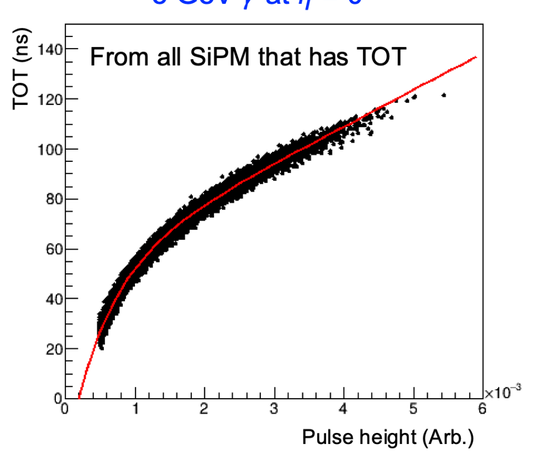


Sanity checks (ADC & TOT)

5 GeV γ at η = 0



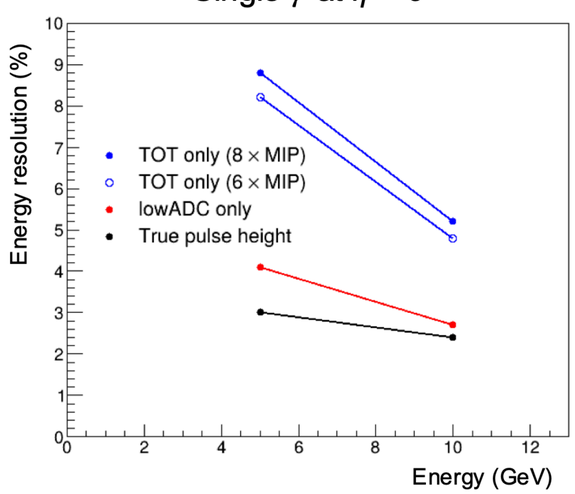
5 GeV γ at η = 0



Sanity checks for the ADC, TOA, TOT done

More studies are coming

Single γ at η = 0



Update request from detectors

1. What is the capacitance of the detector per channel? (pF)
2. What is the lowest signal measurement required? (fC)
3. What is the highest signal measurement required? (fC)
4. Do you have a measurement with certain settings of MIP peak, other fixed signal? (With the H2GCROC and settings)
5. What is the charge resolution requirements? (Percentage as a function of charge, not in bits)
6. What is your timing requirements/measurements?
7. What is the expected occupancy per channel from simulation? (Including full background)
8. What is the maximum hit rate per channels needed if all channels are activated at the same time?
9. What is the expected dark noise rate?
10. What is the maximum hit rate required for a single channel? (If only one receives signal)
11. What is the double pulse separation needed? Overlap signals from two independent bunch crossings? (This affects small or large signals differently in your detector?)
12. How many number of samples you require as minimum (max is 7 now in CALOROC)?
13. What is the preference for A or B for CALOROC?

What we received

Understood req.
Progress, but not finished
Nothing to report
Maybe too large requirements

	BackHCal	BackECal	BarHcal	BarEcal	ForEcal	ForHCal	B0	ZDC	Insert	Lumi Pair	Low-Q2	LumiPhot
1												
2												
3												
4												
5												
6												
7												
8												
9												
10												
11												
12												
13												
(14)												
(15)												

Summary

- First CALOROC chips will be available in March:
  - First tests basic communication, performance at Omega
  - Prepare readout electronics for all detectors and laboratories (small and large)
- Simulation implementation of the digitization is ongoing
- New request for the calorimeters to update the requirements and performances using the chip:
  - Most of the answers lies in simulation, some in testing of the chip
  - Vision is to write a document by the end of the year, before the CALOROC-2 is sent for production