Inner MPGD CyMBaL Status

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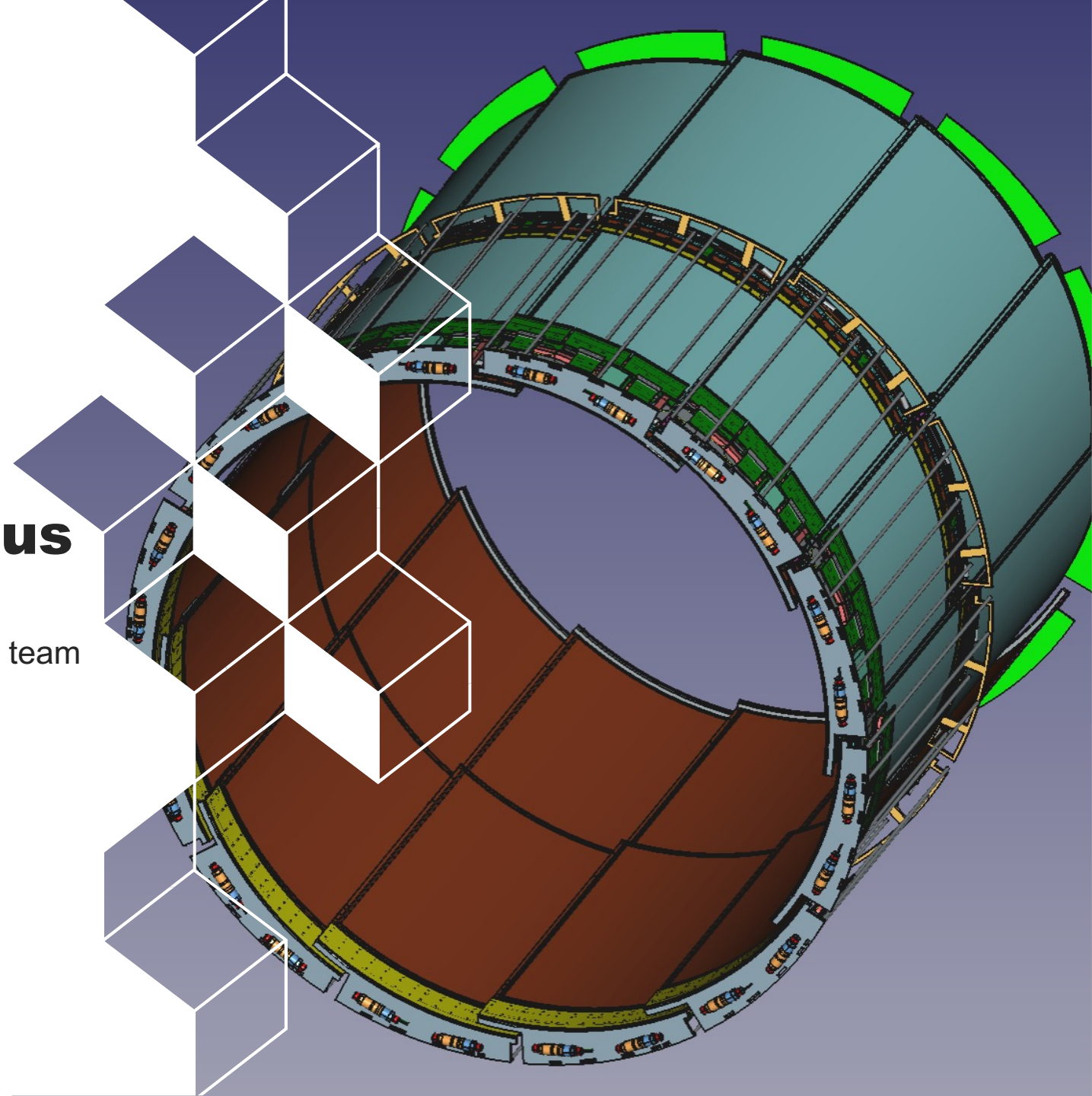
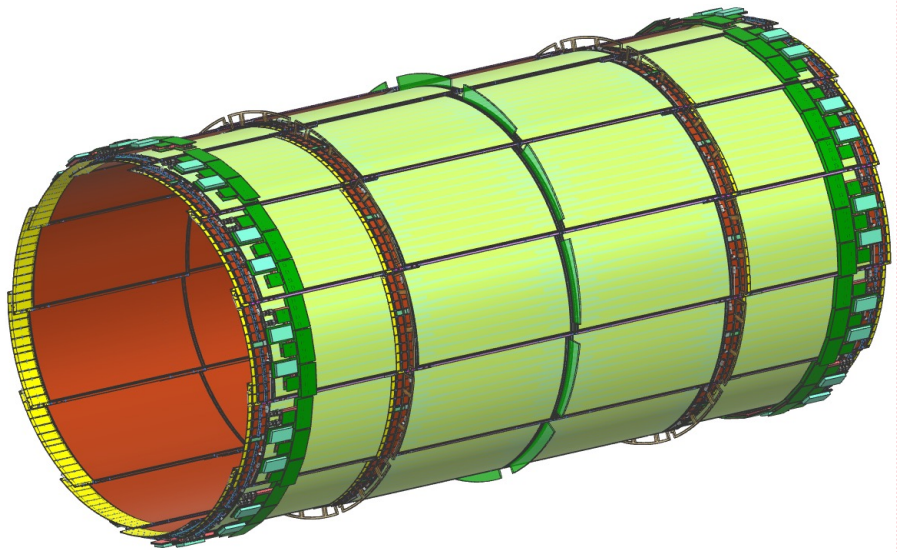


EIC/EPIC 3I meeting, 23 February 2026

CyMBaL tiles integration & test article design

CyMBaL: Current design



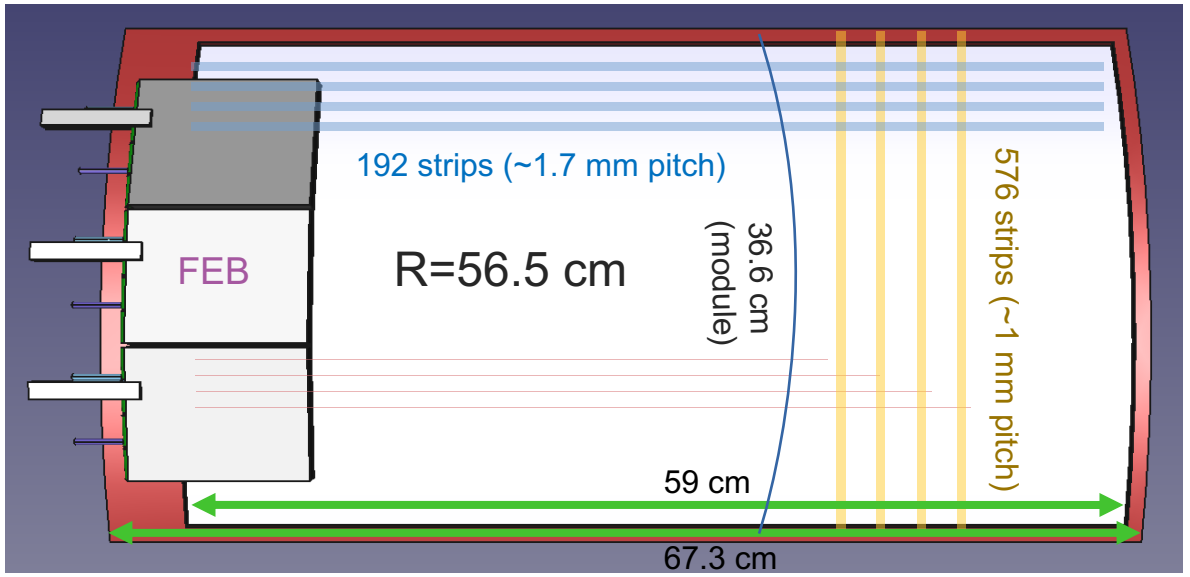
Services
via patch panel(s)

- 3 OF (to DAM)
- 5 HV cables
- 3 LV cables (1 tile)
- Gas I/O (2 tiles)
- FEB cooling I/O

2 tiles – 6 FEBs+DC/DC

few l/min of 18°C water

Design of a tile / **test article** (Cylindrical)



48 tiles: 12 in ϕ × 4 in z (integration in GST in "fish scale")

- R_{min} = 55.5 cm; R_{max} = 61.5 cm
- Overlaps in ϕ and in z for hermeticity (~2-4 cm)
- 768 readout channels/tile
- **36K readout channels in 3 FEBs/tile**

Module dimensions

Z = 673 mm / R*phi = 366 mm

Active zone dimensions

Z = 590 mm / R*phi = 340 mm

Weigh estimates

~1 kg / tile + ~0,6 kg / FEB

Expected performances

- Spatial resolution: < 300 (500) µm in Z (r*phi)
- Time resolution ~20ns
- Efficiency ≥ 98%
- Material budget ~0.5% X0

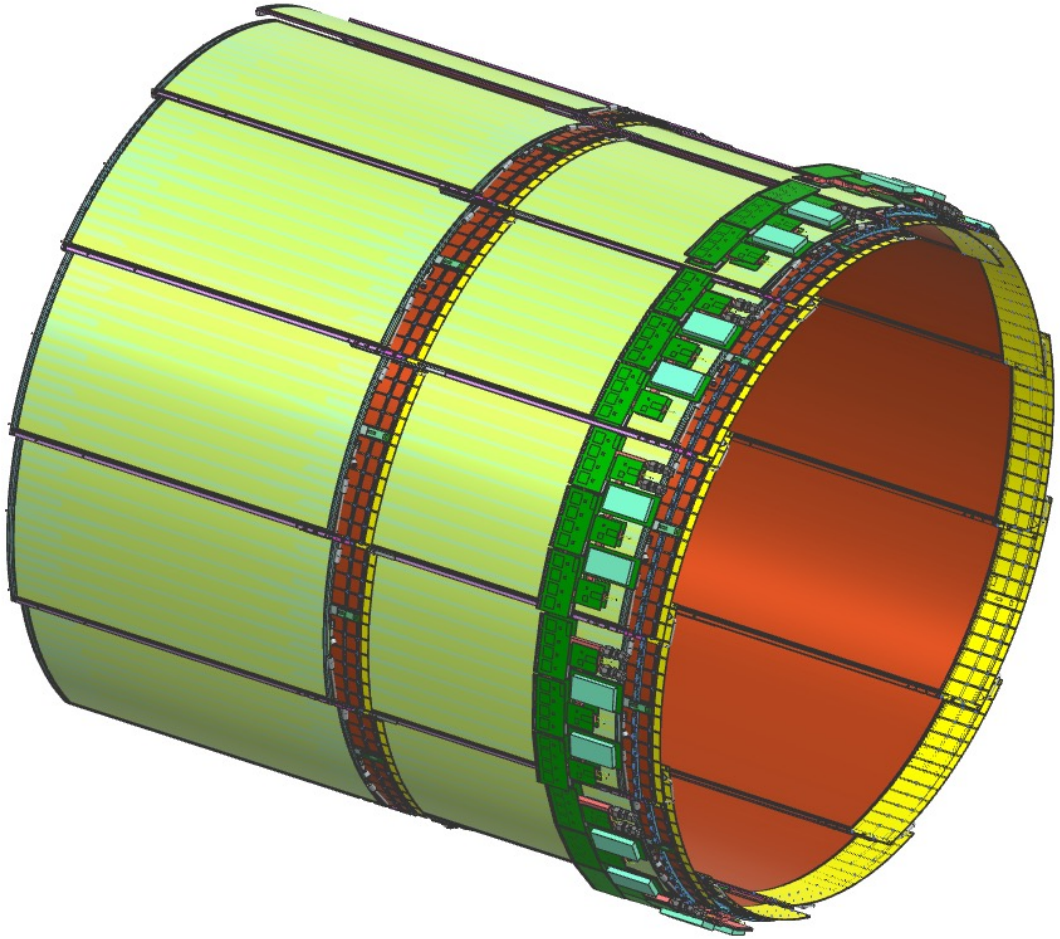
18-20°C water cooling for the CyMBaL Front-End currently estimated to 48 W / Tile (2300 W total for CyMBaL)

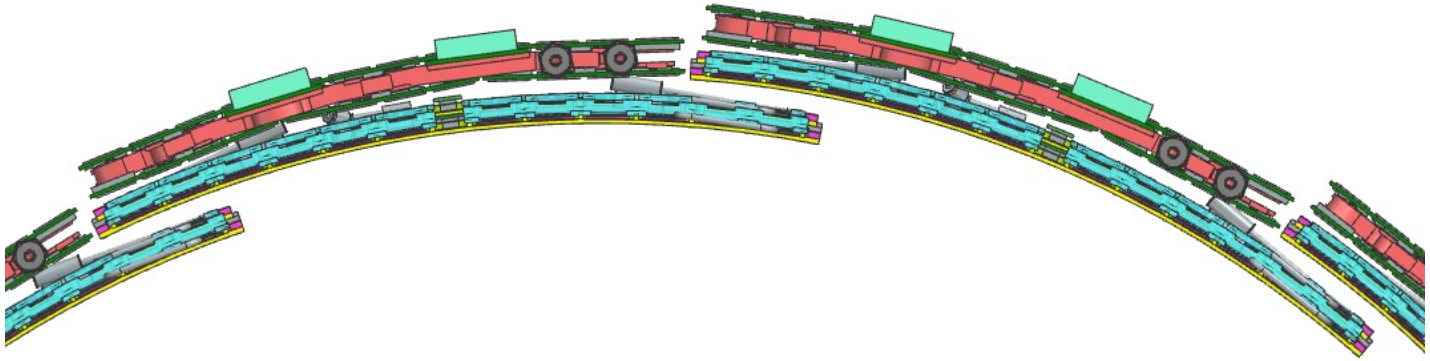
CyMBaL scale 1 test article : « GEICO#0 »

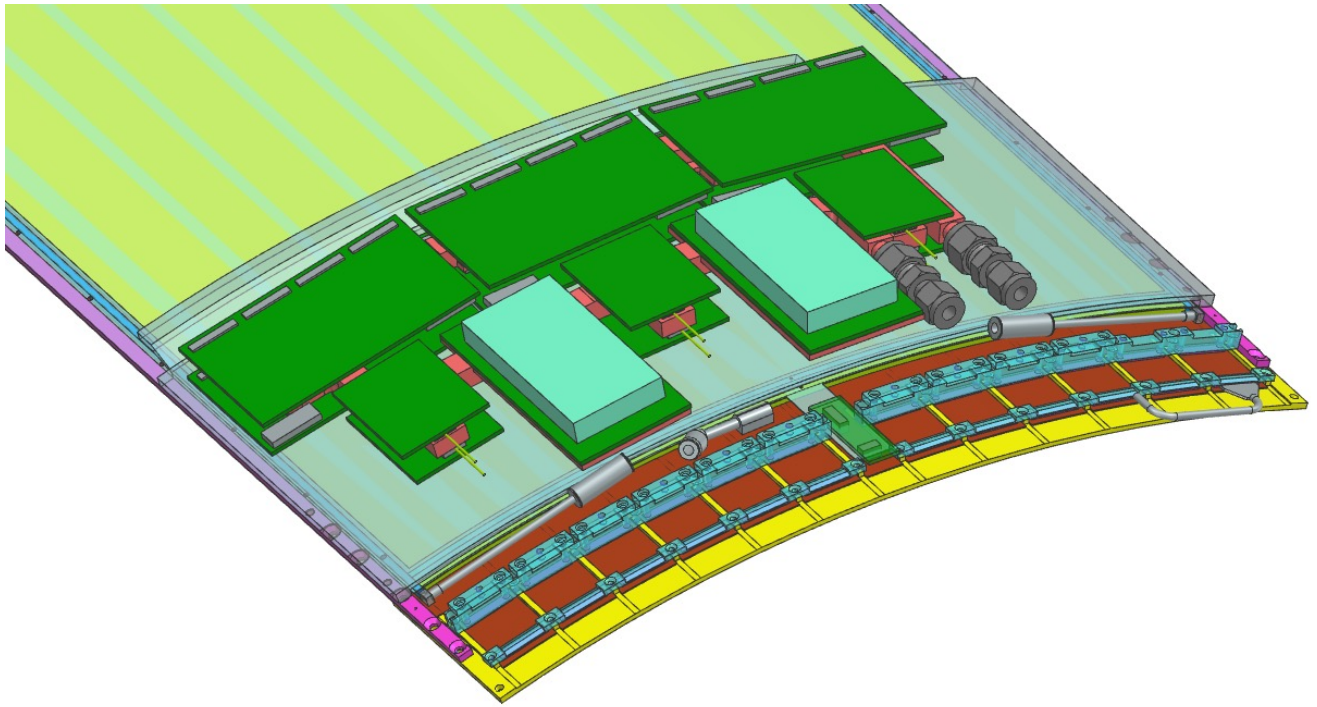
The design of the CyMBaL barrel, composed of 2 half-barrels made of 12 modules of 2 CyMBaL tiles, is well advanced and used to produce a first scale 1 CyMBaL tile (called “GEICO#0”) which includes most of the design inputs currently known for the final CyMBaL :

- The half-barrel design copes with the allocated CyMBaL envelop of 555<R(mm)<615 & -1025<z(mm)<+1450 with a “fish scale” arrangement of 24 identical tiles (R=565 mm) with overlaps of the tiles in z & Phi for a full coverage of the active areas, but with a dead area between the 2 half-barrels (support ring thickness + 2 times the tile inactive borders of 13 mm).
- The current preliminary design of the Front-End readout electronics of a module composed of 2x3 Front-End Boards (FEBs) and DC/DC converter card(s) (PowerBoard) water-cooled through a common heat-sink plate, linked to the Micromegas PCB with 32 ch. KEL USLS20 cable harness. The prototype will be readout with DREAM electronics using Mech-8 to KEL adapters.
- Since there is still no concept on how to attach CyMBaL to TOF and the GST, the design of GEICO#0 does not include this interface which will probably be implemented in a future final design of a CyMBaL tile with holes/threads in the “mechanical” longerons of the tiles.

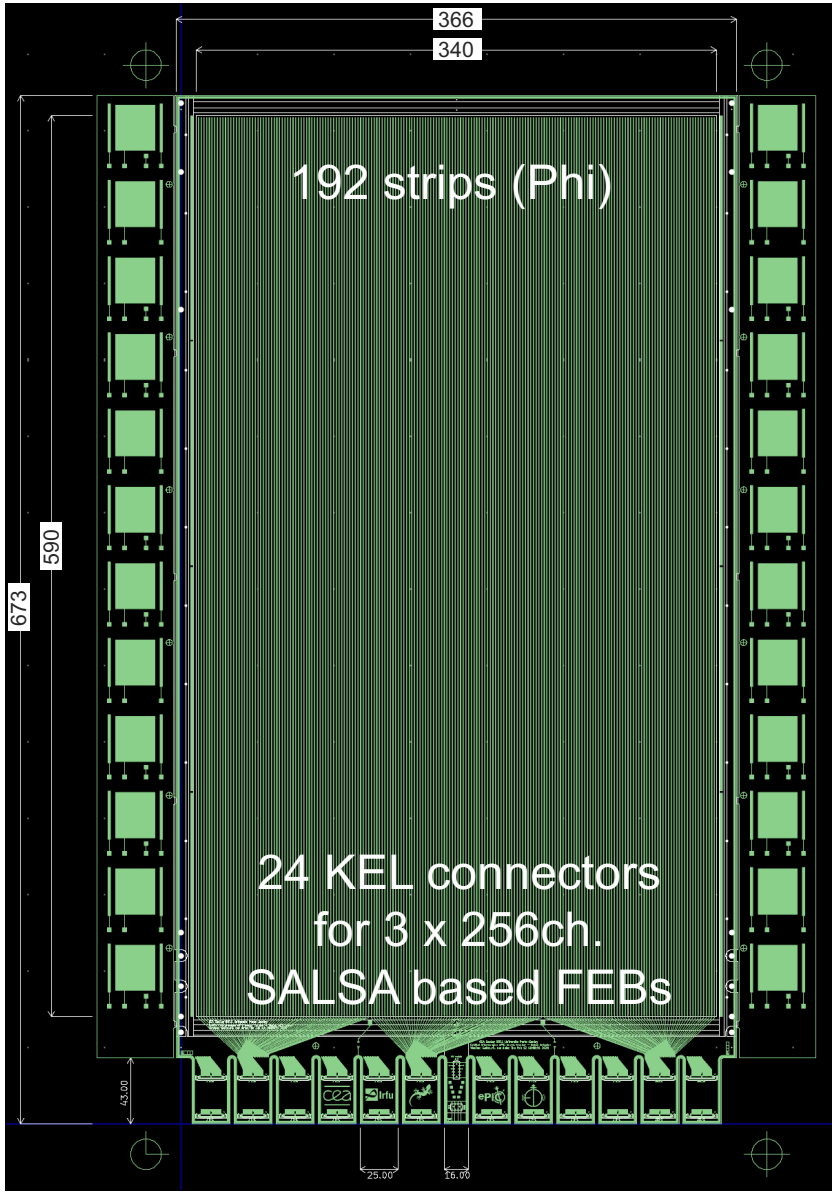
Status of CyMBaL design used for production of a scale 1 test article

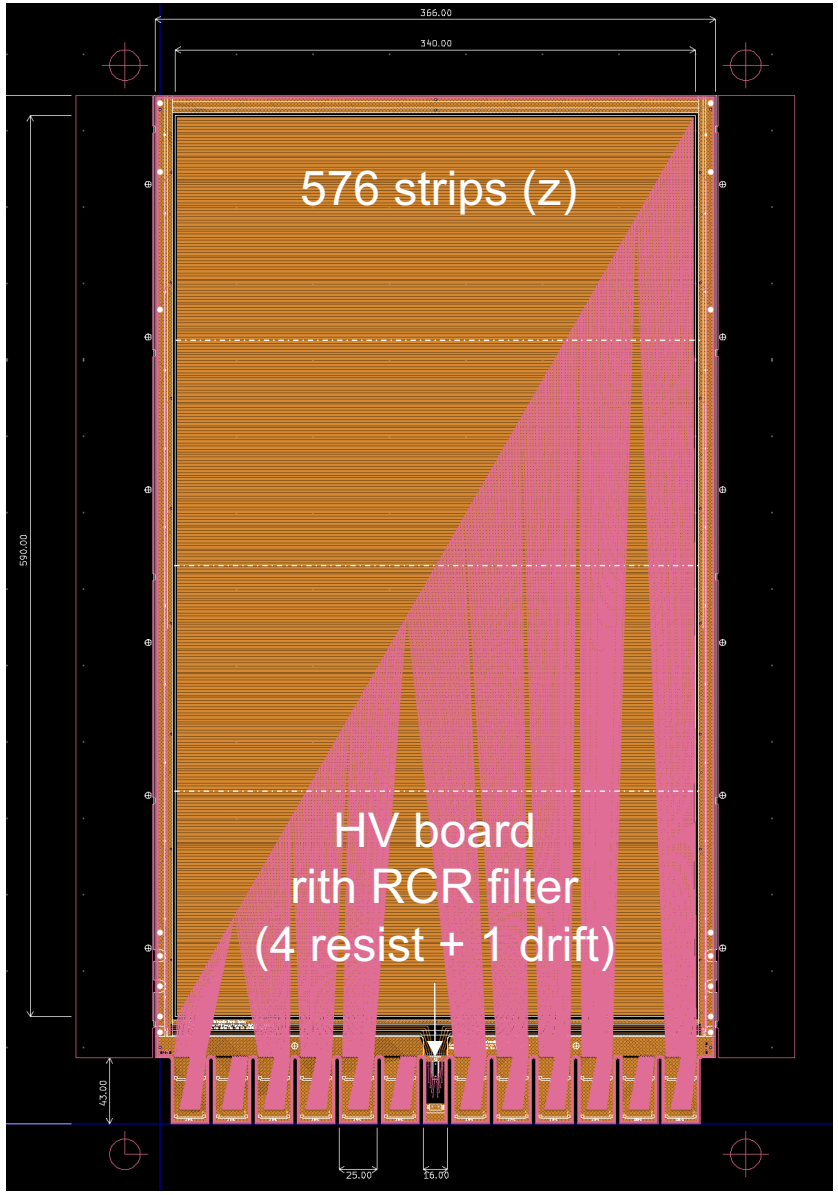






CyMBaL « GEICO#0 » : Micromegas (Version 4)

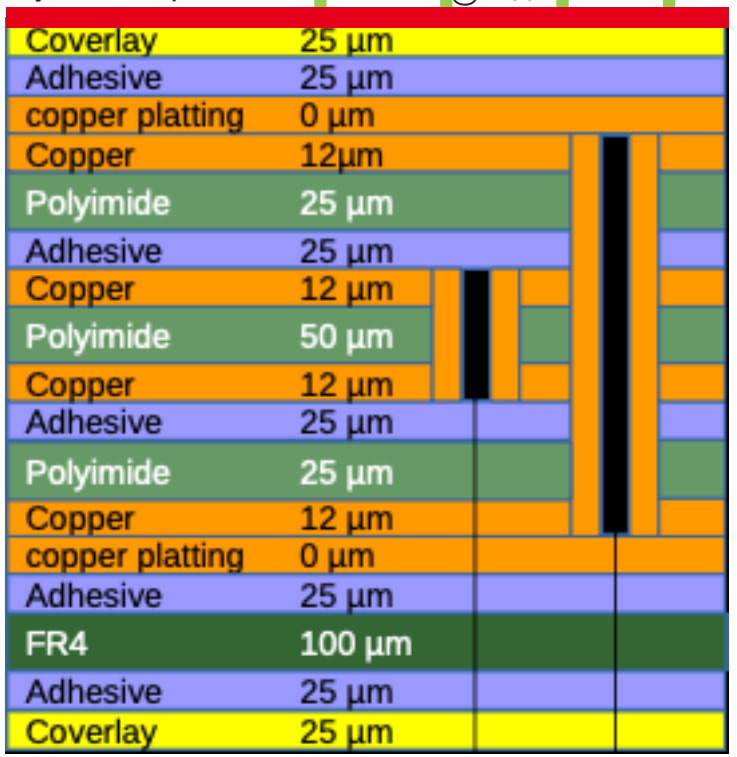




Drift cathode @ 3mm above MM mesh & ~-1 kV

MM mesh @ GND

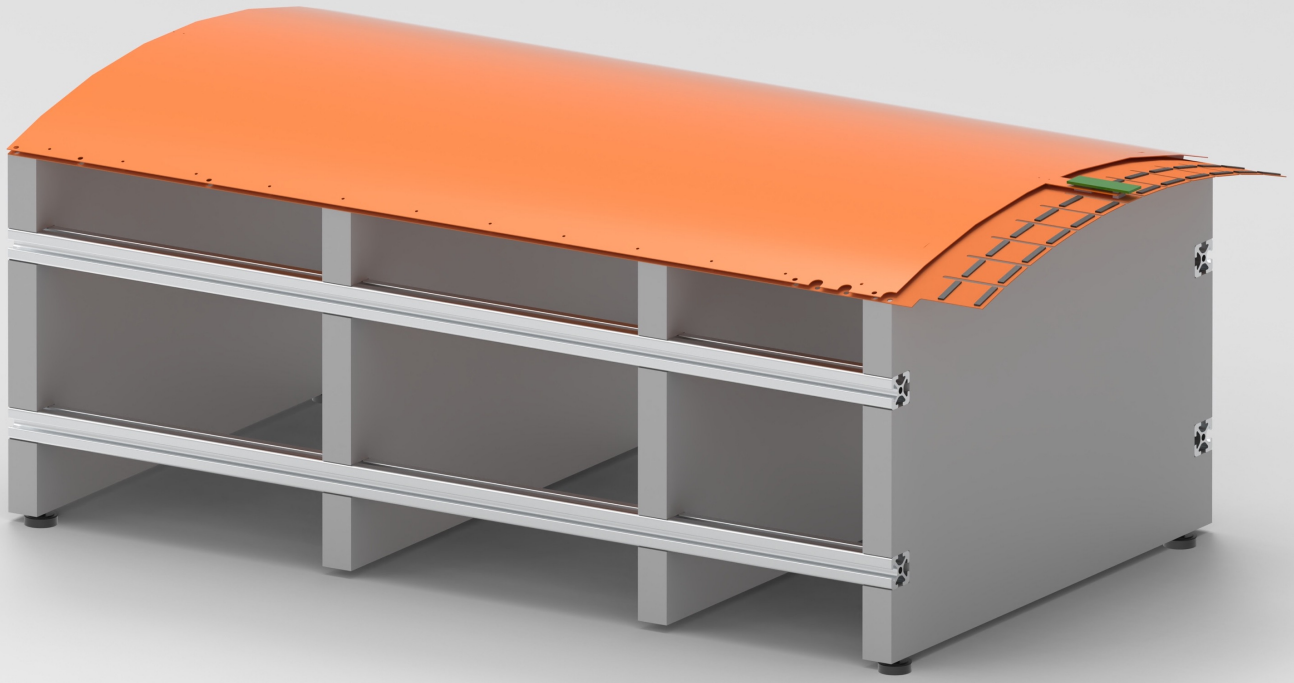
Dynamask pillars @~450V



~300 µm total PCB thickness

CyMBaL tile assembly

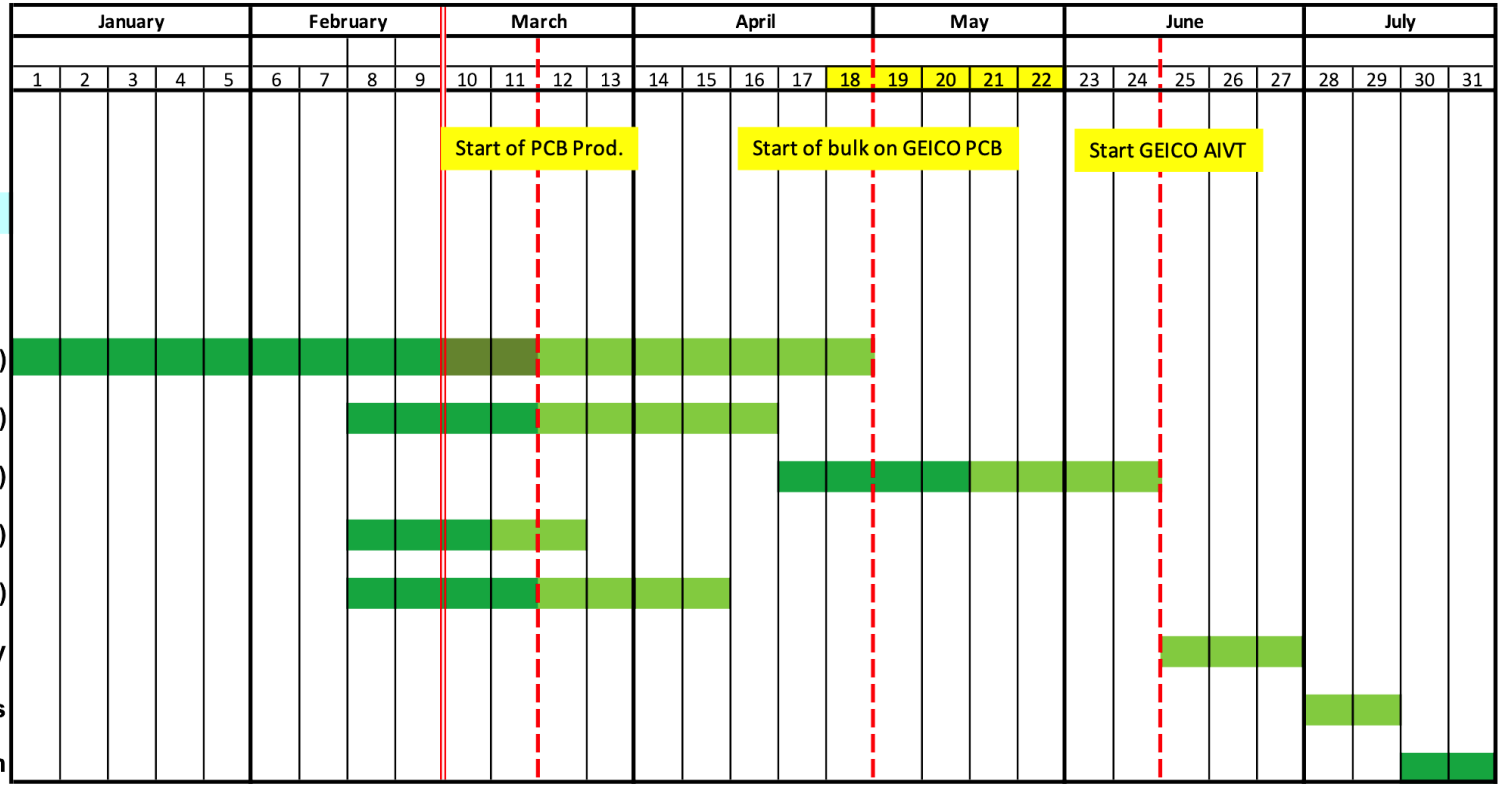
Cylindrical tile assembly tool



- **Micromegas production (in MPGD lab)**
  - Resistive layer serigraphy on PCB
  - Mesh integration in bulk-micromegas
  - QC with HV in air
- **Flat tile (in clean room)**
  - KEL connectors & HV filter soldering
  - Gluing of the 4 longerons using the “flat tile” tooling setup
- **Cylindrical tile (in clean room)**
  - Gluing of the 4 hoops using the “cylindrical tile” tooling setup
  - Gluing of the drift electrode
  - Gas leak QC
- **CyMBaL tile final QC & tests**
  - ^{55}Fe spectrum
  - Uniformity of efficiency with Cosmics

« GEICO#0 » production & AIVT timeline

The goal is to have GEICO#0 ready for the test beam at CERN/SPS w30-31 (**mid-July !**)

16 february 2026 V1.1

PBS#/WBS	ITEM
1 3000	CyMBaL Module Prototype (GEICO#0)
	Management (Manpower availabilities/Milestones)
	PCB (Design/order/production)
	Tile assembly toolings (design-production)
	Bulk MM (Trials on "mechanical PCBs" & final GEICO#0)
	Cathode (design-production)
	Mechanicals (design-production)
	GEICO#0 assembly
	GEICO#0 lab tests
	CERN/SPS DRD1 test beam