AC-LGAD LV power distribution PBv1 & receiver board RBv1 status: efforts from BNL

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LV Power Board – Overall Status Update

Tim Camarda, Prithwish Tribedy

Electrical & Thermal Performance (Measured)

Hardware Status

- 3 prototype boards assembled

- Boards fully populated and test ongoing

- BPOL-V48 based design with LC filtering

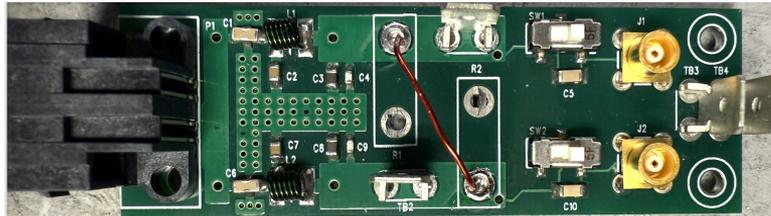- External filter board used for optimization

- **Input Voltage:** ~14 V
- **Output Voltage:** ~1.2 V
- **Output Current:** up to 8–10 A per channel
- **Tested Load:** ~22 W (≈80% of full load)
- **Efficiency:** ~70%
- **Ripple (after filter, 25 MHz BW):** ~1.7 mVpp
- **Heat Sink Temp:** ~38 °C (with fan)
- **BPOL Internal Temp:** ~46 °C

System Testing (so far)
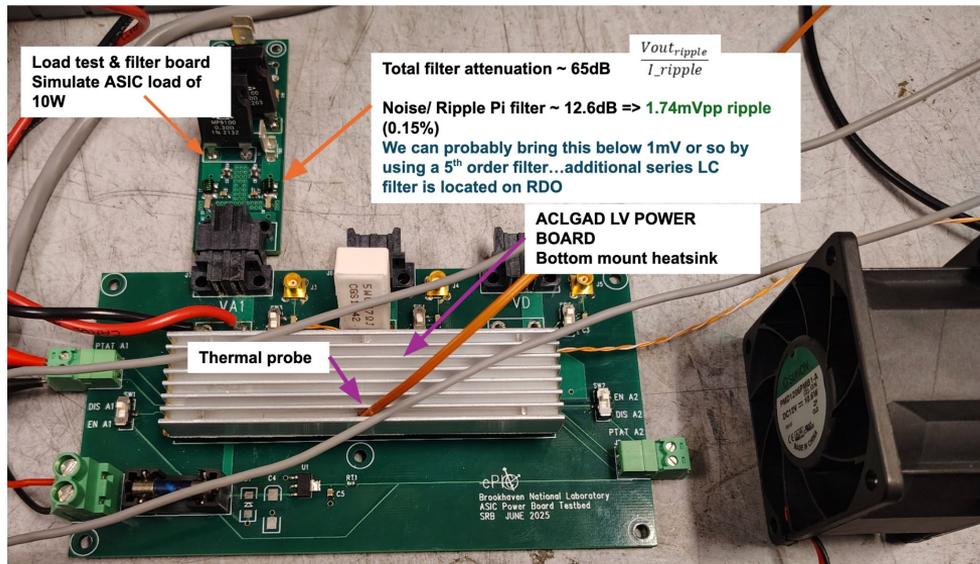
- Static and dynamic load
- Ripple and EMI

PBv1

External load & filter board

Testing with receiver board (RBv1) in progress

30W PBv1 Load, Thermal & Noise Testing

Load test & filter board Simulate ASIC load of 10W

Total filter attenuation ~ 65dB

$$\frac{Vout_{ripple}}{I\_ripple}$$

Noise/ Ripple Pi filter ~ 12.6dB => **1.74mVpp ripple** (0.15%)
We can probably bring this below 1mV or so by using a 5th order filter…additional series LC filter is located on RDO

ACLGAD LV POWER BOARD
Bottom mount heatsink

Thermal probe

Brookhaven National Laboratory
ASIC Power Board Testbed
SRB JUNE 2025

Noise/ Ripple measure pre-filter stage

Noise/ Ripple measure post-filter stage -12.5dB

LOAD & THERMAL TESTING

The test setup was then configured for ~80% load test at **22.32W** (*exact configuration not shown in picture here*)

NOTE: Full Load testing for 30W will be available soon…

CH1A = 1.2V, 8A = 9.6W
CH1A = 1.2V, 8A = 9.6W
CH1A = 1.2V, 2.6A = 3.12W

After 1 hour:
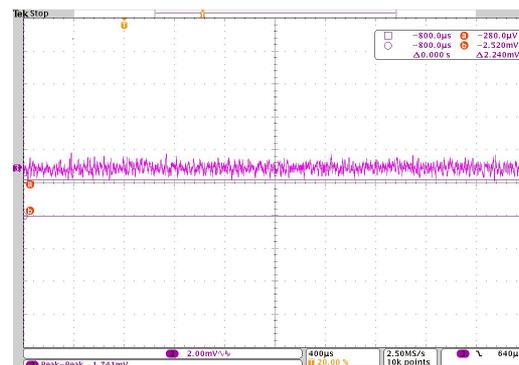Heat Sink w/ small fan: **38°C**
PTAT (bPOL48 internal): **46°C**
Board to connector loss ~2.5% (30mV) @ 8A

Power Efficiency => P_{IN} / P_{OUT} ~ **70%**

Integrating with RBv1+AXAU15 setup at BNL

- PBv1 connected to RBv1 and AXAU15
- Bench test setup completed
- Todo: Optical connection + FMC links

- AXAU15 powered (LEDs, fan OK)
- Ethernet + USB-UART + USB-JTAG connected
- Devices detected (UART, JTAG)
- Serial console verified

PBv1

RBv1
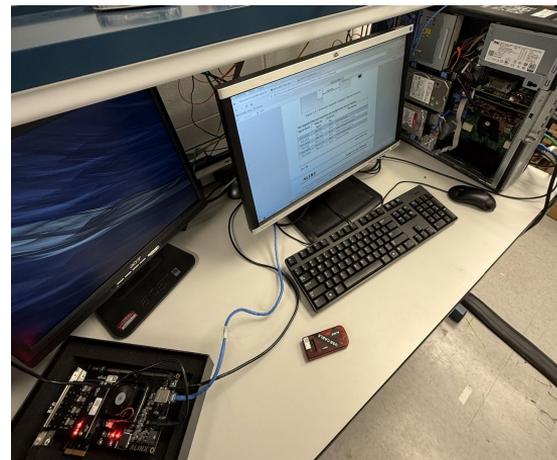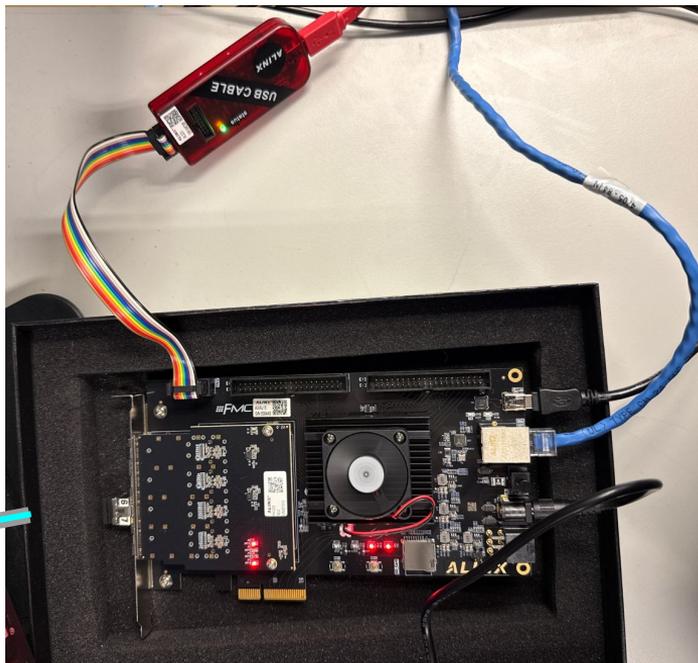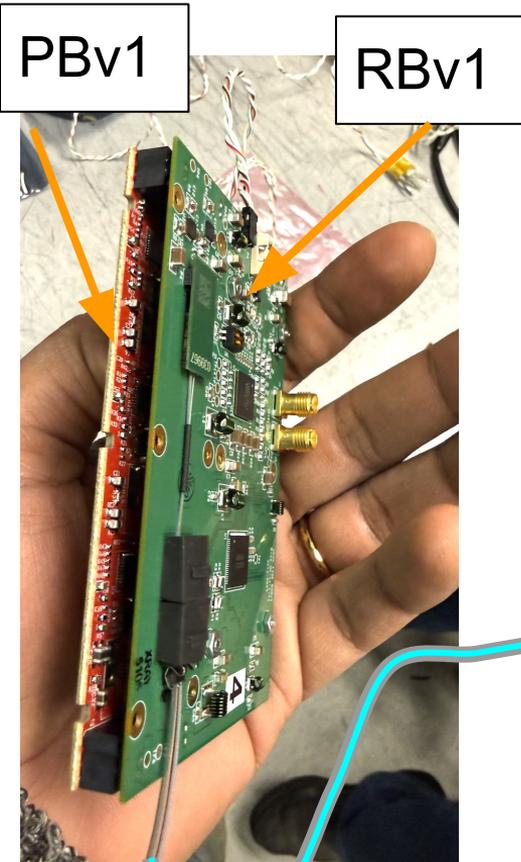
> Hardware integration complete
> Interfaces verified
> Ready for FPGA programming

Summary

Brookhaven National Laboratory   ePIC

Power Board (PBv1) Status

- 3 boards fabricated; 2 tested, 1 remaining (few tests left)
- Overall testing results look very good:
  - Thermal: ~80% load with small heatsink + fan → <40 °C after 1 hr
  - bPOL48 internal temperature <50 °C (within spec)
  - GaN FET temperature: pending
  - Noise/Ripple acceptable; may increase RDO filter order for <1 mV target
  - Near-field EMI looks good
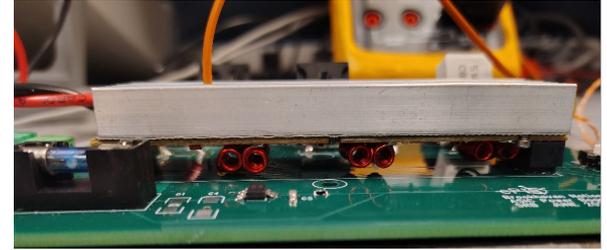
power board side view plugged into test load PCB

Readout Board (RBv1) / DAQ Integration at BNL

- AXAU15 powered and operational (LEDs/fan OK)
- Ethernet, USB-UART, USB-JTAG connected and verified
- CP210x (UART) and FTDI (JTAG) detected via lsusb
- Serial console tested (no output expected without firmware)
- No IP configured on Ethernet (as expected)
- System ready for FPGA programming and remote access

Remaining Tasks

- Full load testing (~30 W)
- Stability/transient testing with dynamic load (preliminary done)
- Ruggedness / reliability testing (power cycling, long-term heat run)
- Long Vin cable test
- Thermal map with a camera
- FGPA installation with Tonko