AstroPix5 Design

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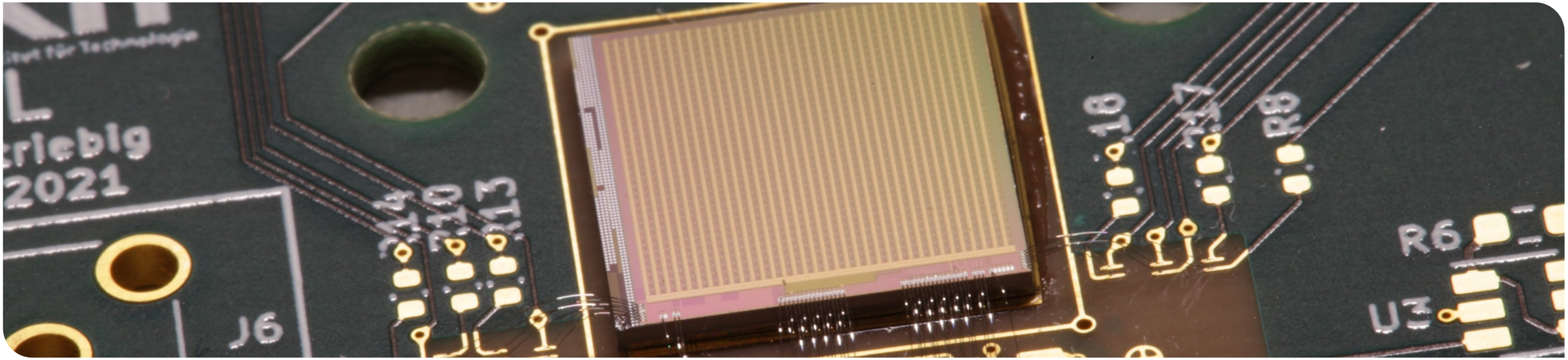


AstroPix Development Overview

AstroPix1 (2020)

- 5 mm × 5 mm
- SPI
- Breakdown: 120 V
- Pixelsize: 175 x 175 um2

AstroPix2 (2021)

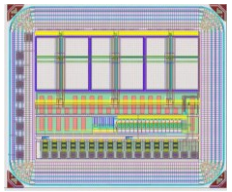
- 1 cm × 1 cm
- QSPI Daisy chain
- Breakdown: 190 V
- Pixelsize: 250 x 250 um2

AstroPix3 (2022)

- 1.9 cm x 2 cm
- Voltage DACs
- Breakdown: 350 V

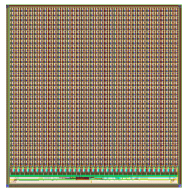
AstroPix4 (2023)

- 1 cm x 1 cm
- DLL stabilized per-pixel TDC
- PLL
- Improved SNR
- TuneDACs



LF-AstroPix (2024)

- 3 mm × 4 mm
- 4 kOhm-cm Cz substrate
- Analogue Testchip



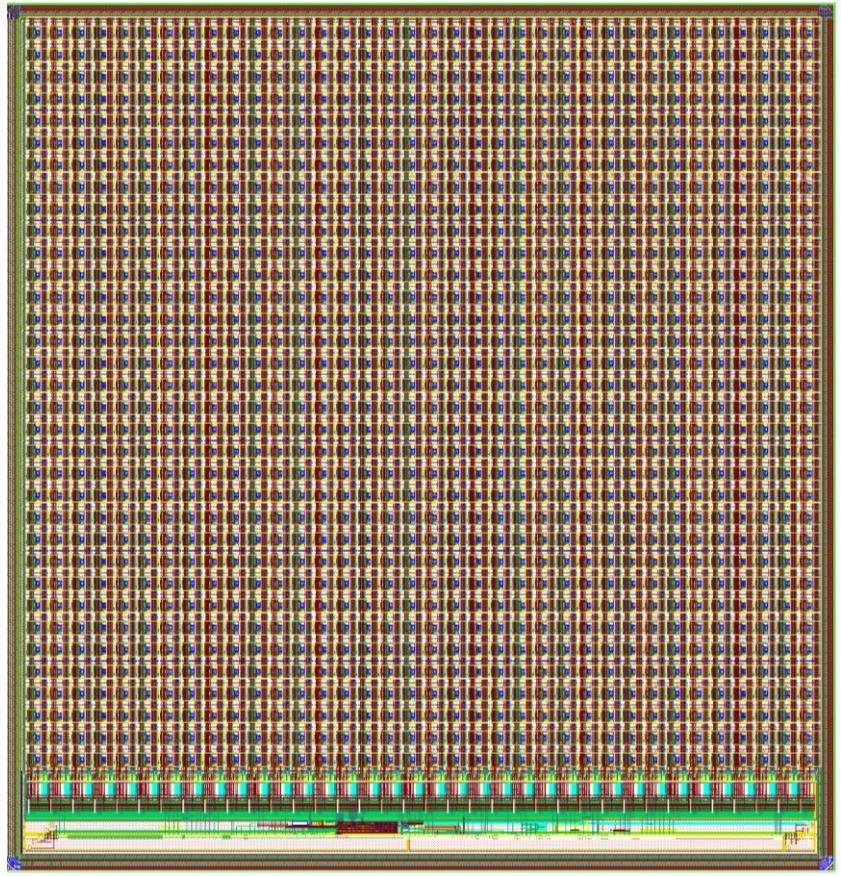
AstroPix5 (Est. 2025)

- 1.9 cm x 2 cm
- Improved dynamic range pixels
- Reduced pixel capacitance
- Monitoring ADC
- Expected breakdown: 500 V
- 2kOhm-cm Cz substrate

AstroPix5 Key Specifications

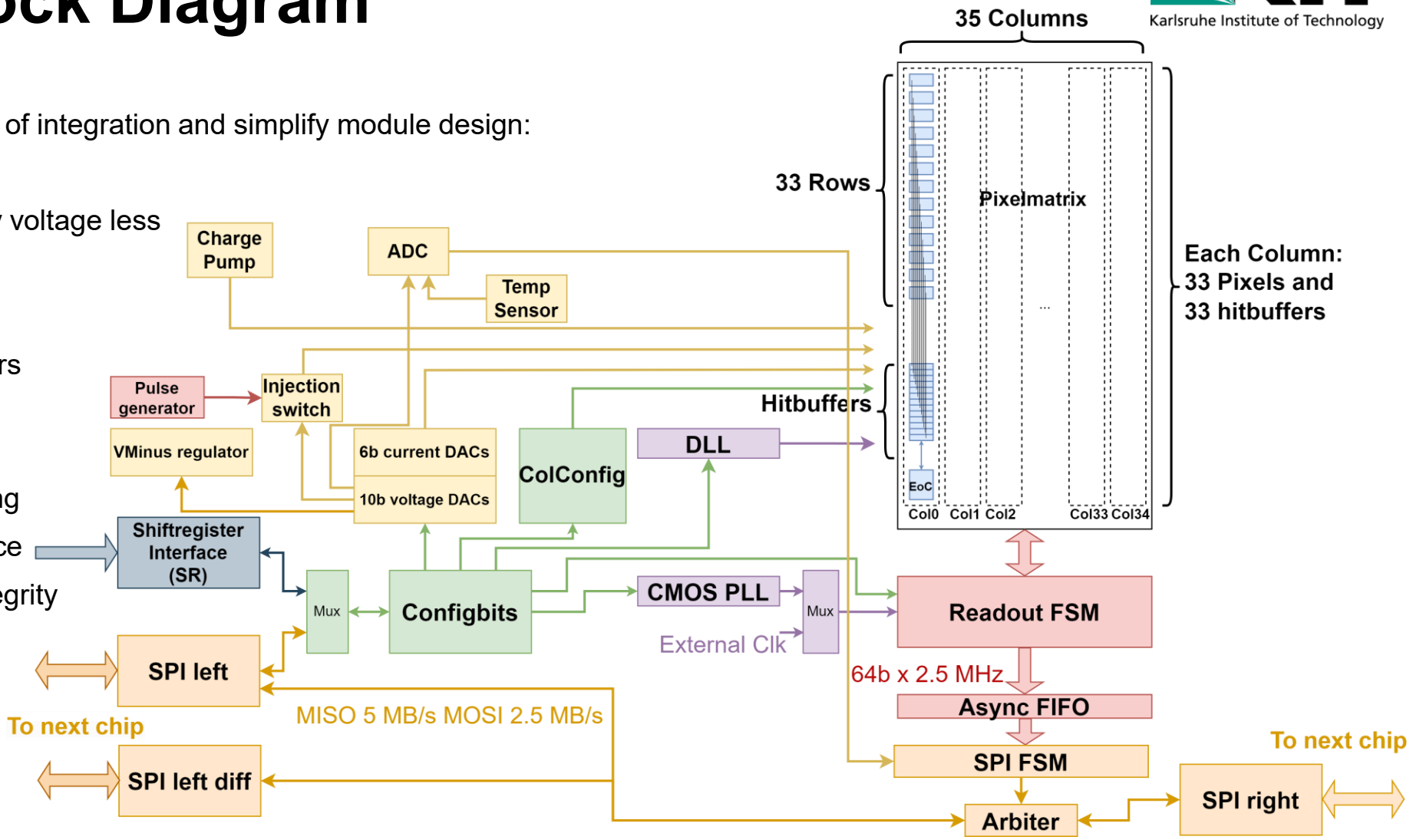
- Process
  - „New/old“ AMS ah18 180nm after TSI 180nm discontinuation
  - TSI compatible but only 6 Metal Layers
    and no deep p-well option

- Engineering run
- Design ready for submission
- 18610 um x 19485 um similar to AstroPix3
- 36 x 34 pixels
- 2 Wafer resistivities: 200 – 400 and 600 – 2kOhm-cm Cz
- Columns:
  - 32 Columns with Standard NMOS Comparator
  - 2 Columns with dynamic Feedback
  - 1 Column with NMOS Comparator and Resistor Load
  - 1 Column with NMOS Comparator and PMOS Load



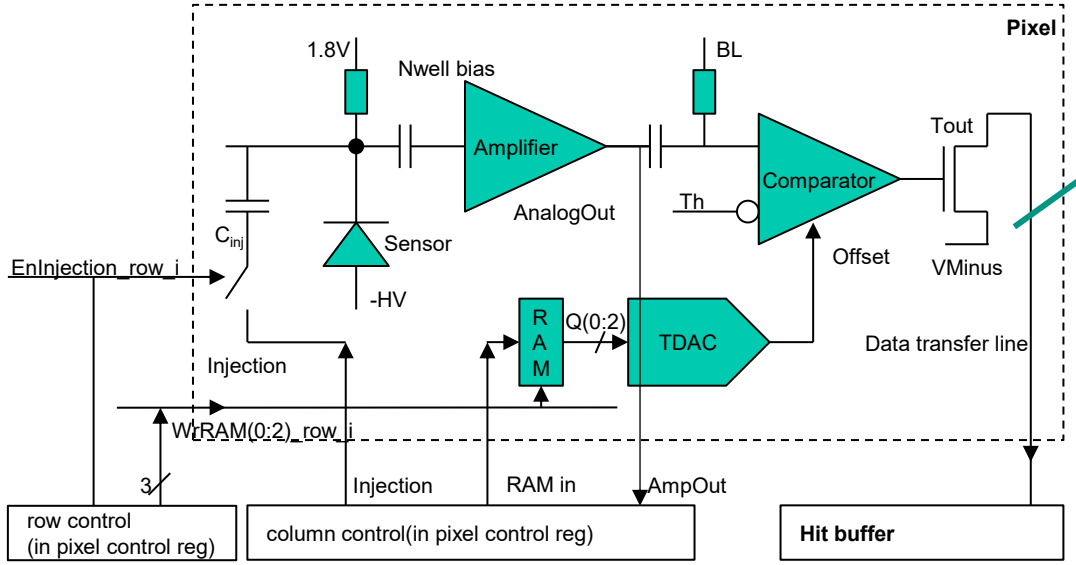
AstroPix5 Block Diagram

- New Blocks to increase level of integration and simplify module design:
  - Vminus Regulator
    - One external supply voltage less
  - Monitoring ADC
    - Bias voltages
    - Temperature Sensors
  - Pulse Generator
    - Helpful for chip calibration and tuning
  - Optional diff. SPI interface
    - Improved signal integrity
    - Less EMI

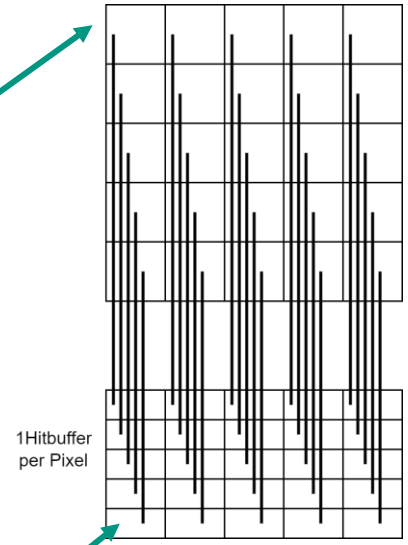


AstroPix Pixel Matrix

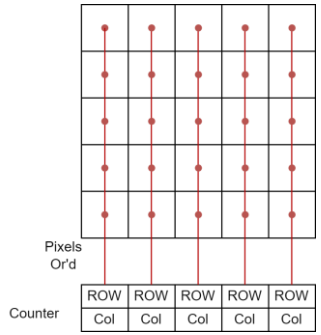
NMOS type amplifier with NMOS only Comparator

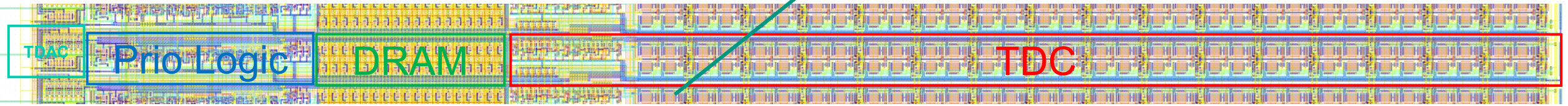


Individual pixel readout from V4



AstroPix1-3: Row/column based readout



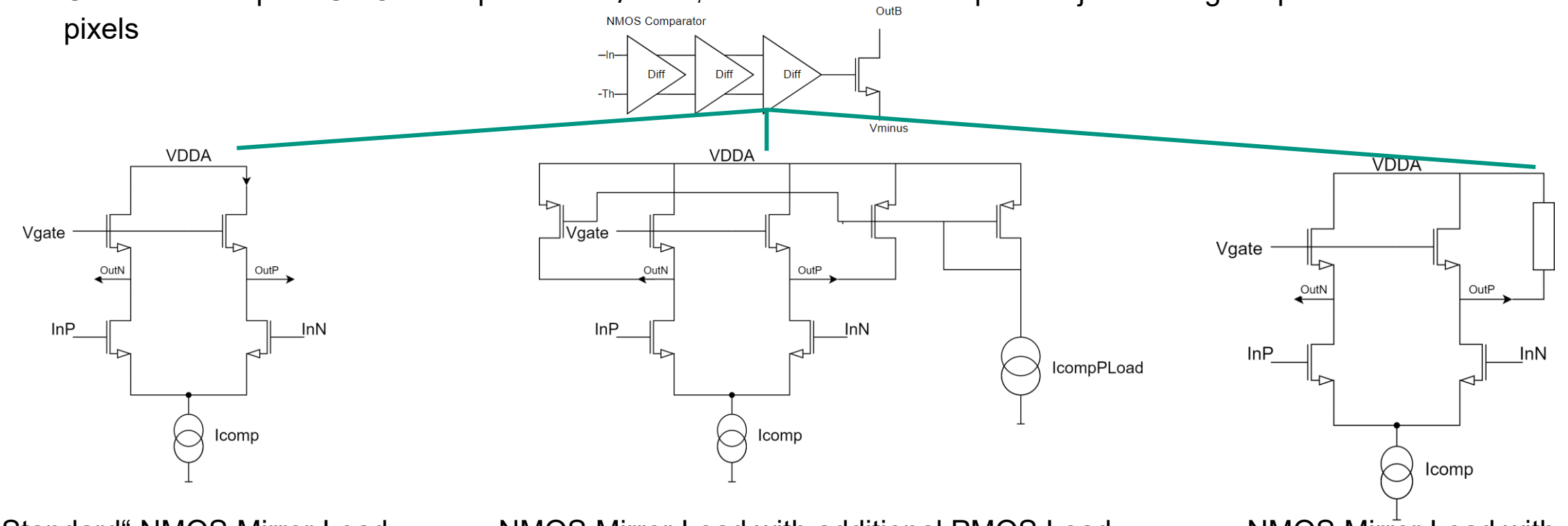


Hitbuffer

- TS gets saved on positive and negative edge of a hit:
- 17 bit 20 MHz corse timestamp (Wraps over after 6.55 ms
- 16 bit TDC for 3 ns fine timestamp

NMOS Comparator Flavours Test Columns

- AMS will not offer deep pwell option in production runs
- Cannot use in-pixel CMOS comparator anymore, because unisolated pmos injects charge in pixel n-well -> oscillating pixels



„Standard“ NMOS Mirror Load

NMOS Mirror Load with additional PMOS Load

NMOS Mirror Load with additional Resistive Load

Design Goal: Low power consumption, high output impedance and large signal swing

Dynamic Feedback Capacitance

- Improve dynamic range from 250 to 700 keV
- Implemented with an NFET to achive bilinear gain

- Small signals only see overlap capacitance (weak inversion)

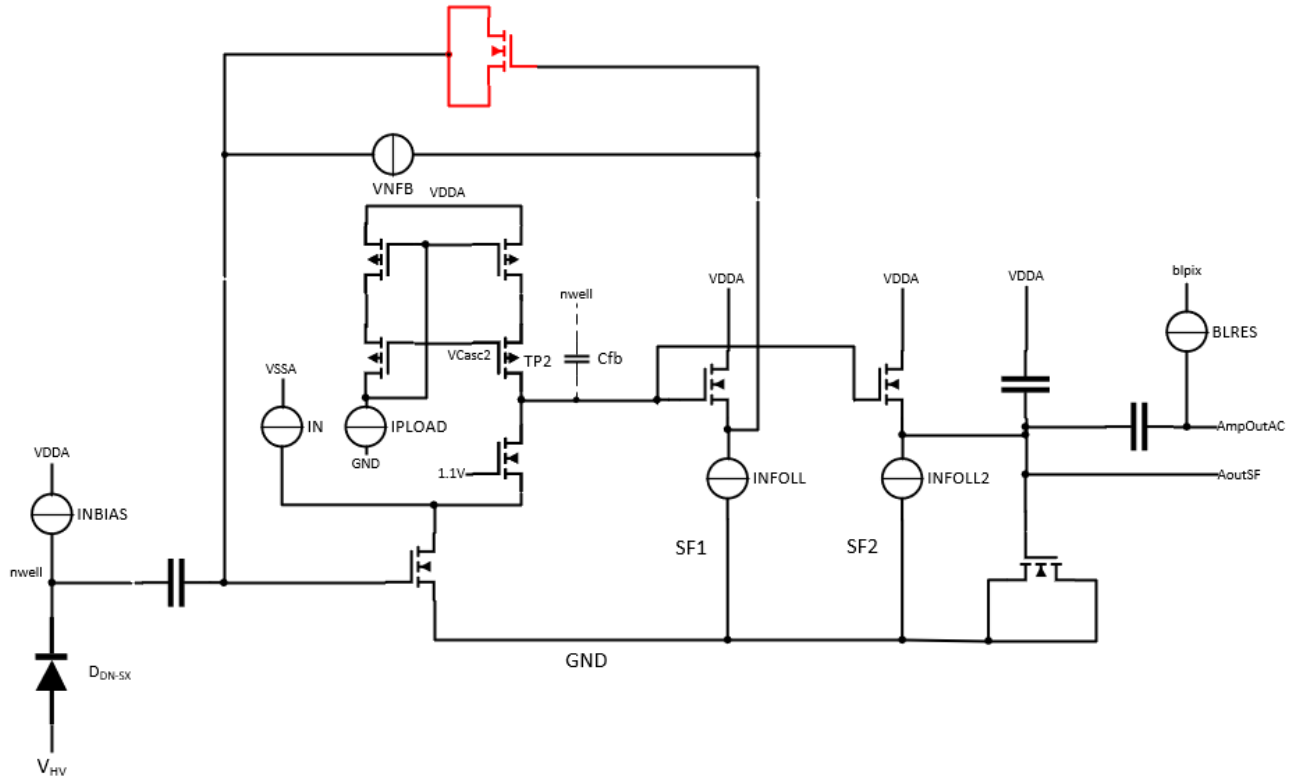
$$C_{small} = C_{fb} + WC_{OV}$$

Small Width to minimise Csmall

- Large signals see also much larger depletion capacitance (strong inversion)

$$C_{large} = C_{fb} + WC_{OV} + \frac{2}{3}\mathrm{WL}C_{ox}$$

Large Length to maximise Clarge



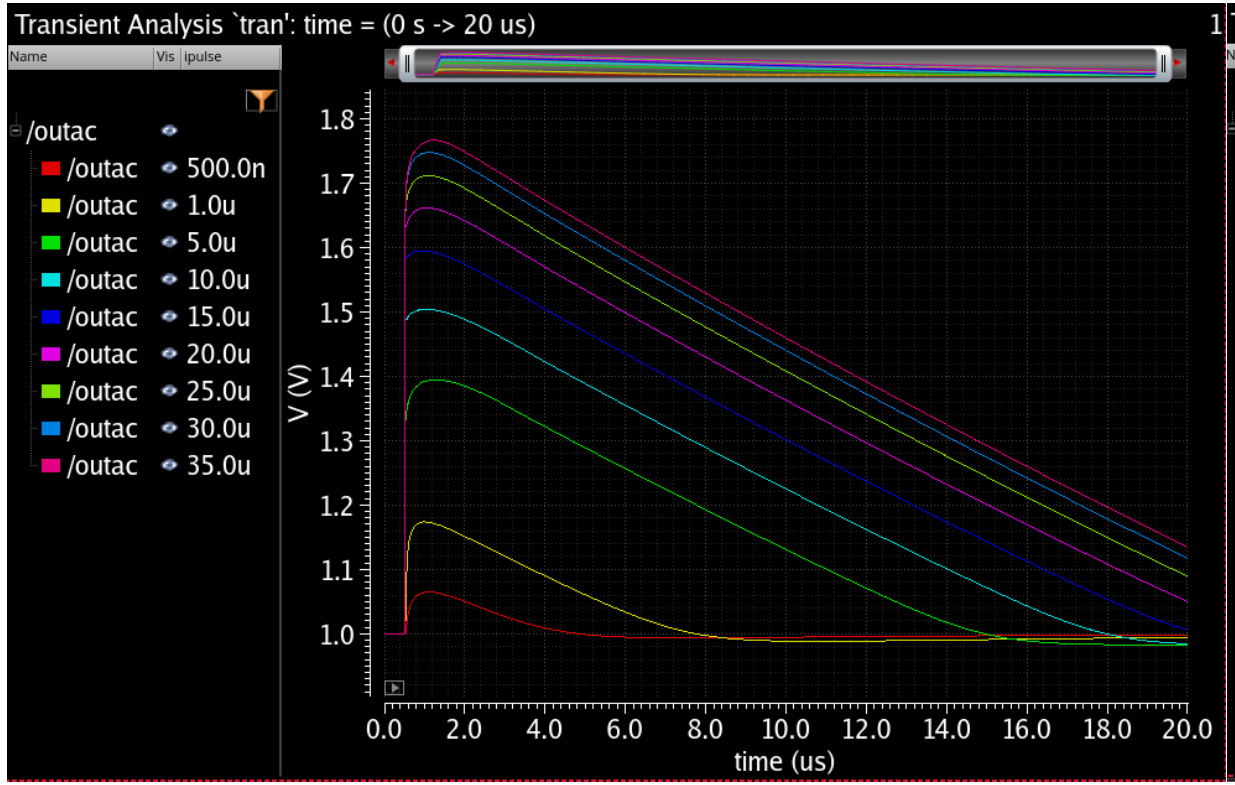
https://ieeexplore.ieee.org/document/8214263

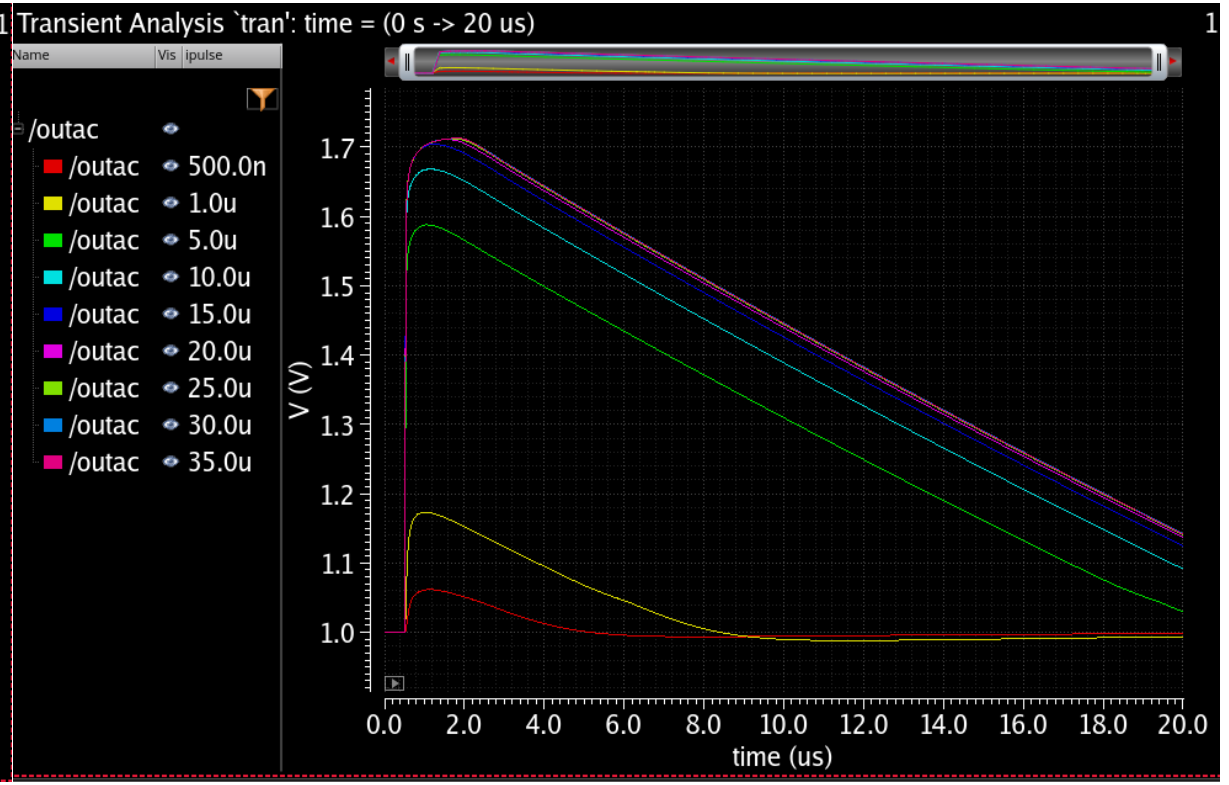
Dynamic Feedback Simulation

Signal at Comparator Input

W/L = 400n/8u

V3/V4 HiDr mode



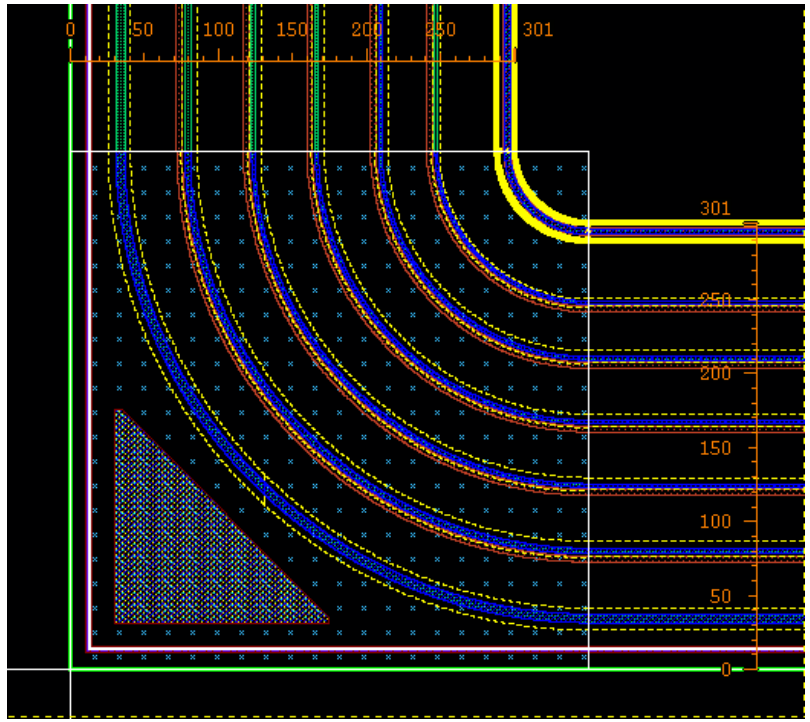


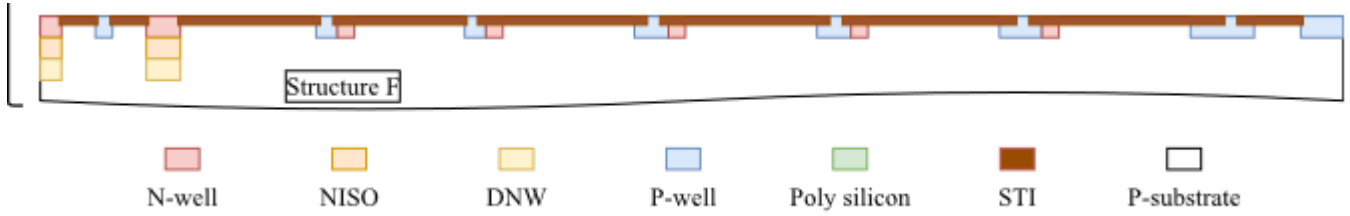
No saturation up to 700 keV, larger dV/dE in upper region

Amplitude saturates > 250 keV

Guardring

- Based on Design from Uni. Bonn
- Measured breakdown > 550 V
- Combination of floating n and p rings
  - Higher potential of floating rings and more equal potential drop
  - Lower maximum electric field strength
- Designed for 1.9 kOhm Wafer
  -> fits well to the 600 – 2kOhm Wafer we use
- Smaller dead area compared to AstroPix3/4 design



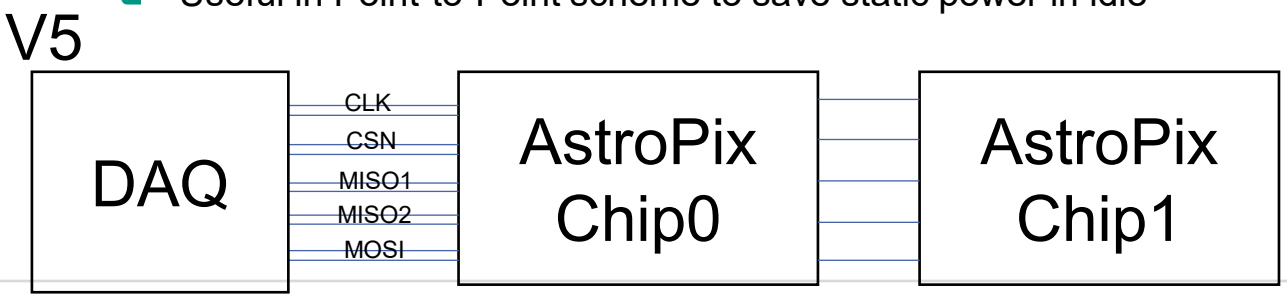


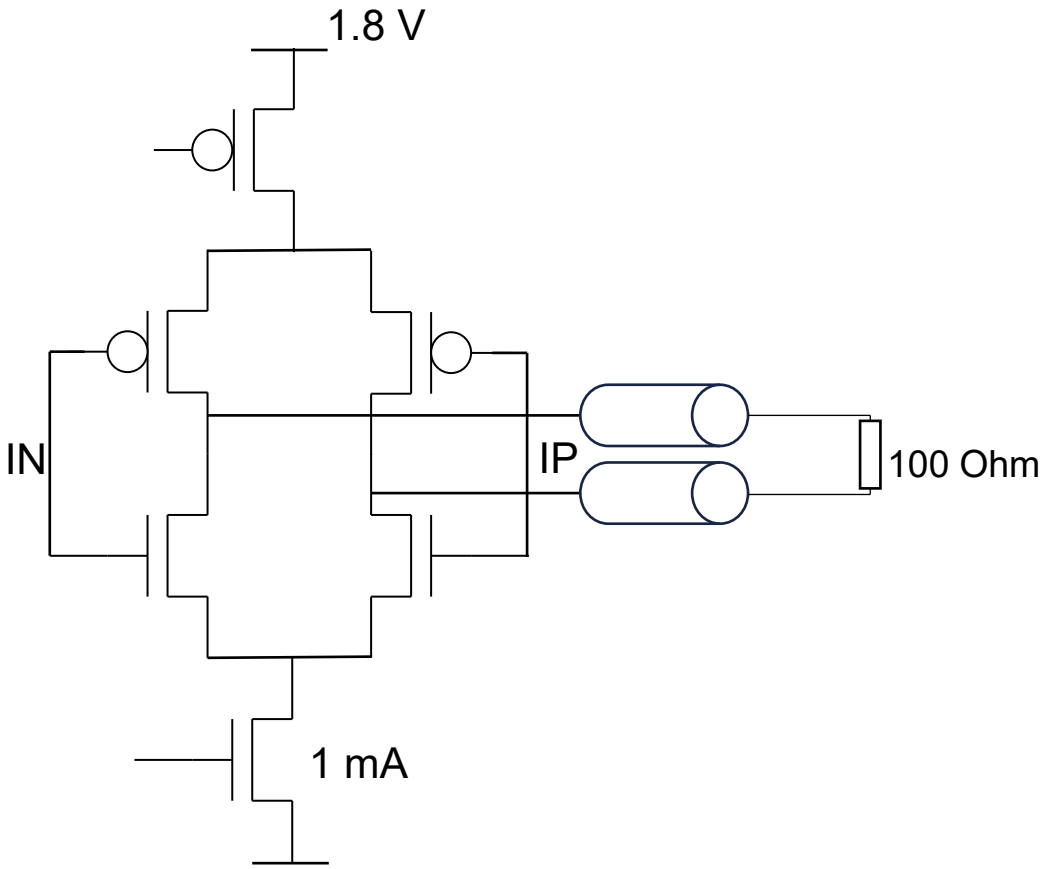
Sinuo Zhang, Ivan Caicedo, Tomasz Hemperek, Toko Hirono, Jochen Dingfelder,
Breakdown performance of guard ring designs for pixel detectors in 150 nm CMOS technology,2024,
ISSN 0168-9002,
https://doi.org/10.1016/j.nima.2024.169287.

Differential SPI Option

- First chip in a row can be optionally connected differentially to DAQ
- Differential drivers/receivers disabled on other chips

- Low power switched current sources driver
- Static Power consumption: 2.5 mW
- Vdiff: 100 – 200 mV
- Vcm: 0.8V
- **Bus mode**:
  - Output stage tristated if CSN high
  - ~70 ns setlling time from Tristate to on-state
  - Useful in Point-to-Point scheme to save static power in idle





New SPI commands

- Heartbeat
  - Send to specific chips via ID or broadcast to all chips
  - Chip answers with special data packet
    16 bit Extrabits + 16bit ExtrabitsN from the chipconfig + 8 bit SEU count
  - **Useful to check if chips are alive and correctly configured (Matching ExtraBits)**

- ADC Readout
  - Implemented low power Sigma-Delta ADC
  - Triggers ADC to read 7 voltages
    (2 Temperature sensors and 5 Biasvoltages)
  - Improved temperature sensor:
    - Good linearity from -40 to 100 °C
    - Higher sensitivity ~3 mV/K vs 1.8 mV/K
  - One ADC Readout cmd per second (~1ms acqusition time for all 7 values) -> 0.3 uW average power for ADC
  - **Easy way to monitor voltages in the experiment**

Command	
0x1	IDLE
0x2	Routing Command
0x3	Shift Register Config
0x4	**Heartbeat**
0x5	**ADC Readout**

Improved SEU Tolerance

- Synthesized Digital Configbits are now also triple modular redundant
  - 3 Memory cells for every bit -> Majority Voter Output
  - In case of mismatch between cells -> Refresh with Majority Voter Output
- Single SEU Bitflips can be corrected

- Majority mismatch connected to an 8 bit TMR counter to monitor refreshes
  - Readout of the counter value via SPI Heartbeat

- Special Constraints for Place and Route Tools to ensure enough clearance between triplicated memory cells

Estimated Power Consumption

- Pixel 4.6 uW Pixel Matrix 5.3 mW
  - 3.6 uW Amplifier + Comparator (if 1.2 V supply is used to bias amplifier)
  - ~1 uW for Bandpass filter and etc.
- Digital 2.2 mW
  - 700 uW DigitalTop
  - 400 uW DLL + PLL
  - 1.1 mW TS (0.5 mW)
- Analog 300 uW
  - Biasblock, VDACs ~250 uW
  - Chargepump ~50 uW
- **Total: ~2 mW/cm^2** for 2 x 2 cm chip

Summary

- First large AstroPix chip with per pixel readout and TDC
- Can be powered from single 1.8 V supply, Vminuspix and Vgate are generated internally
- Removed deep p-well to be compatible to AMS ah18 standard process and technologically compatible to more other foundries like SkyWater etc.
- New guardring design with higher breakdown and less dead area
- Testcolumns with improved dynamic range and different comparator flavours
- Integrated injection generator, less external control signals needed
- Improved SPI Interface with differential readout option
  - Heartbeat and ADC readout command
  - Improved Interrupt for more efficient readout
- Improved SEU tolerance by TMR Configbits for digital logic