Overview of AstroPix Performance

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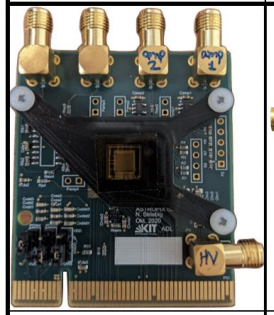
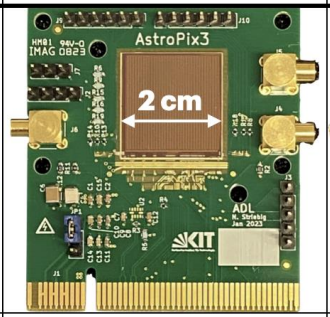
4th BIC Workshop, Argonne National Lab

Overview

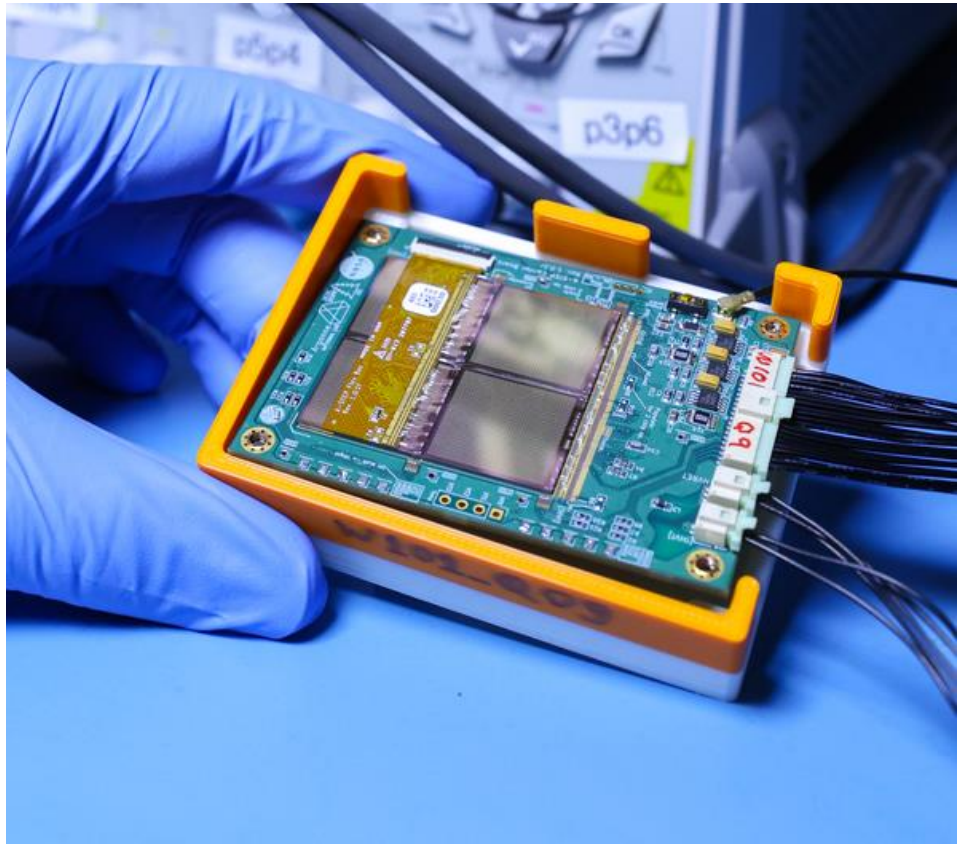
2020 AstroPix_v1	2021 AstroPix_v2	2023 AstroPix_v3	2024 AstroPix_v4	2025 AstroPix_v5
				
1st prototype: incremental design changes from ATLASPix	2nd prototype: Power reduction, Radiation testing '22	**Flight prototype:** Beam tests '23, '24 Sounding Rocket '26	4th prototype: individual pixel readout, Power reduction	5th prototype: AMS Foundry Energy range, Power reduction, Balloon '28(?)

Discussion Topics:

- AstroPix Version 3
- AstroPix Version 4
- SW/FW Development

AstroPix Version 3 : Overview

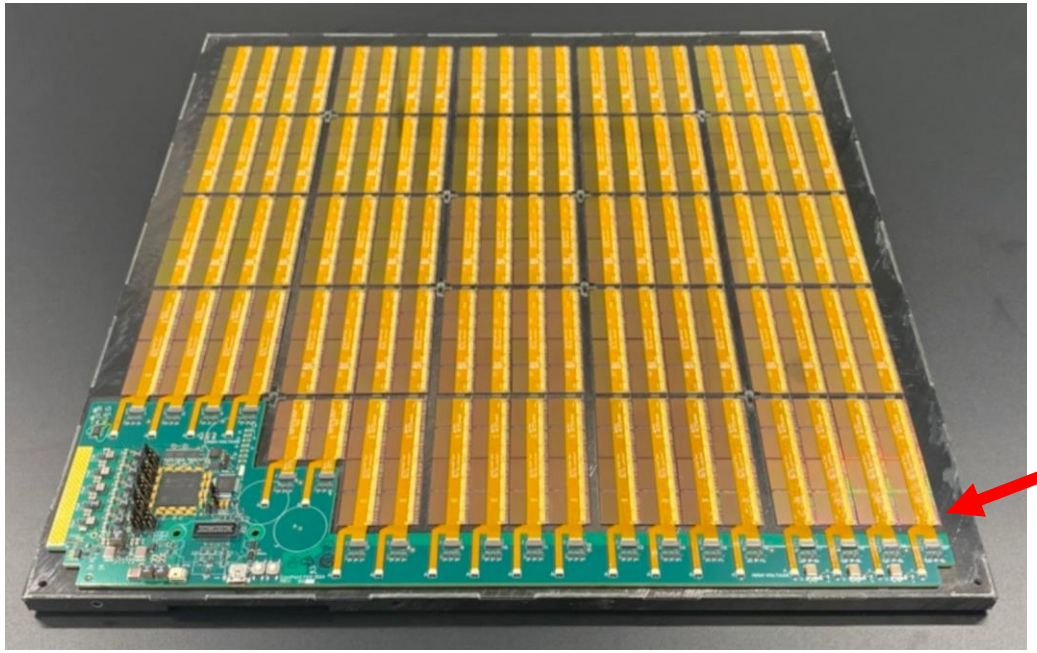
- **AstroPix v3** is the first 2x2 cm^2 chip implemented.
- Last version with OR'd Row/Column Hit Buffers
- First version of AstroPix tested in "quad-chip" design.
- Testing with AstroPix v3 is still providing lots of important feedback on how to operate the AstroPix daisy-chain readout.



AstroPix v3 Quad Chip Test Board

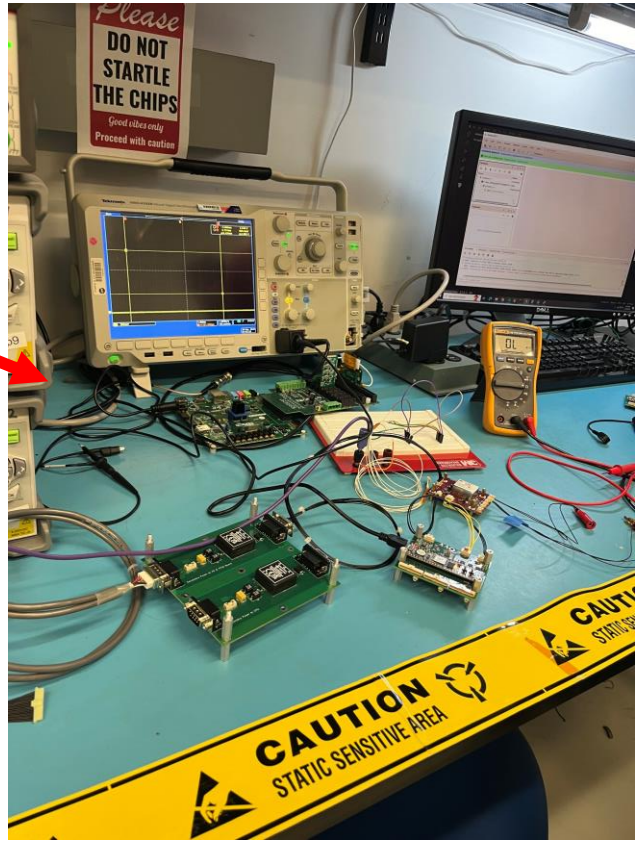
AstroPix Version 3 : Overview

New hardware has been developed to interface with AstroPix v3, moving away from the Nexys Video + GECCO board readout.



Compton-Pair (ComPair-2) Segment

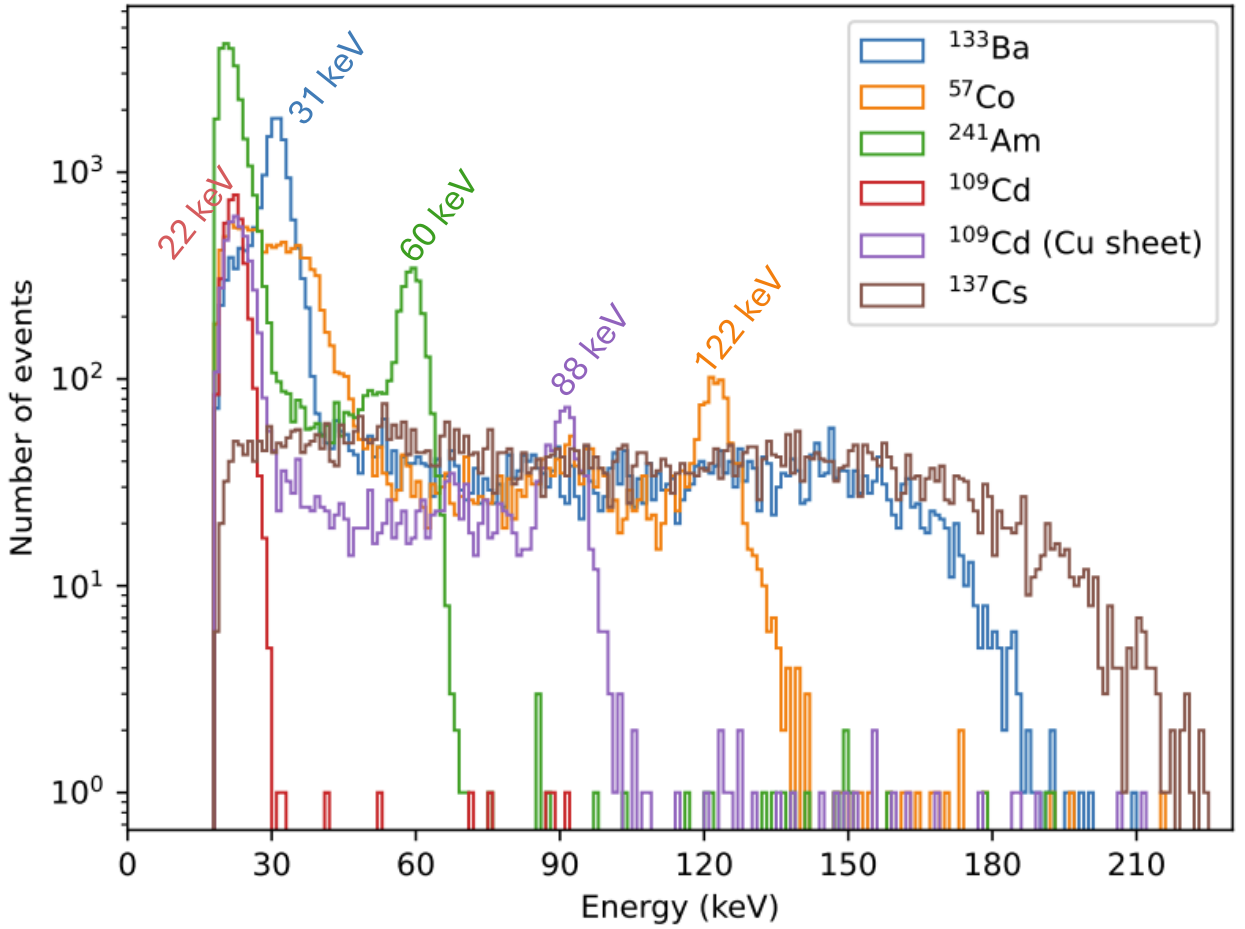
AstroPix Sounding Rocket Technology Demonstration Payload (A-STEP)



AstroPix Version 3 : Single Chip Performance

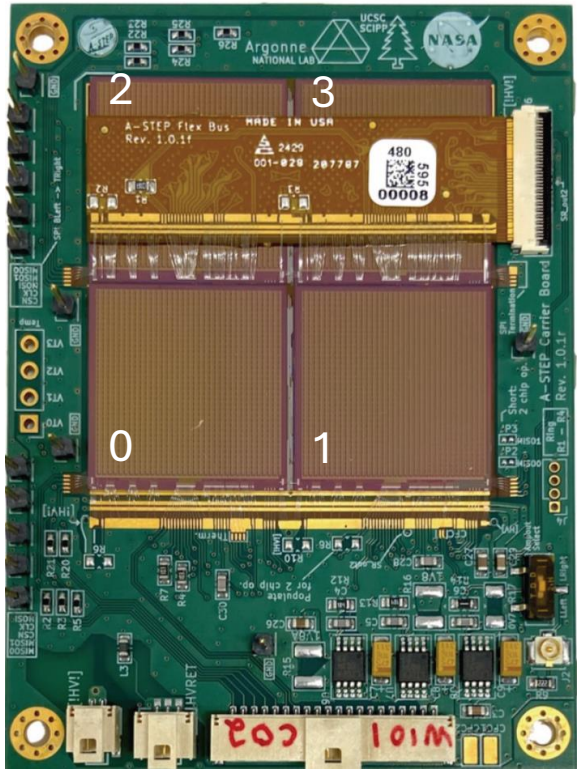
- AstroPix v3 detector testing: mean 6.4 keV FWMH at 59.5 keV.
- 44% of pixel meet target (<10% FWHM at 60 keV)

Single Pixel Source Spectra

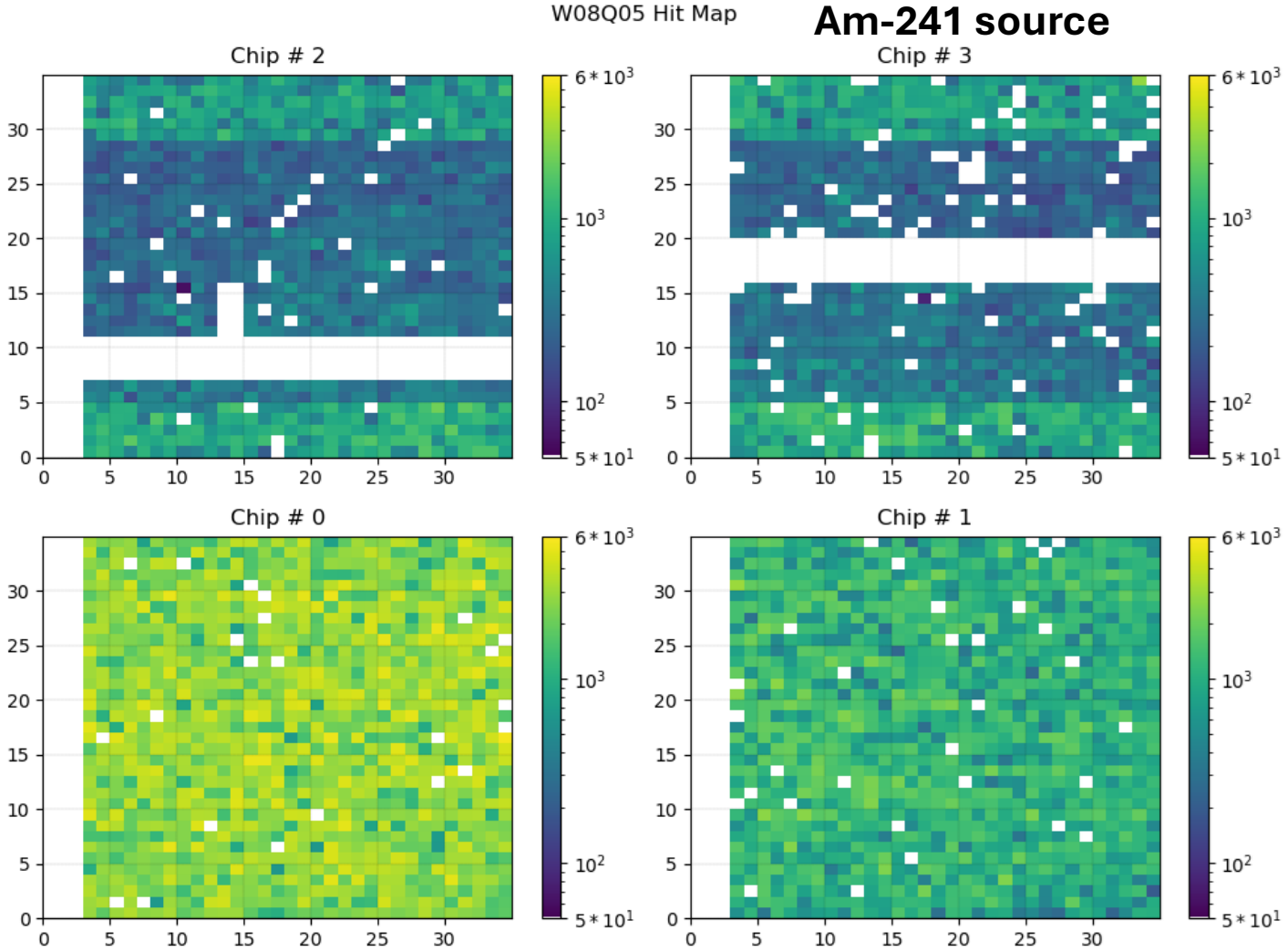


Credit: Yusuke Suda, Hiroshima U. (https://arxiv.org/abs/2408.12891)

AstroPix Version 3 : Quad Chip Performance



- Hit-map of four AstroPix chips on one SPI bus
- Recorded 580 events/s after row/col hit matching

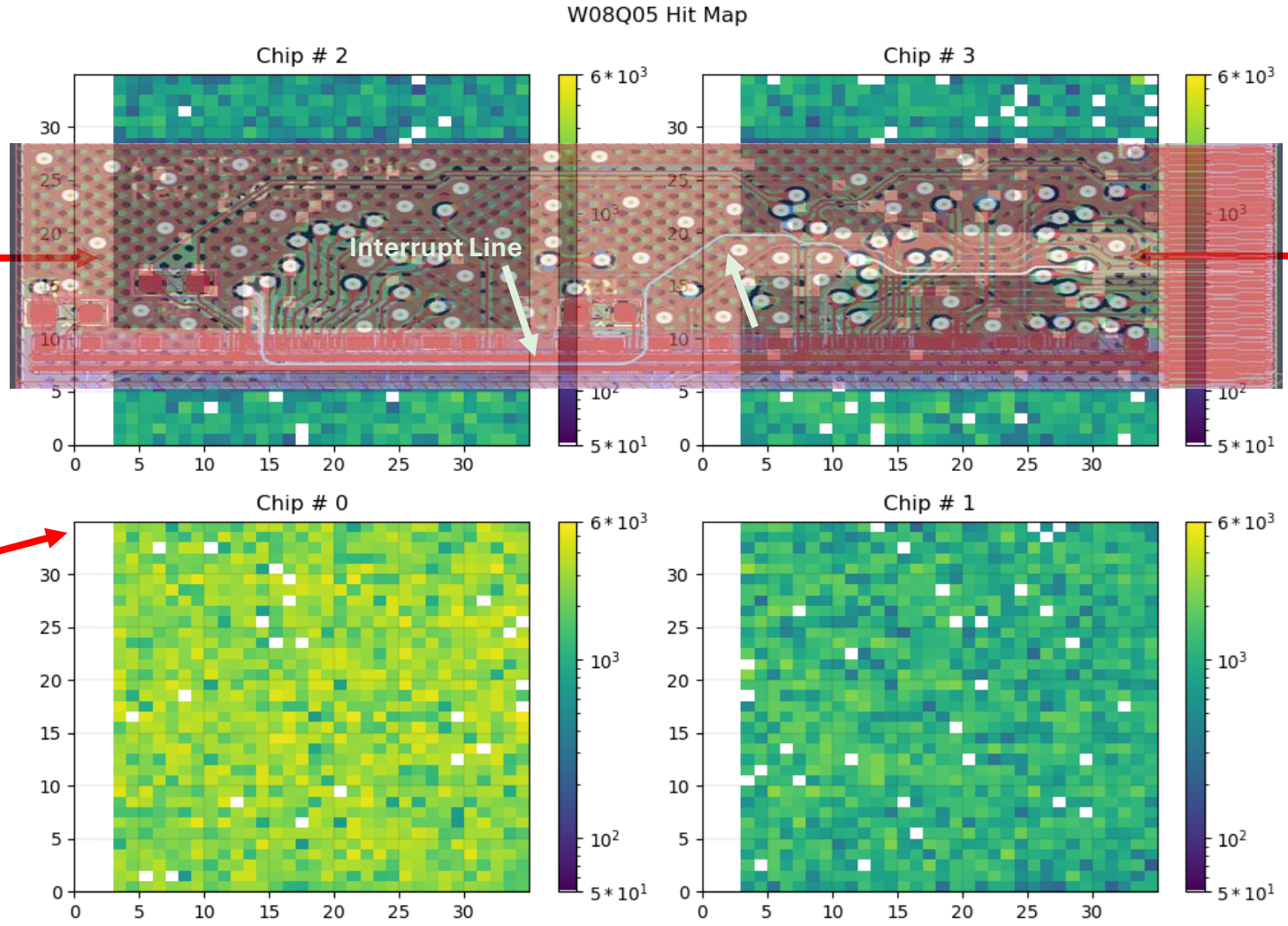


Credit: Kavic Kumar, UMD College Park, Adrien Laviron NASA\GSFC

AstroPix Version 3 : Quad Chip Performance

Bus bar photon attenuation

PMOS comparator test columns disabled



AstroPix Version 3 : Thermal Testing

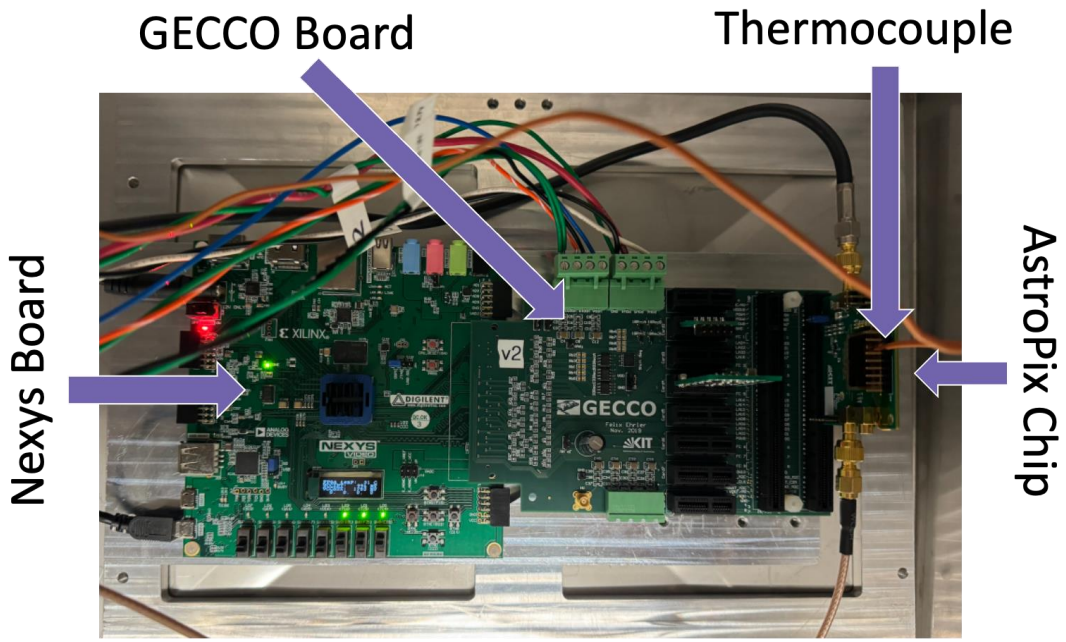
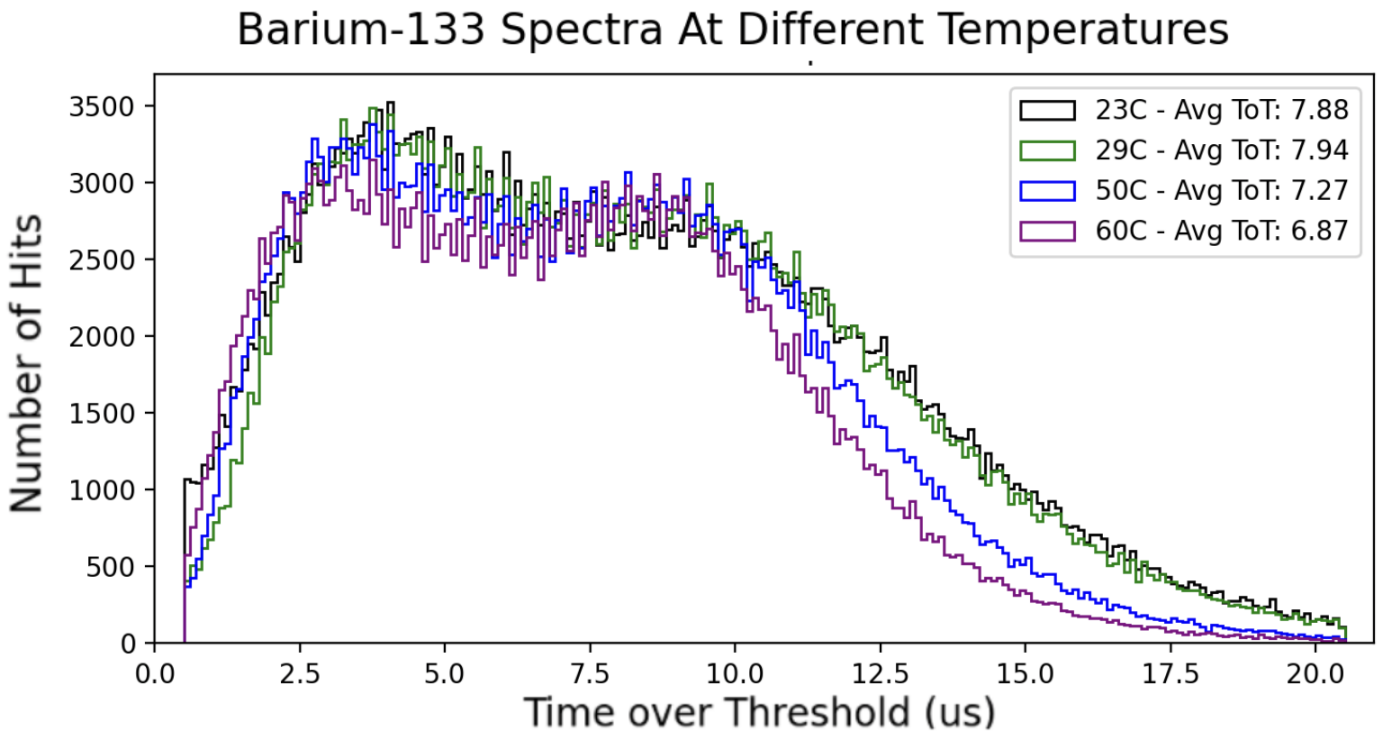


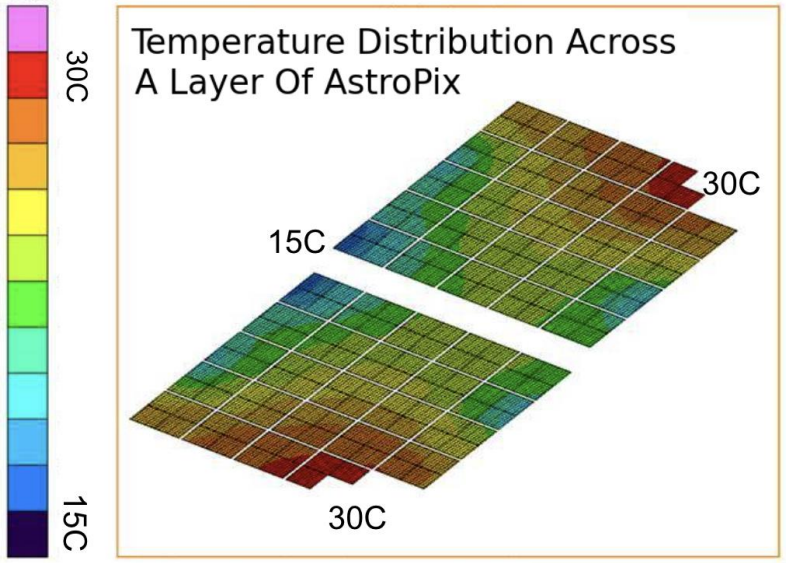
Figure 4: Experimental setup with AstroPix in a thermal chamber

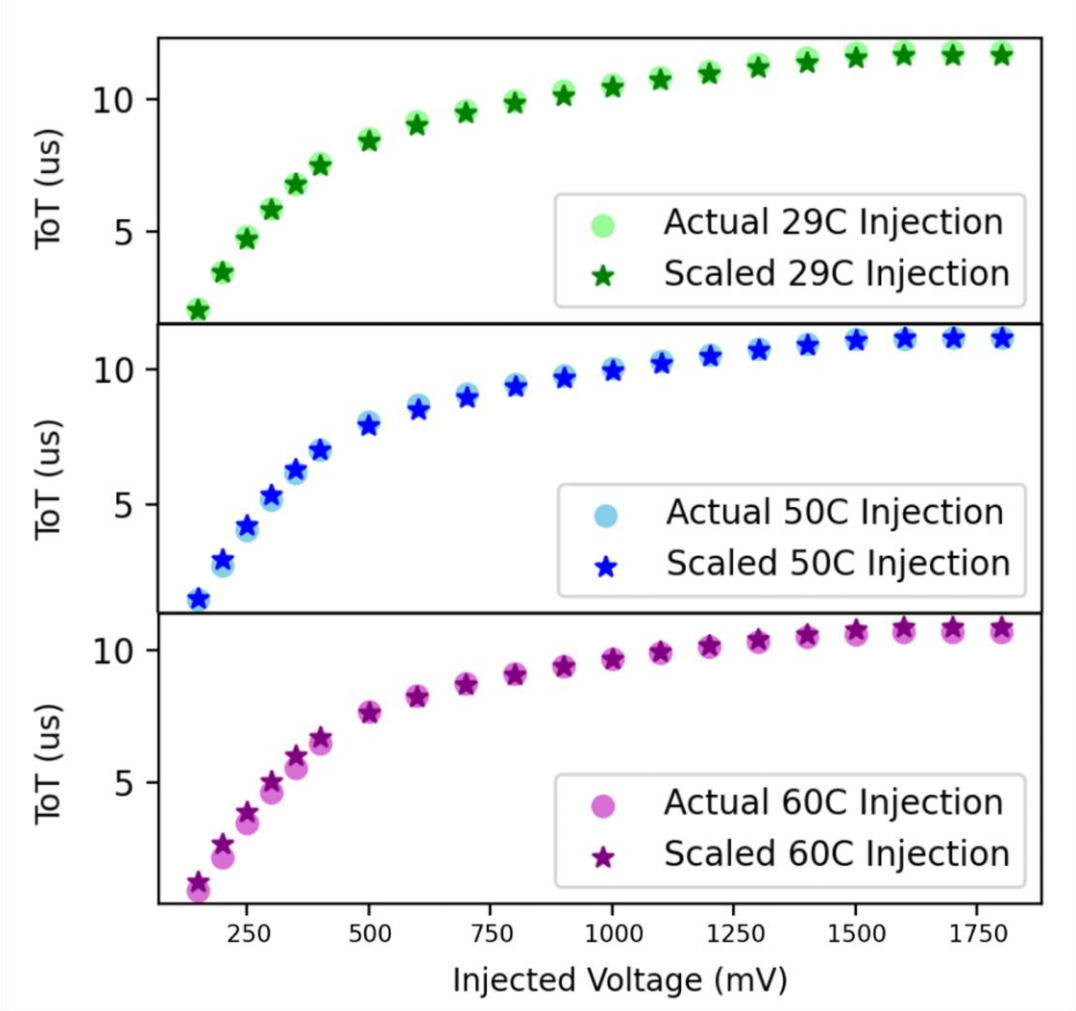


Credit: Carolyn Chinatti, Carleton College

AstroPix Version 3 : Thermal Testing

- Attempted a linear scaling of the shifted ToT spectrum as a function of temperature.
- Some noted energy dependent shifts remain, bimodality of the amplifier, other effects?

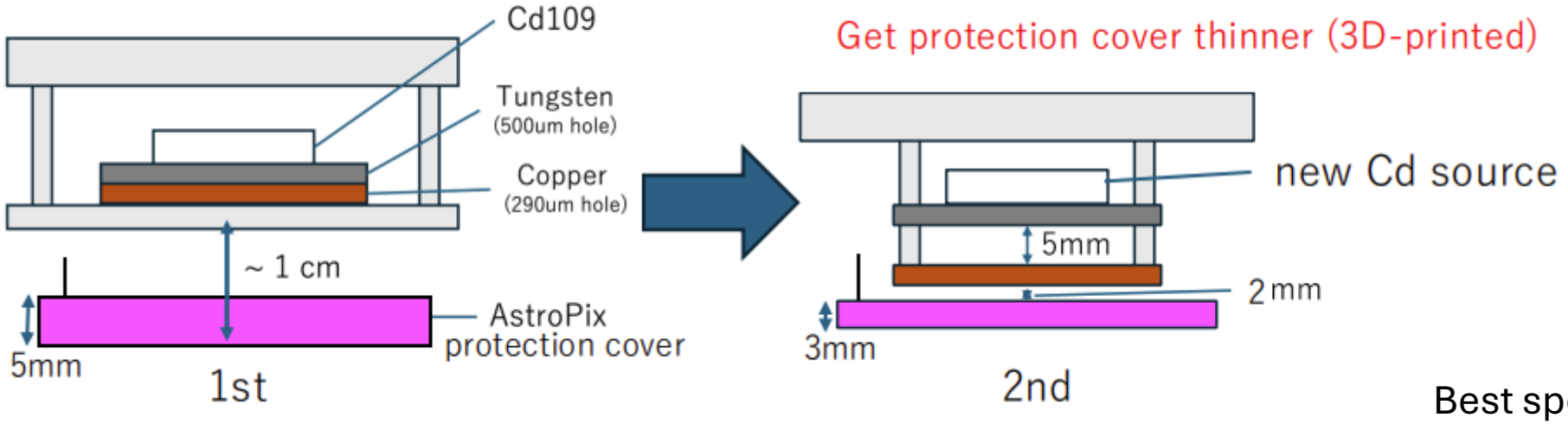




Credit: Carolyn Chinatti, Carleton College

AstroPix Version 3 : Sub-Pixel Scans

- We want to understand AstroPix's subpixel detection efficiency.
- Is depletion uniform? What does charge collection look like at pixel boundaries?
- Norito Nakano designed experiment to collimate x-rays for a 2-D scan using Cd-109.



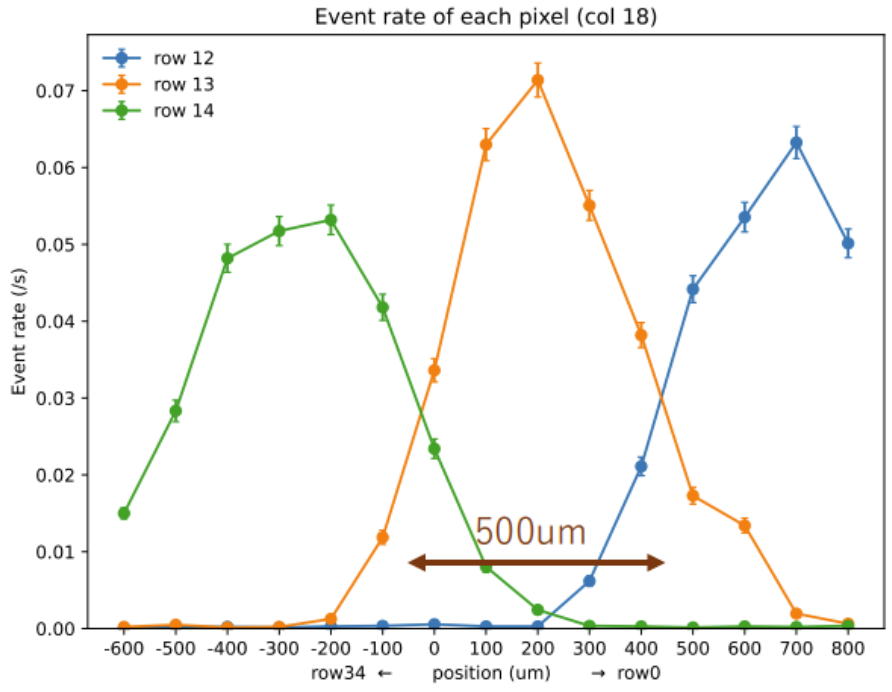
Best spot size: ~220 um

Credit: Norito Nakano, Hiroshima U.

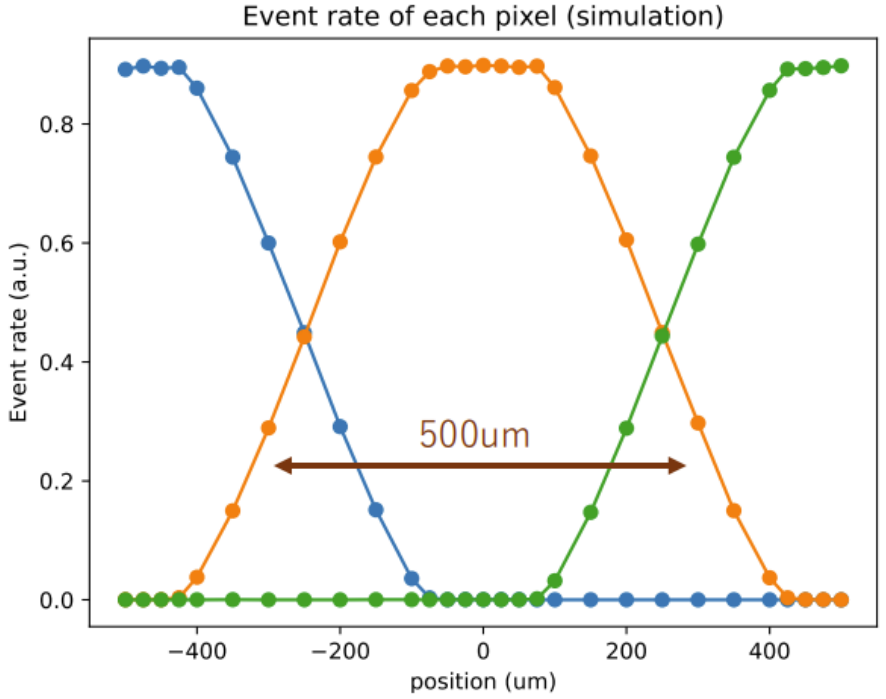
AstroPix Version 3 : Sub-Pixel Scans

- Showed change-over in count rate from one pixel row to the next while scanning across a column. Compared simulations.

Data

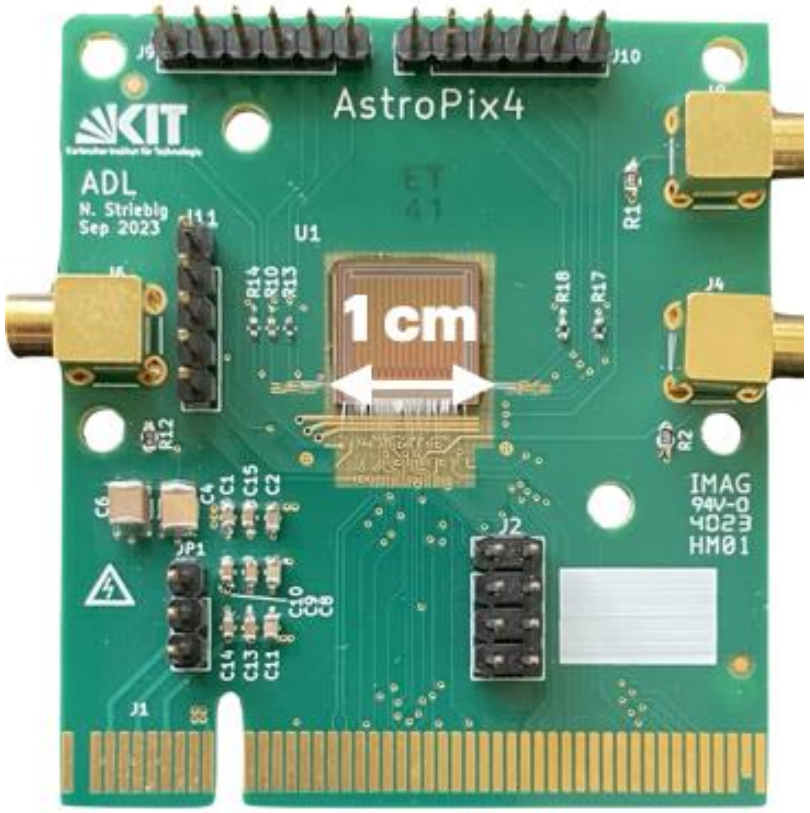


Simulation

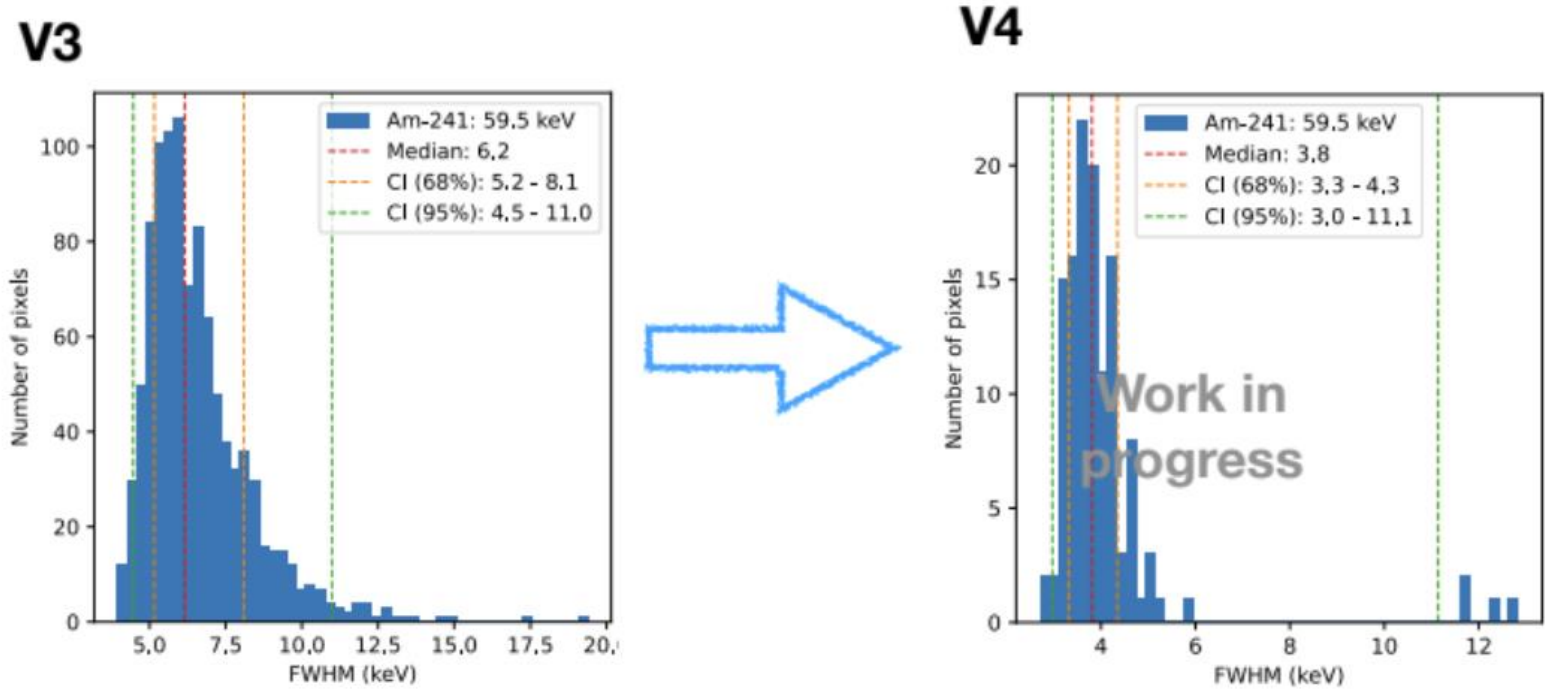


Credit: Norito Nakano, Hiroshima U.

AstroPix Version 4

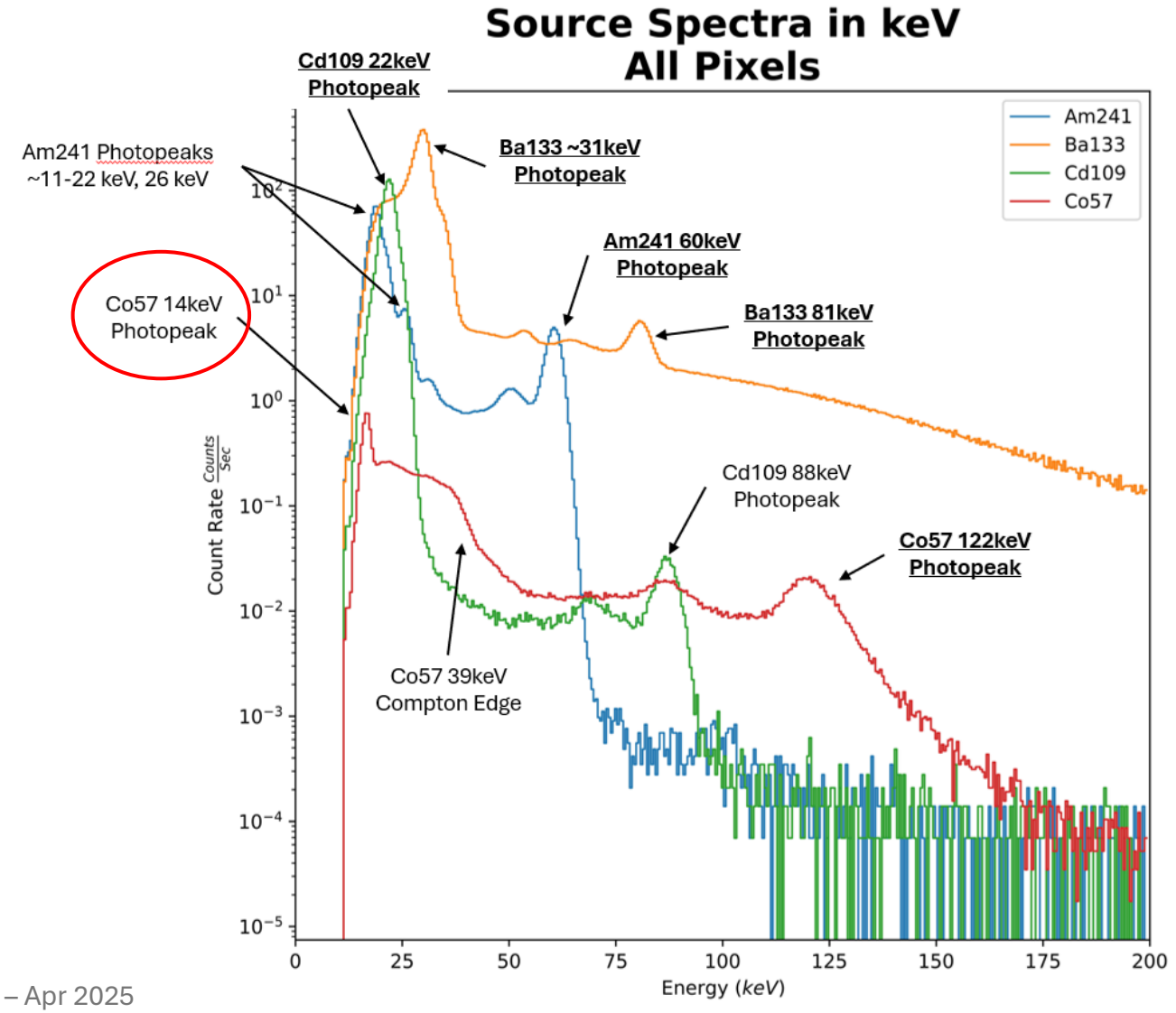


Reduction in pixel capacitance!



Credit: Yusuke Suda, Hiroshima U

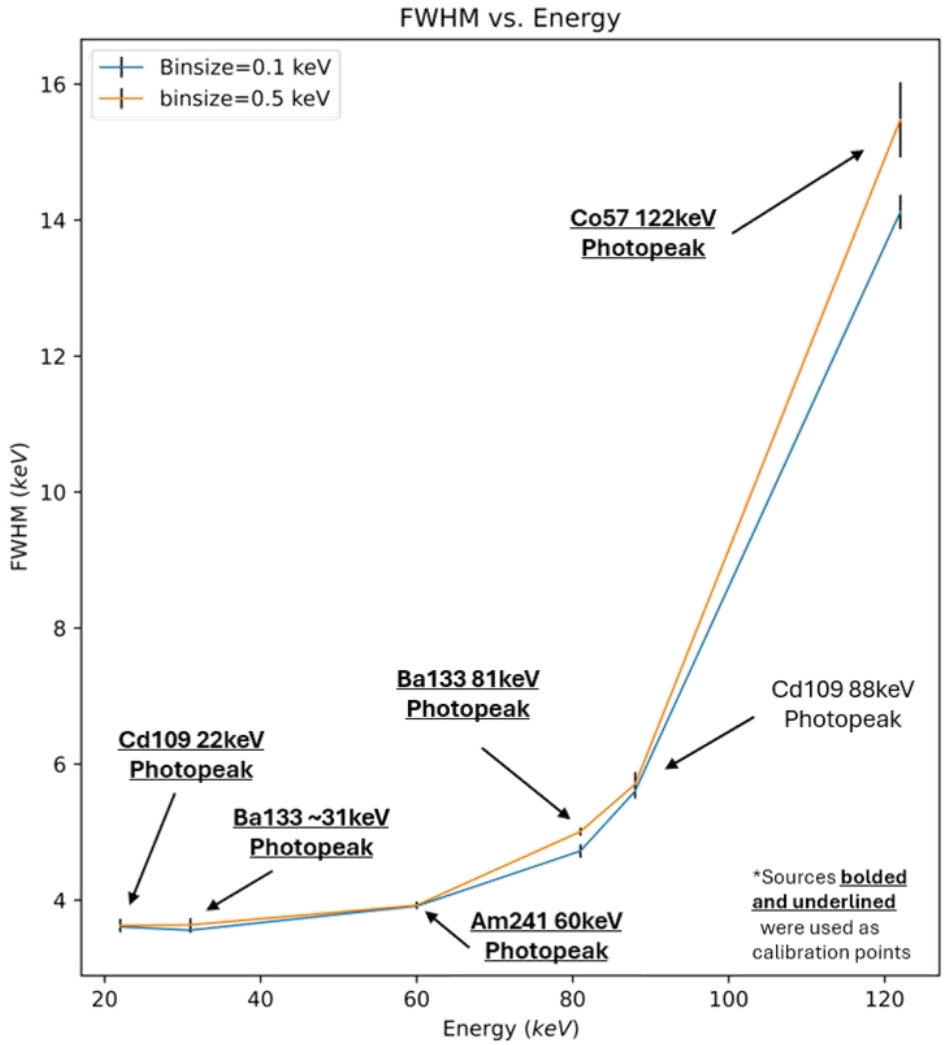
AstroPix Version 4: Performance

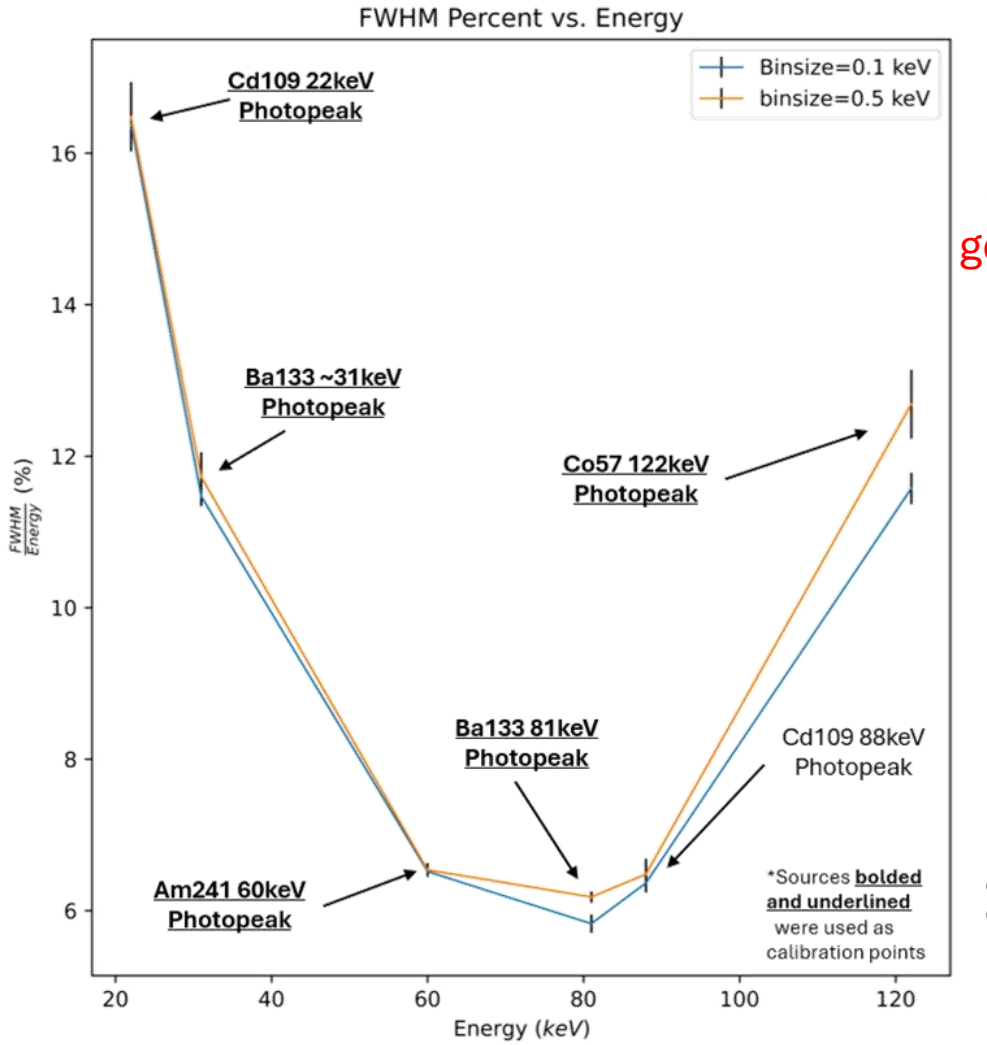


Credit: Grant Sommer, GW University.

*Sources **bolded and underlined** were used as calibration points

AstroPix Version 4: Performance



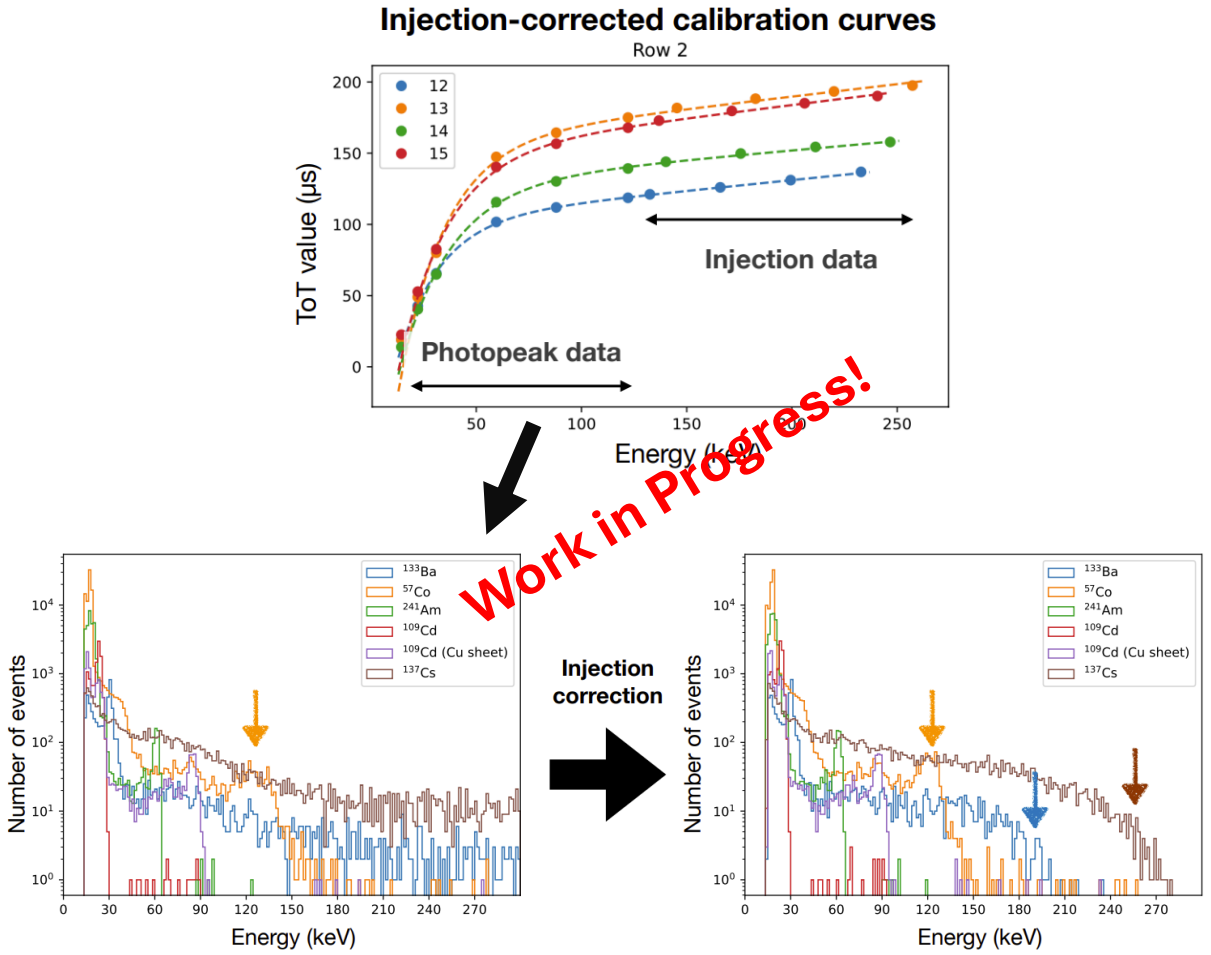


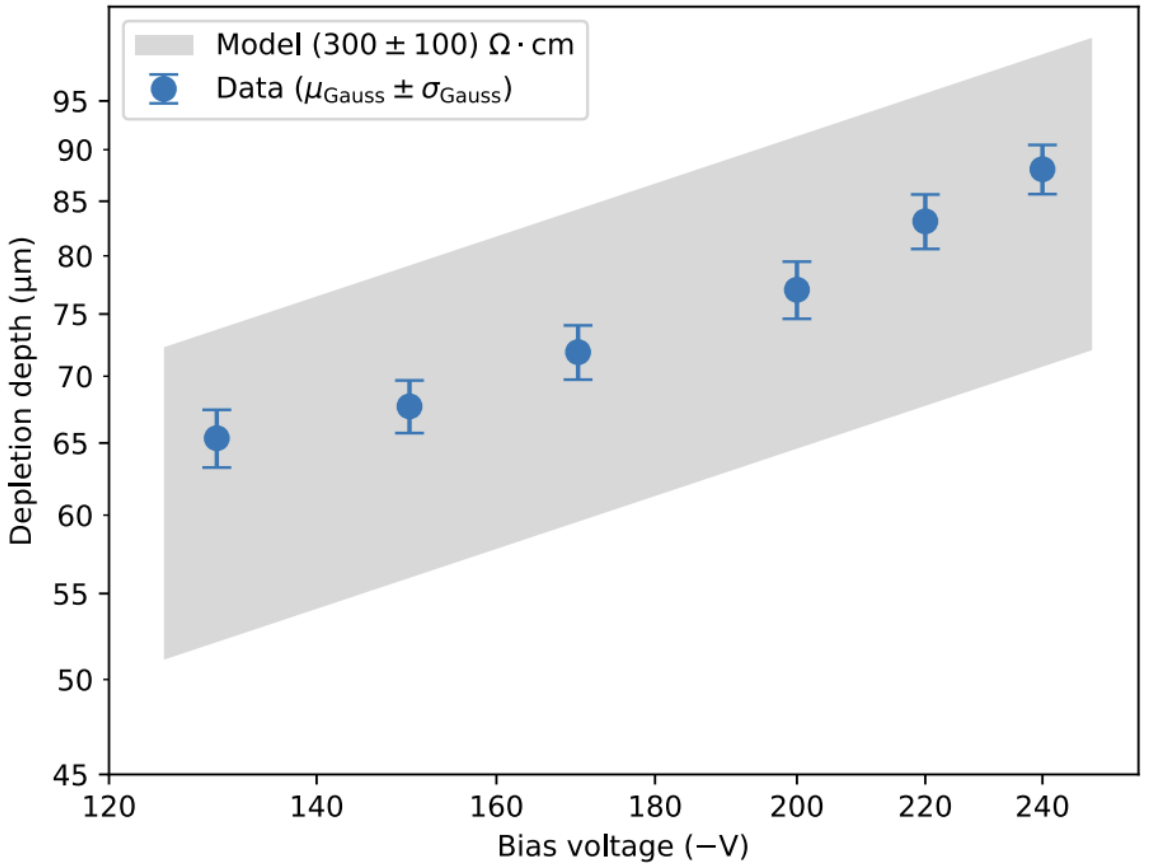
Slightly above goal 10% FWHM at 122 keV!

Credit: Grant Sommer, GW University.

Credit: Grant Sommer, GW University.

AstroPix Version 4: Injection Calibration + Depletion





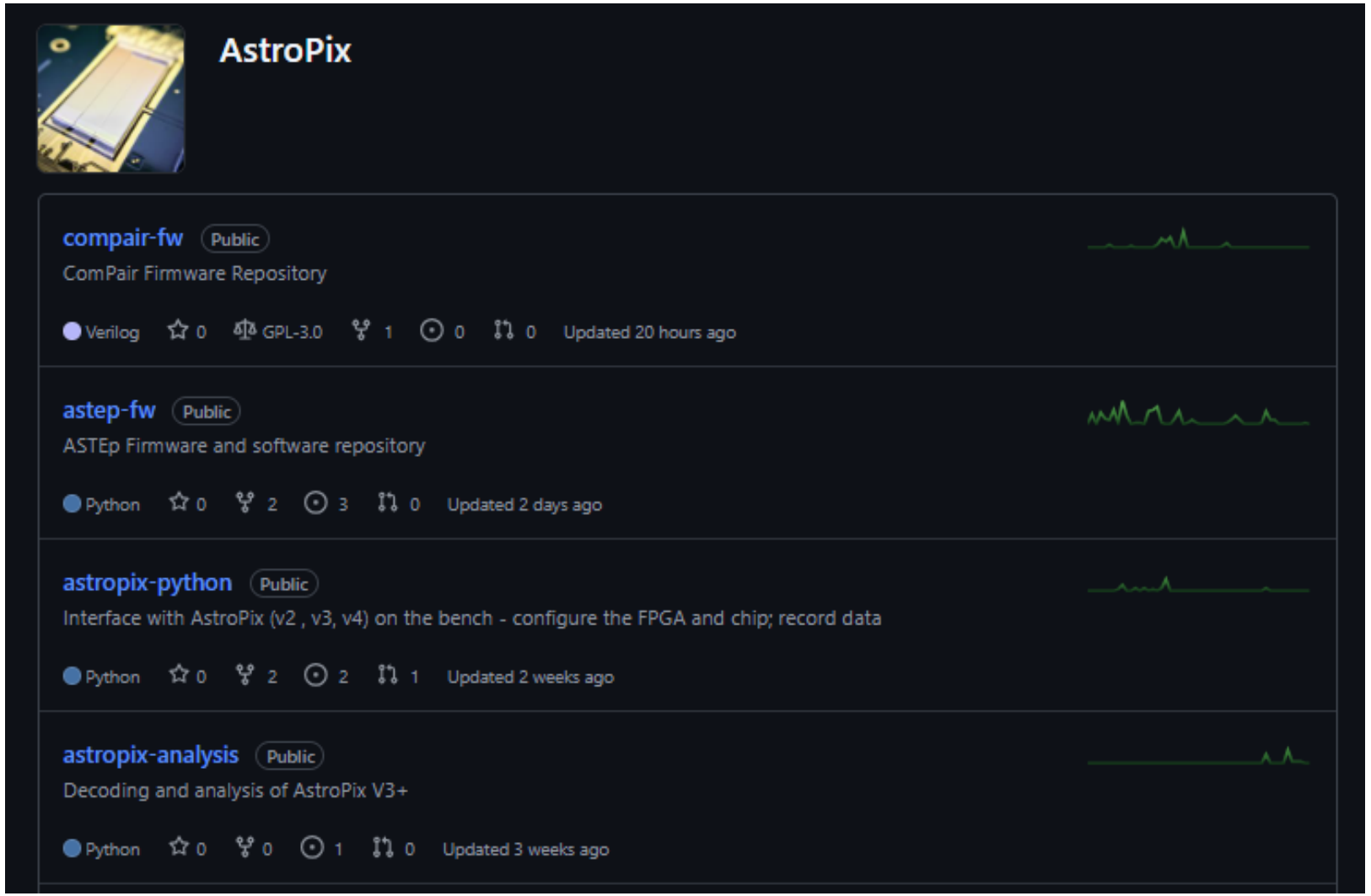
Credit Yusuke Suda, Hiroshima U.

Methods: https://www.sciencedirect.com/science/article/pii/S0168900224006880?via%3Dihub

Software Development

- As the AstroPix user group grows we are attempting to adjust from an R&D mindset.
- Looking for feedback!

https://github.com/AstroPix



Software Development

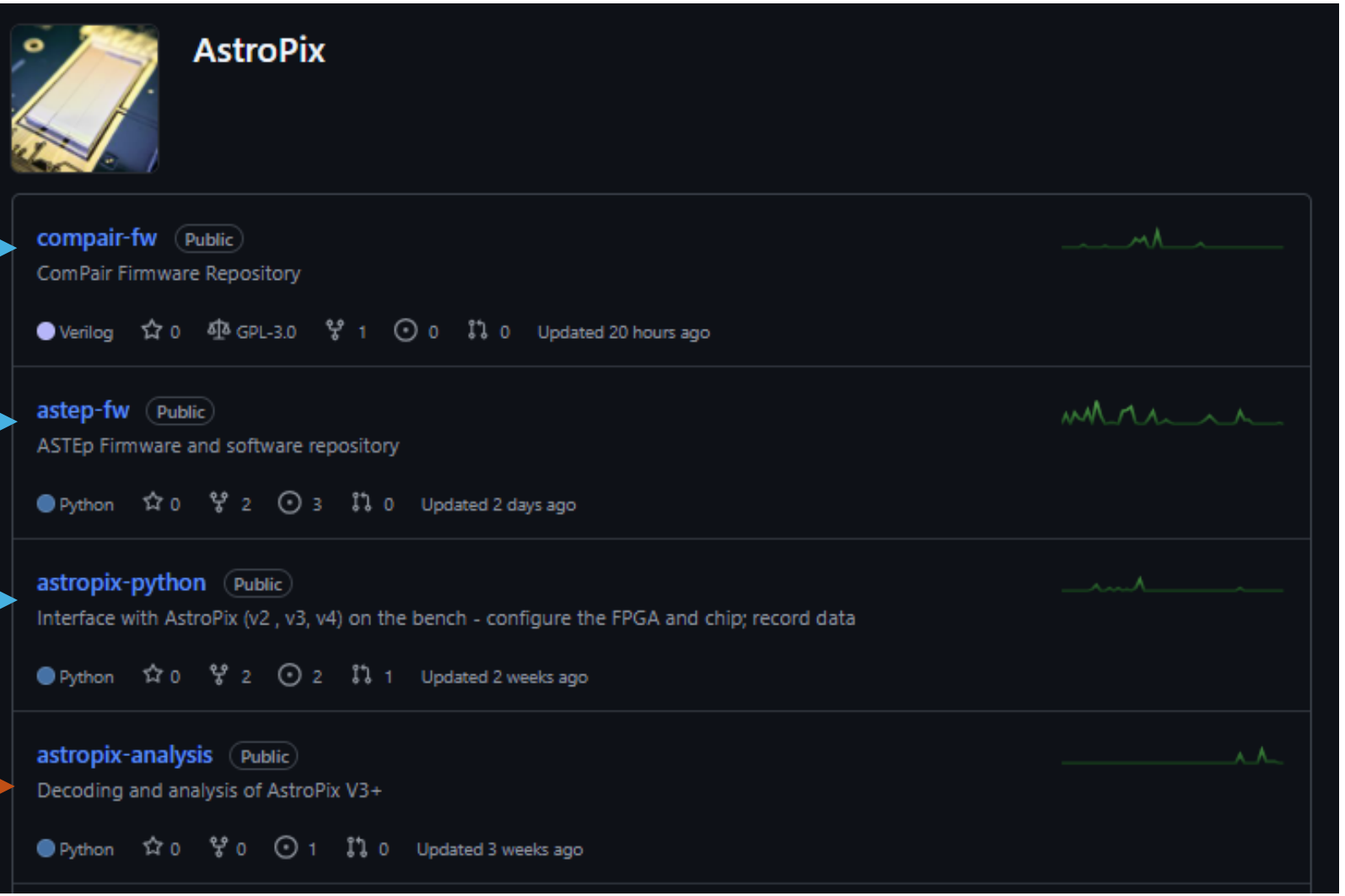
How HW agnostic can this be?

ComPair Segment Running (380 Detectors)!

Quad Chip (v3) Running, Daisy Chain Readout

Single-Chip (v3,v4) Running

AstroPix v3, Quad-Chip, v4 Decoding



Software Development

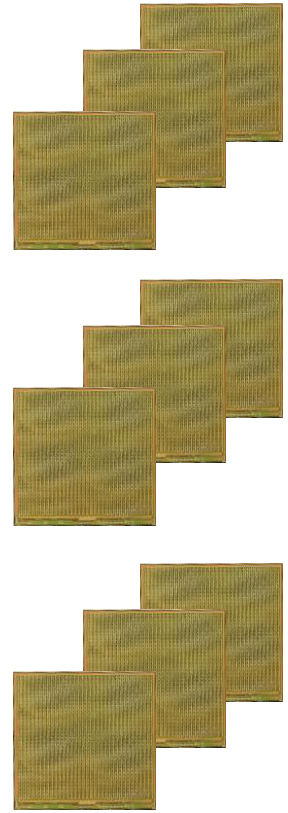
Mostly design agnostic? HW change, # daisy chains just update Register File Map references

Software

Use-specific firmware/ logic

Register File Map

low-level firmware



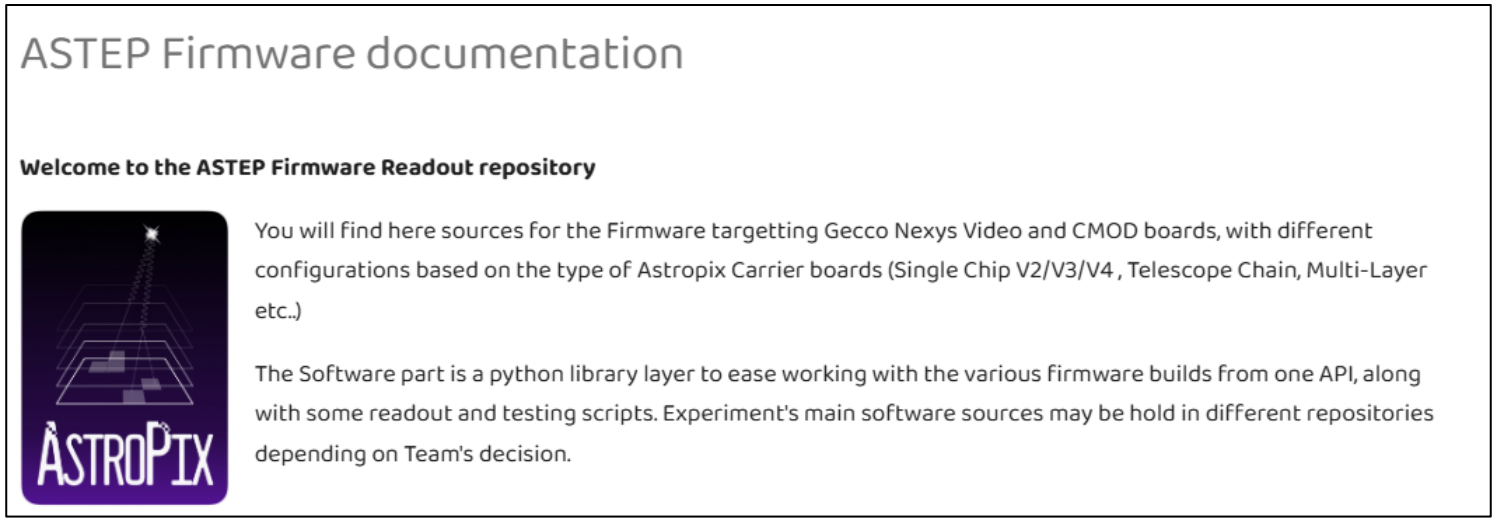
*Adjustable # of AstroPix daisy-chains

Register File Reference

Address	Name	Size	Features	Description
0x0	hk_firmware_id	32		ID to identify the Firmware
0x4	hk_firmware_version	32		Date based Build version: YEARMONTHDAYCOUNT
0x8	hk_xadc_temperature	16		XADC FPGA temperature (automatically updated by firmware)
0xa	hk_xadc_vccint	16		XADC FPGA VCCINT (automatically updated by firmware)
0xc	hk_conversion_trigger	32	Counter w/ interrupt	This register is a counter that generates regular interrupts to fetch new XADC values
0x10	hk_stat_conversions_counter	32	Counter w/o interrupt	Counter increased after each XADC conversion (for information)
0x14	hk_ctrl	8		Controls for HK modules
0x15	hk_adcdac_mosi_fifo	8	AXIS FIFO Master (write)	FIFO to send bytes to ADC or DAC
0x16	hk_adc_miso_fifo	8	AXIS FIFO Slave (read)	FIFO with read bytes from ADC
0x17	hk_adc_miso_fifo_read_size	32		Number of entries in hk_adc_miso_fifo fifo
0x1b	spi_layers_ckdivider	8		This clock divider provides the clock for the Layer SPI interfaces
0x1c	spi_hk_ckdivider	8		This clock divider provides the clock for the Housekeeping ADC/DAC SPI interfaces
0x1d	layer_0_cfg_ctrl	8		Layer 0 control bits
0x1e	layer_1_cfg_ctrl	8		Layer 1 control bits
0x1f	layer_2_cfg_ctrl	8		Layer 2 control bits
0x20	layer_0_status	8		Layer 0 status bits
0x21	layer_1_status	8		Layer 1 status bits
0x22	layer_2_status	8		Layer 2 status bits

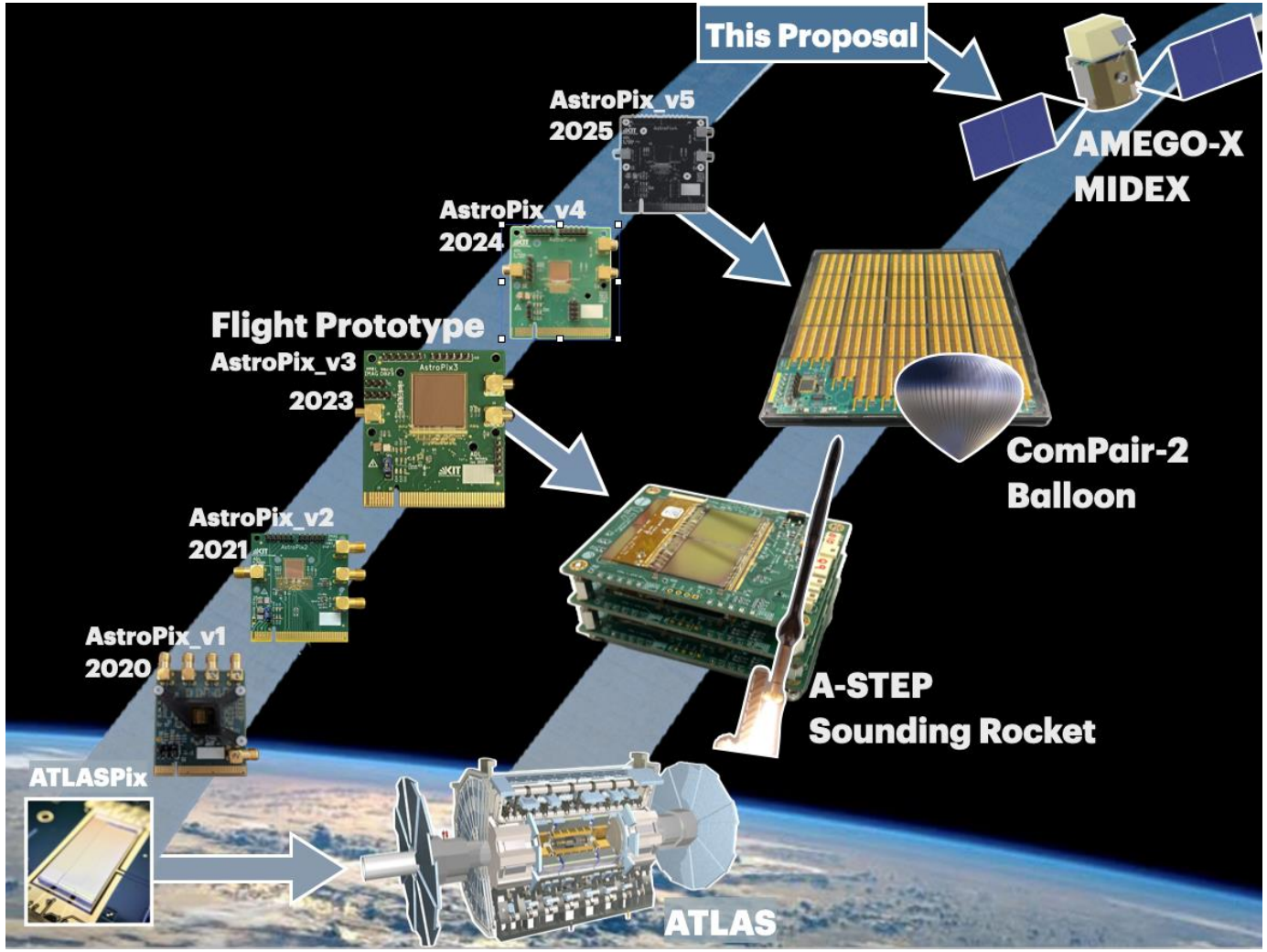
Software Development

- Great firmware/software documentation by Richard Leys



https://astropix.github.io/astep-fw/

Thank You!


This Proposal
AstroPix_v5
2025
AMEGO-X
MIDEX
AstroPix_v4
2024
Flight Prototype
AstroPix_v3
2023
ComPair-2
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2020
A-STEP
Sounding Rocket
ATLASPix
ATLAS