H2GCROC/CALOROC for the BIC

Everything you forgot to ask

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(ORNL)

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H2GCROC overview

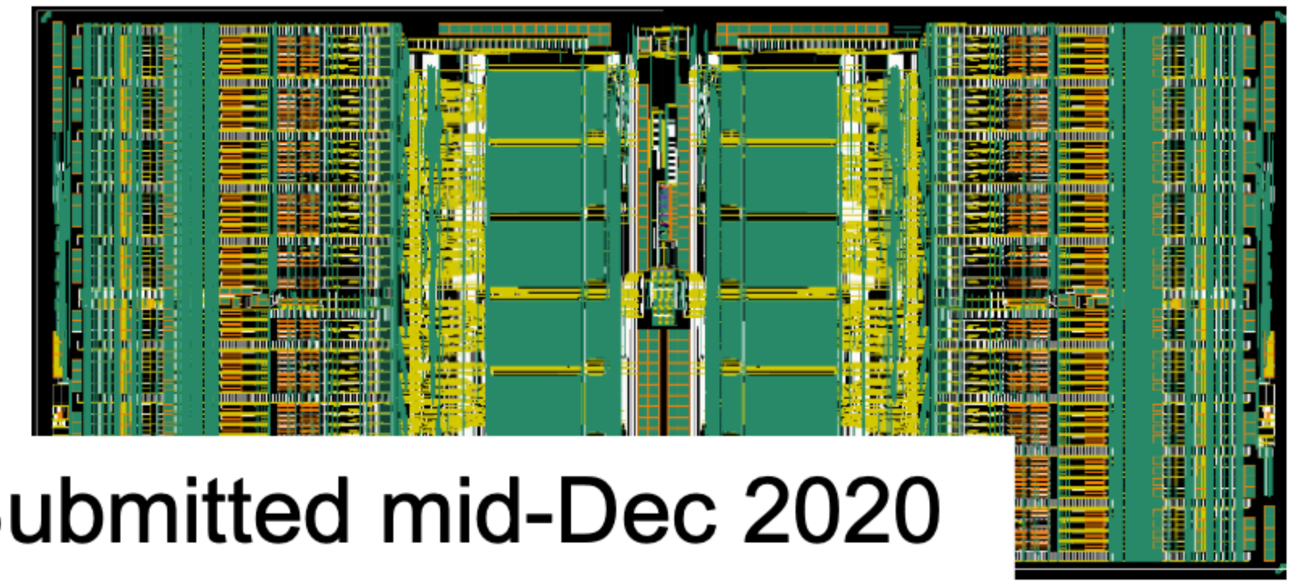
Existing ASIC for CMS, ALICE detectors

Overall chip divided in two symmetrical parts:
- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

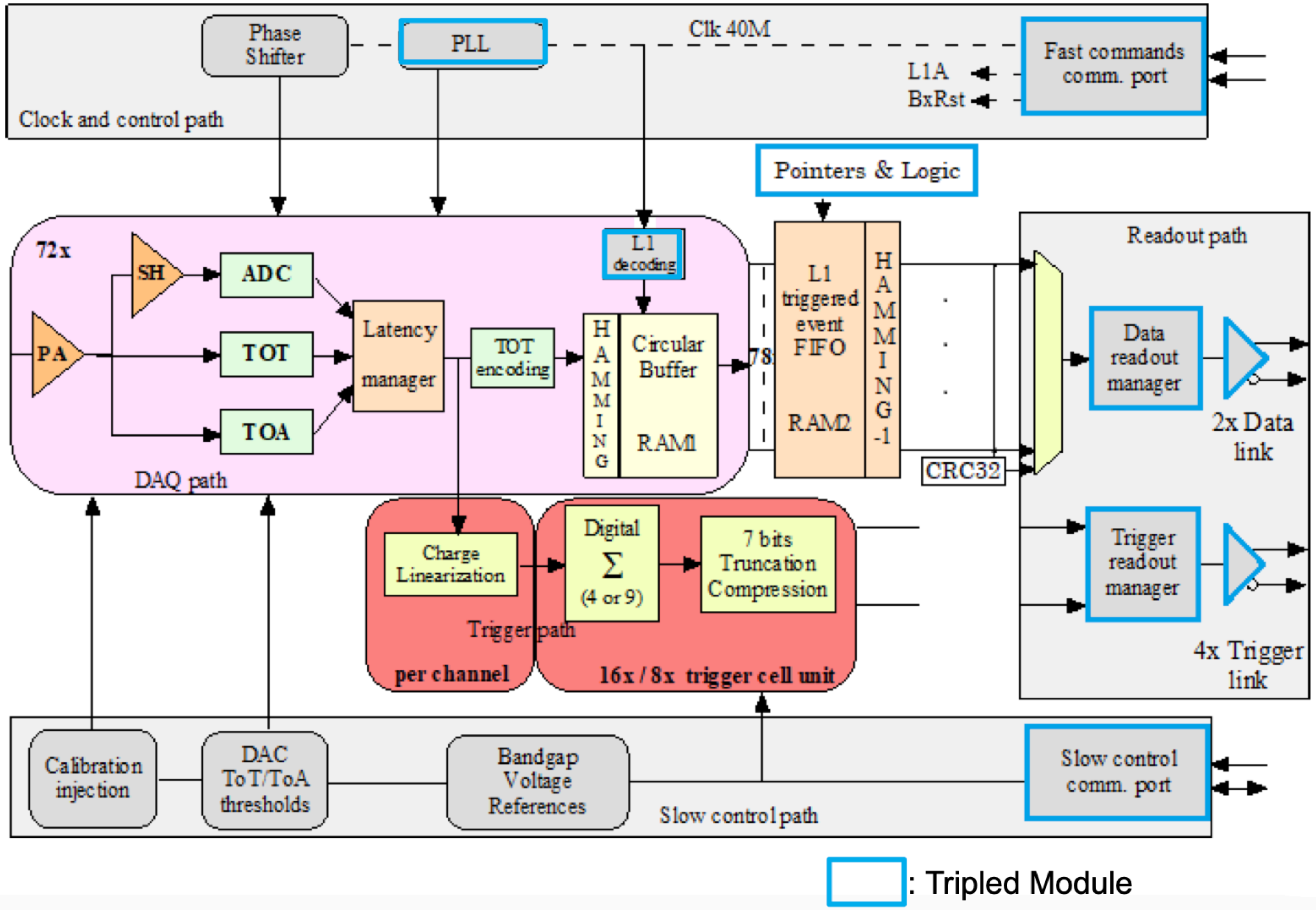
Measurements:
- Charge:
  - **ADC** peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution
  - **TOT**: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - **TOA:** Time of arrival, 10 bits (25ps)

Data flow:
- **DAQ path:**
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- ***Trigger path:***
  - Sum of 4 or 9 channels, linearization, compression to 7bits
  - 4 x 1.28 Gbps links

Control:
- Fast commands, 40MHz and 320MHz clock
- I2C for slow control



Submitted mid-Dec 2020



CALOROC

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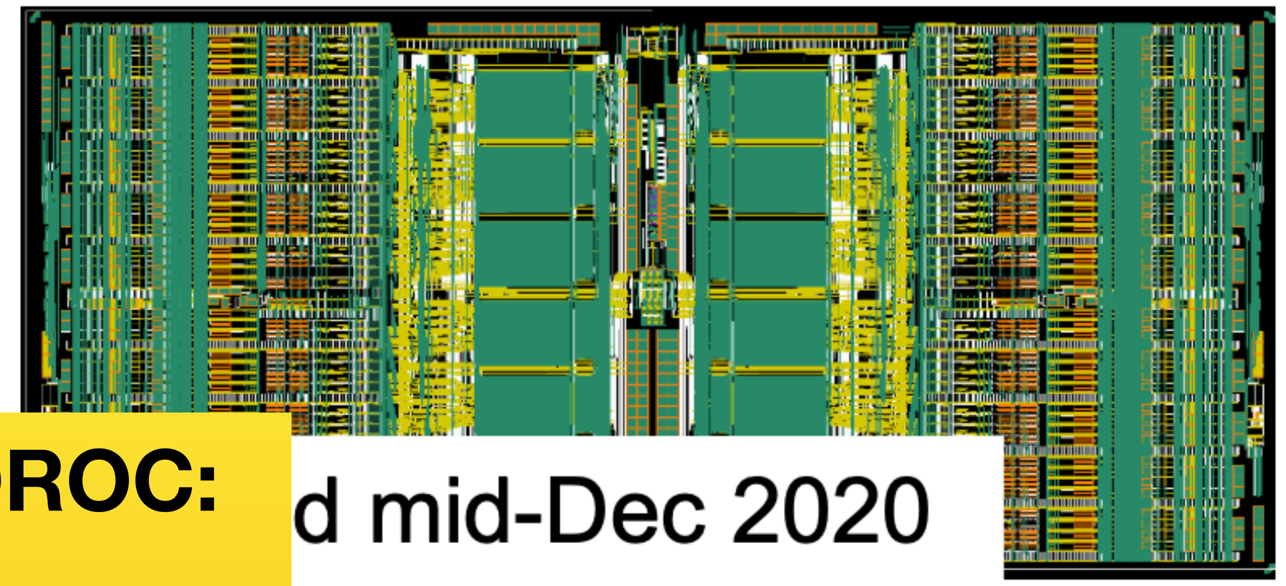

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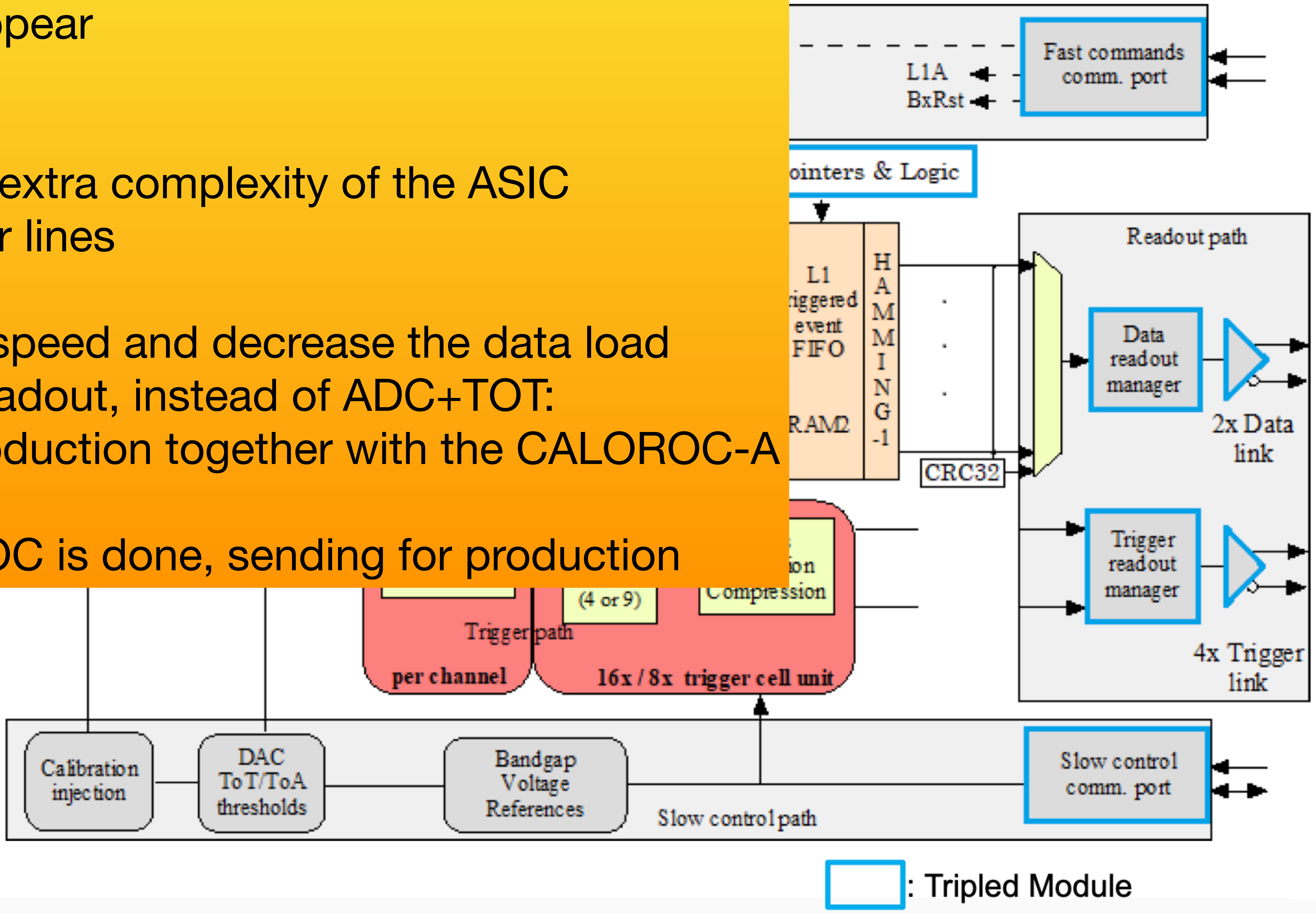
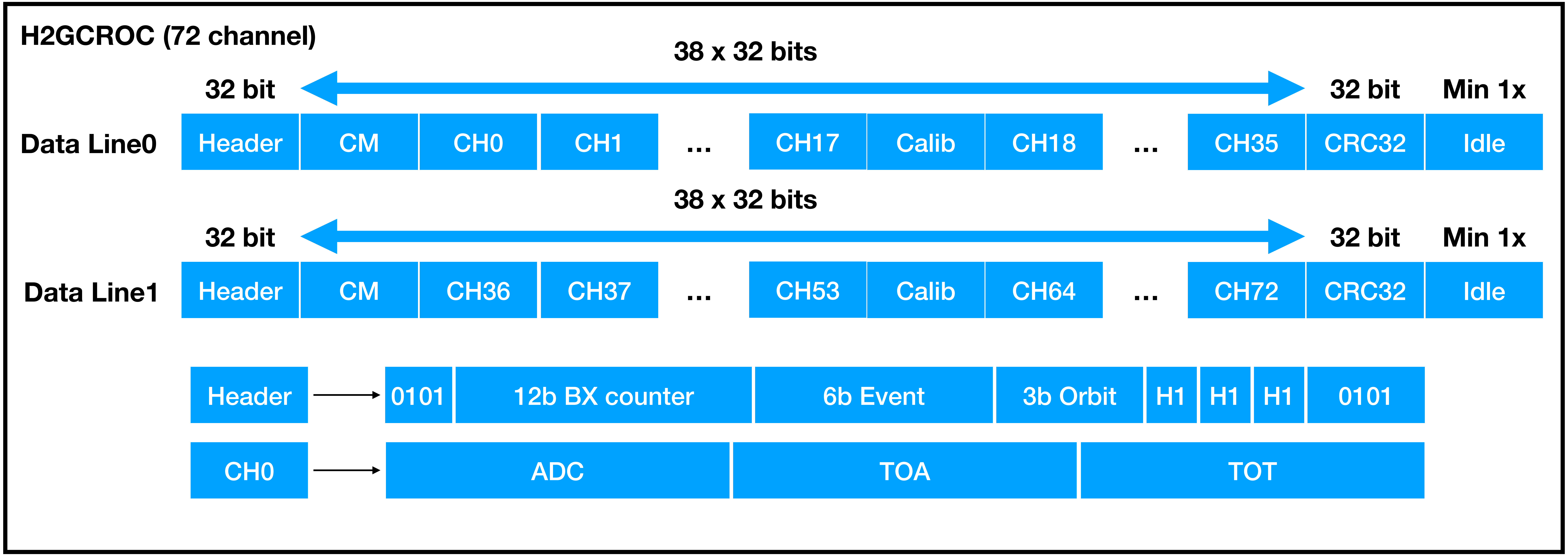


Main changes to the ASIC to apply for the EIC — CALOROC:

1. Self-triggering instead of triggered readout:
   - Trigger lines will disappear
   - Self-trigger on TOA
2. 64 channels per ASIC
   - Reduction due to the extra complexity of the ASIC
   - 4 data lines, no trigger lines
3. Zero-suppression:
   - Increase the readout speed and decrease the data load
4. (Optional) Dual-ADC readout, instead of ADC+TOT:
   - CALOROC-B Test production together with the CALOROC-A

The design of the CALOROC is done, sending for production

H2GCROC Data Format



No zero suppression. The two lines are not independent, they always provide all the data:

- One needs an idle word between the samples (hence 80x32bit on 1.28 Gbps)
- This is one sample in the waveform

Header:

- Always has to start and finish with “5” = 0101 - this changed in 3B, but still constant
- Couple of counters - 12 BX is the 40MHz clock, Event is when received trigger and Orbit counter (these are LHC standards)

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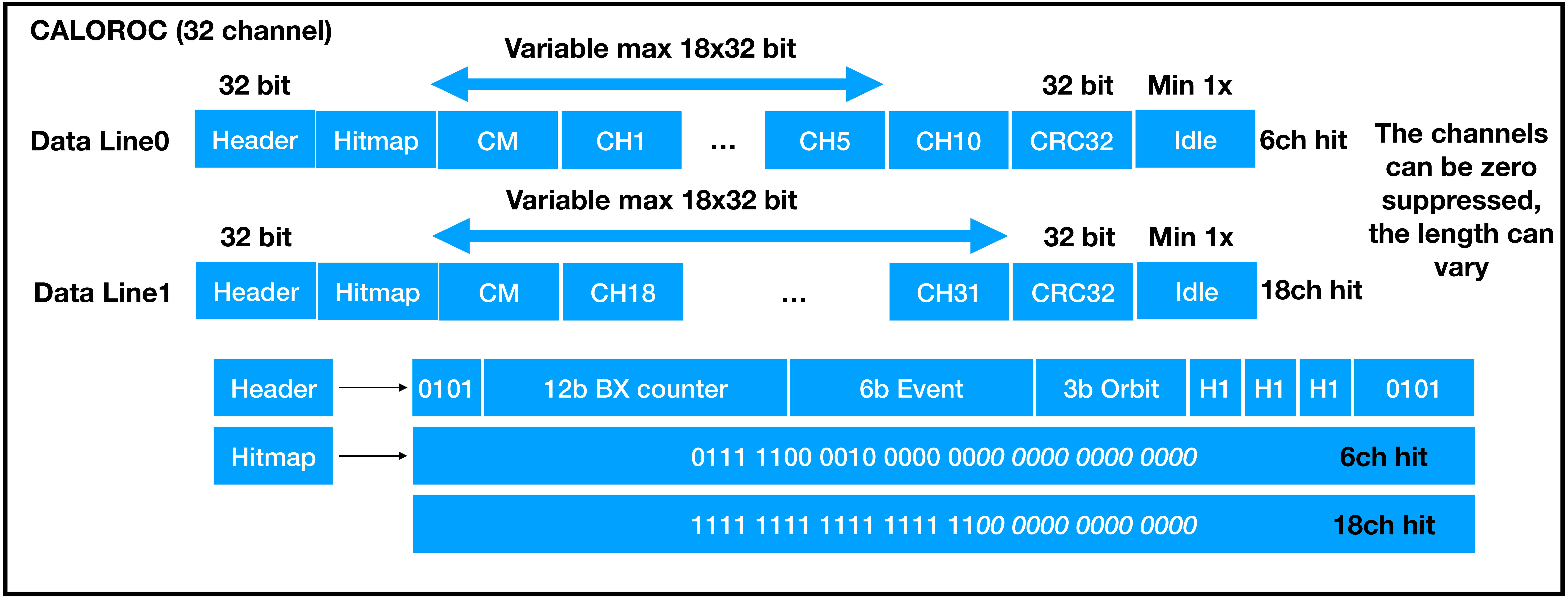
CALOROC data format



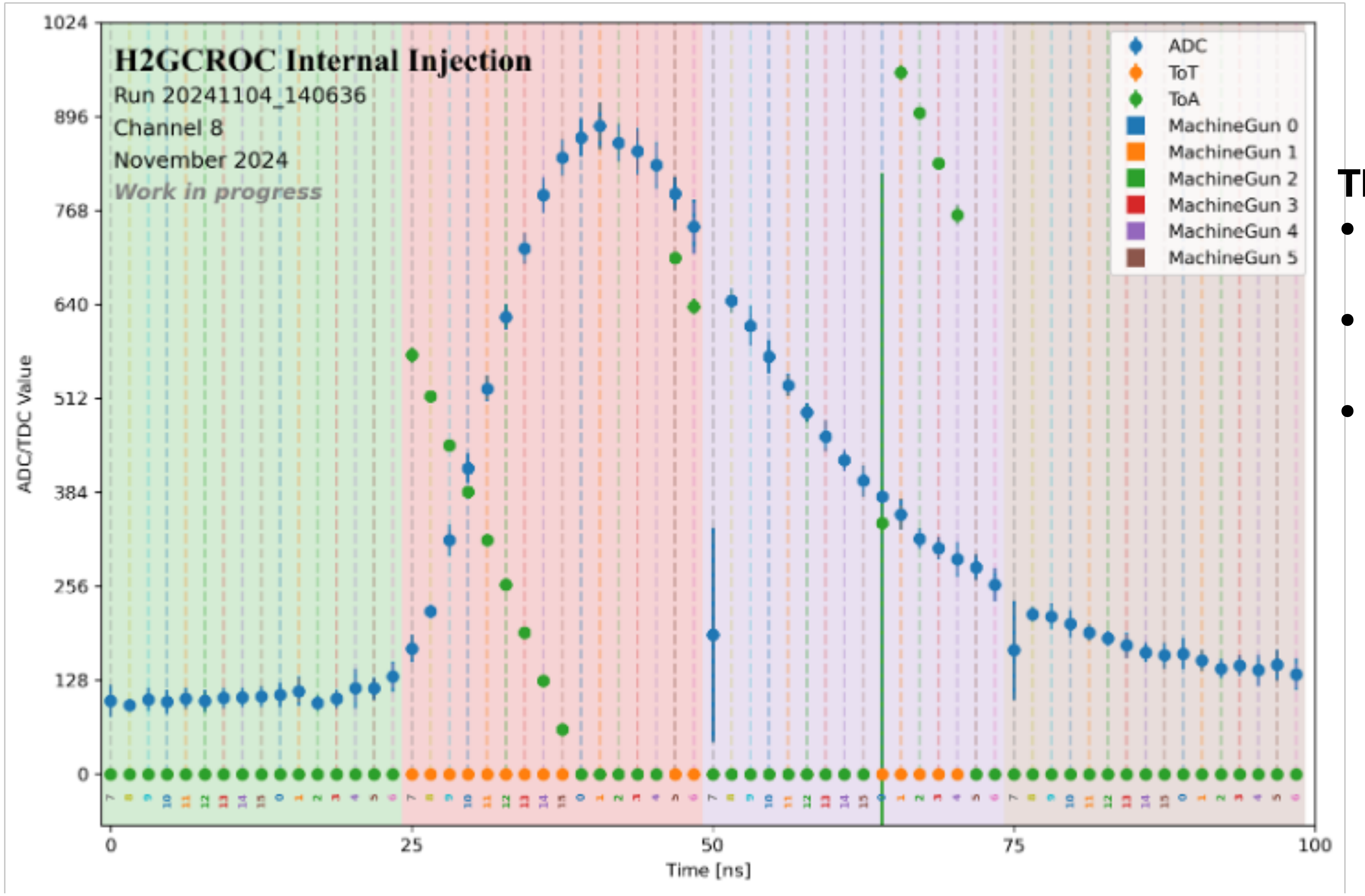
Header is just copy-paste:

- This can be updated

With the zero suppression implemented, it assign a bit to each channel (to map which channel was hit)

- Only 18 channels, but it has 32-bit word (the last 14 bits are unused)

Phase



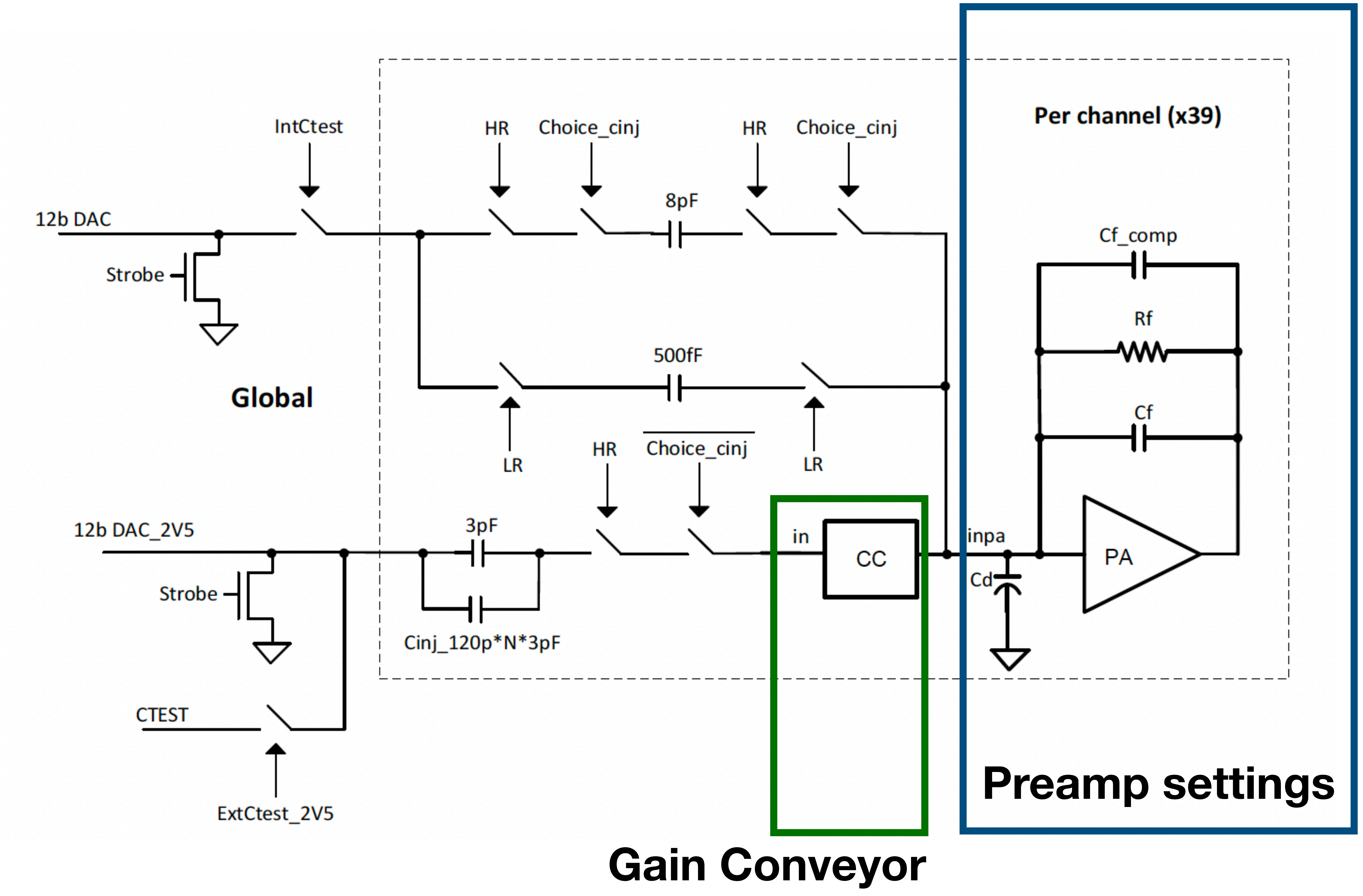
The H2GCROC is running on a 40 MHz clock:

- Input of the H2GCROC is actually 320MHz
- ADC, TOA, TOT are sampled every 25 ns
- There is a variable applied to the whole chip - phase [0-15]. This is a 25/16th phase variance between the clock reference and chip

Key aspects of the H2GCROC

Calibration circuit:

- Internal injection of the ASIC:
  - Low injection:
    - Testing the ADC response, preamp settings
    - Calibrating the TOA
  - High injection:
    - Calibration of the TOT
  - 2V5 injection:
    - Calibrating the Current Conveyor
    - More realistic shape response



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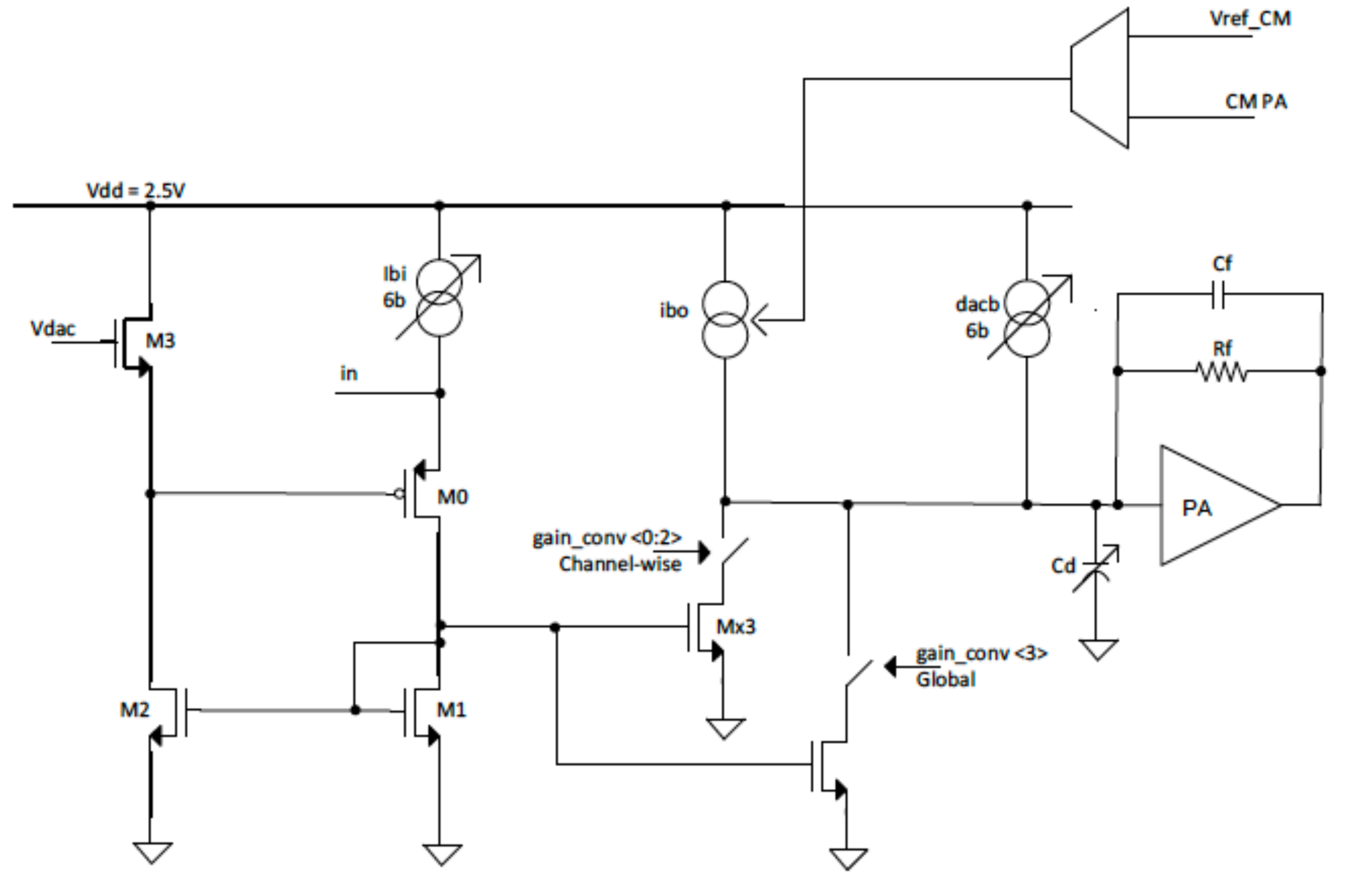
Gain Conveyor



3.2 "Channel-wise" I2C parameters

6	gain_conv<0>	"0"	Conveyor Gain: <0> = 0.025, <1> = 0.05
7	gain_conv<1>	"0"	
7	gain_conv<2>	"0"	Conveyor Gain: <2> = 0.1

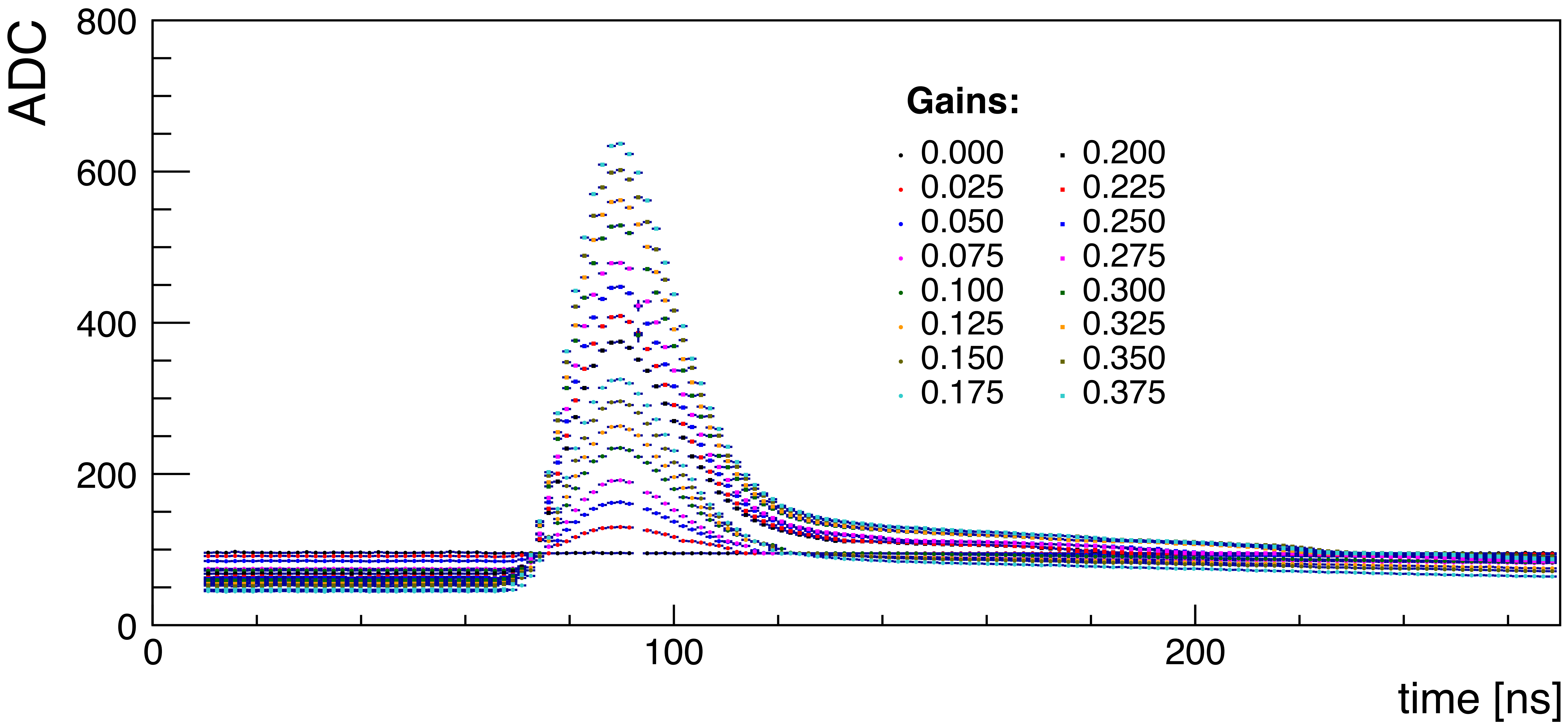
3.3 "Global analog" I2C parameters

7	gain_conv	"1"	Conveyor Gain: <3> = 0.2

There are 4 bits to setup:
- 3 of them are settable channel-by-channel
- 1 of them is global

The range of the same injection value with different gain settings

16 different settings are possible, full phase scan was performed



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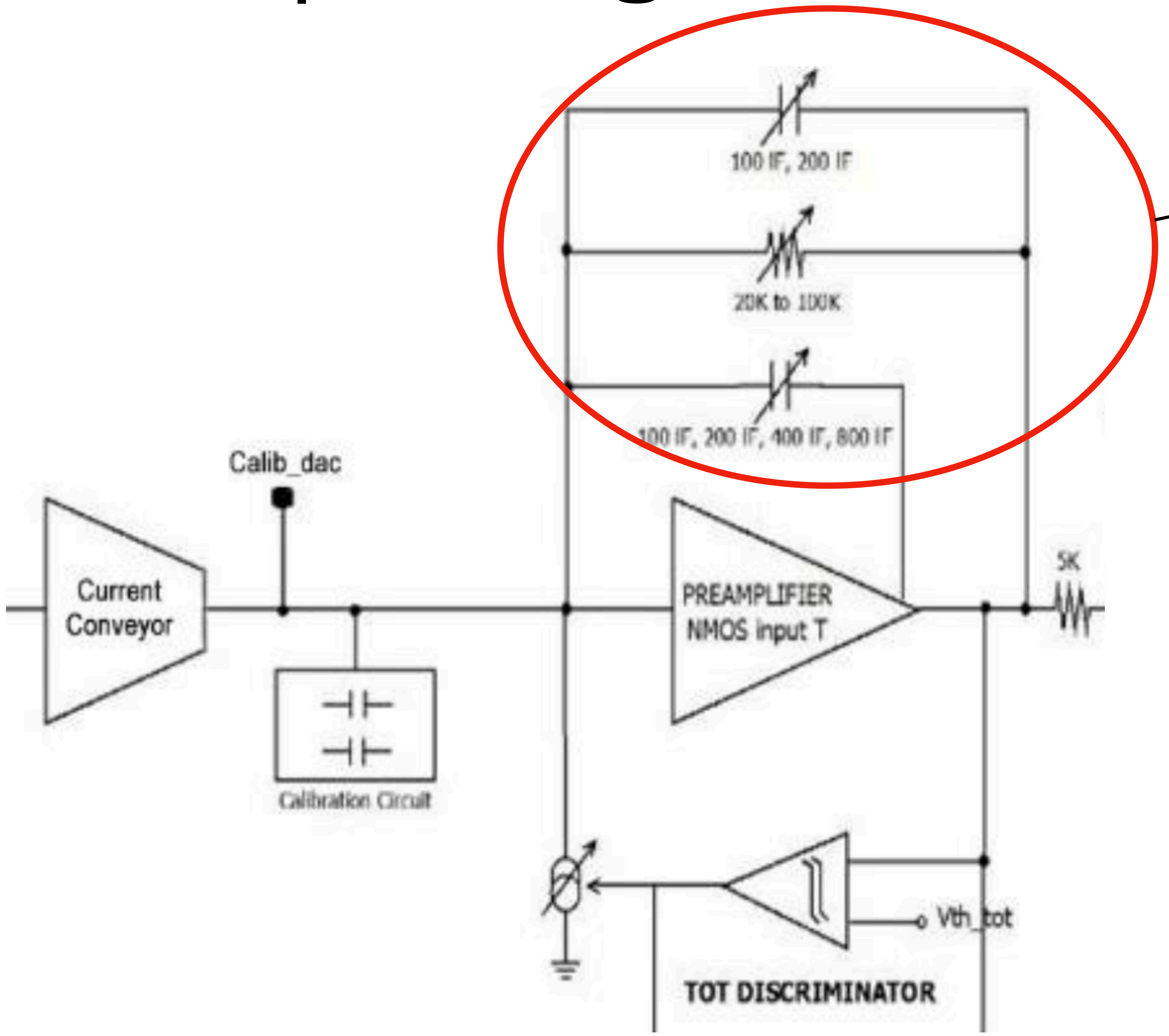
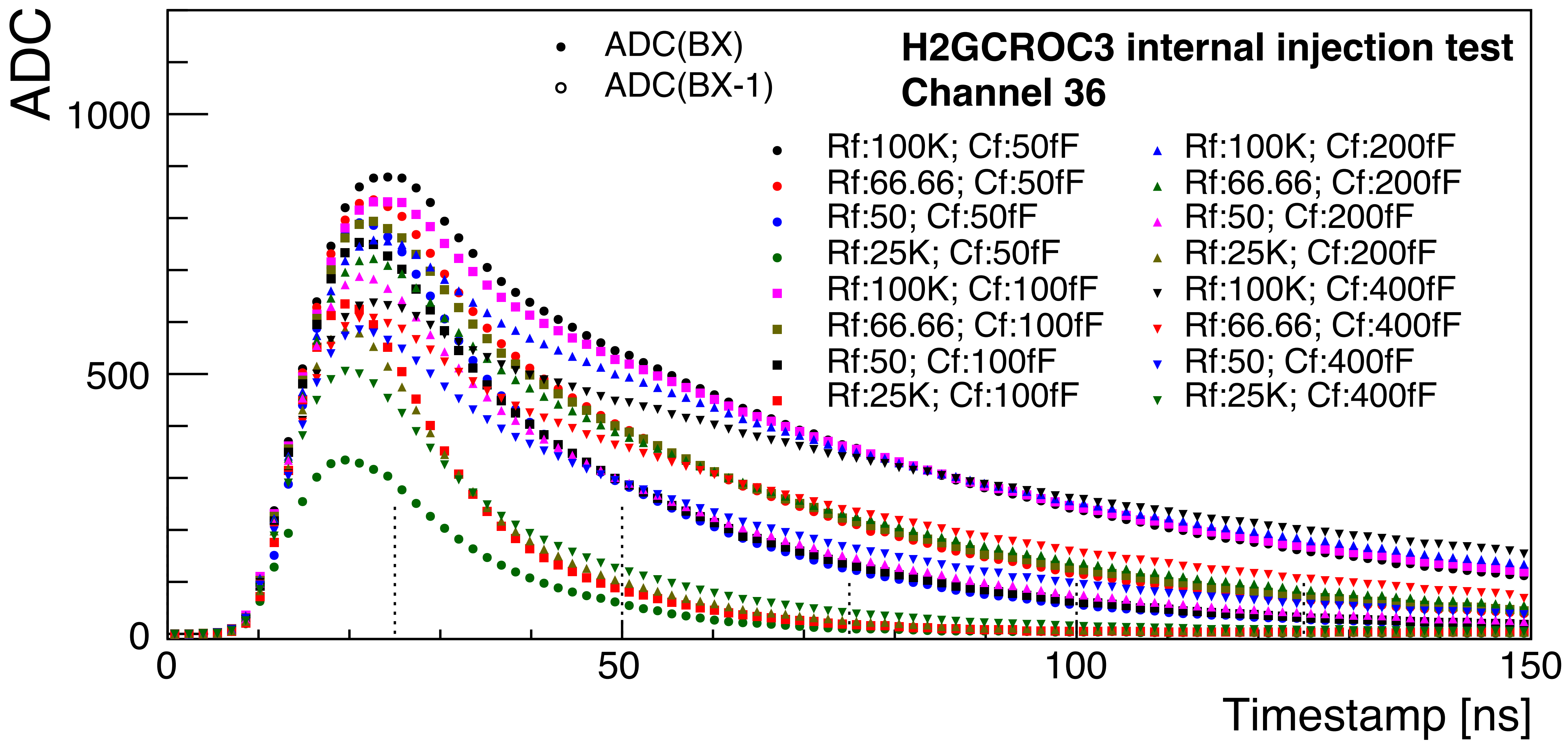
Pre-amp Settings



Cd (pF)	5, 10, 20	At the conveyor output and at the preamp input. To ensure the preamp stability.
Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50, 100, 200, 400	Same purpose than Cf capacitors but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table 1.1: Values for Rf, Cf and Cd

Same injection in the same channel



Pre-amp gains can be changed in the ASIC anytime, built-in setup can be further tuned to our needs (EIC)

With the quick test, 16 different gains were explored:

- Dynamic range can change a factor of 3!
- More setups can be added

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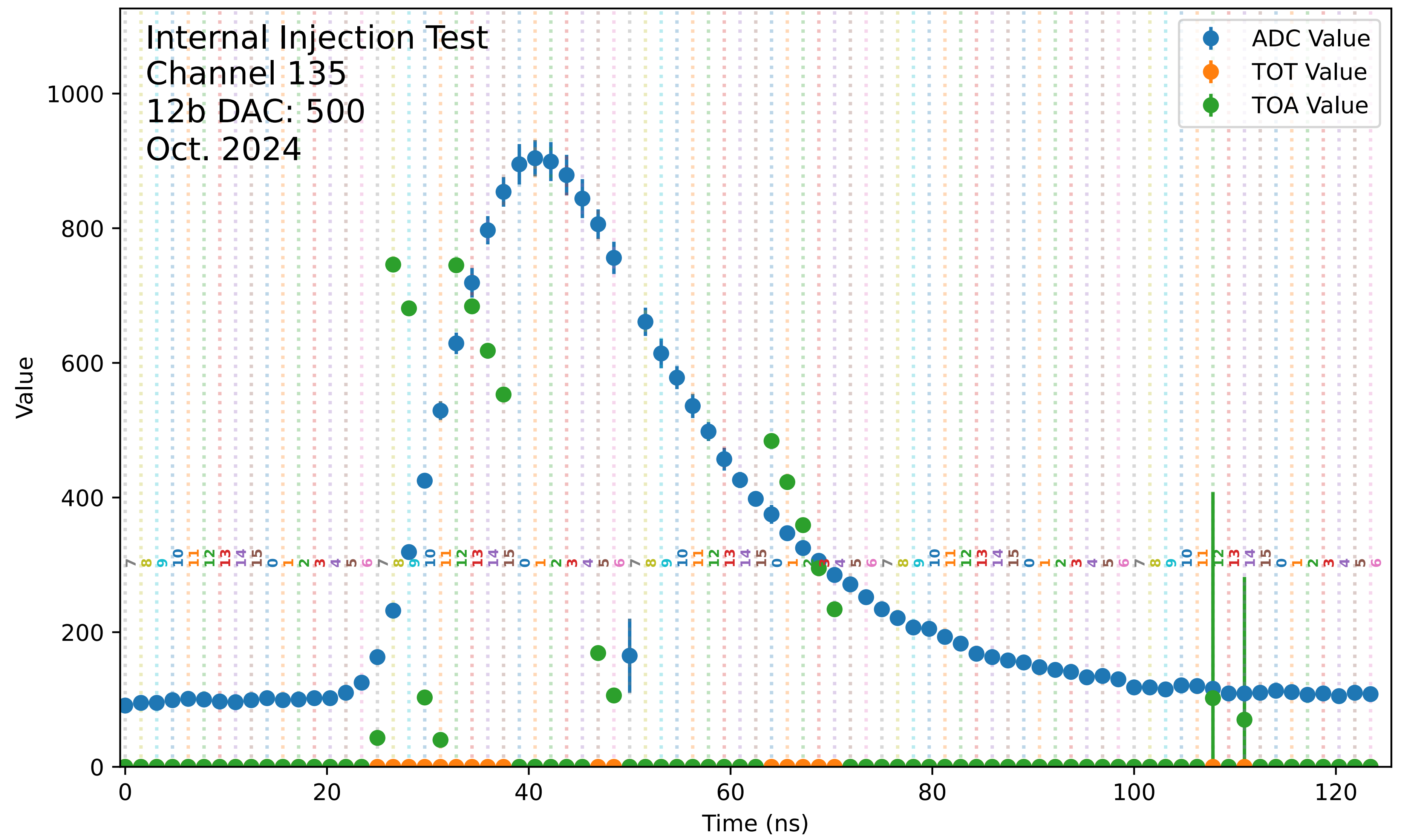
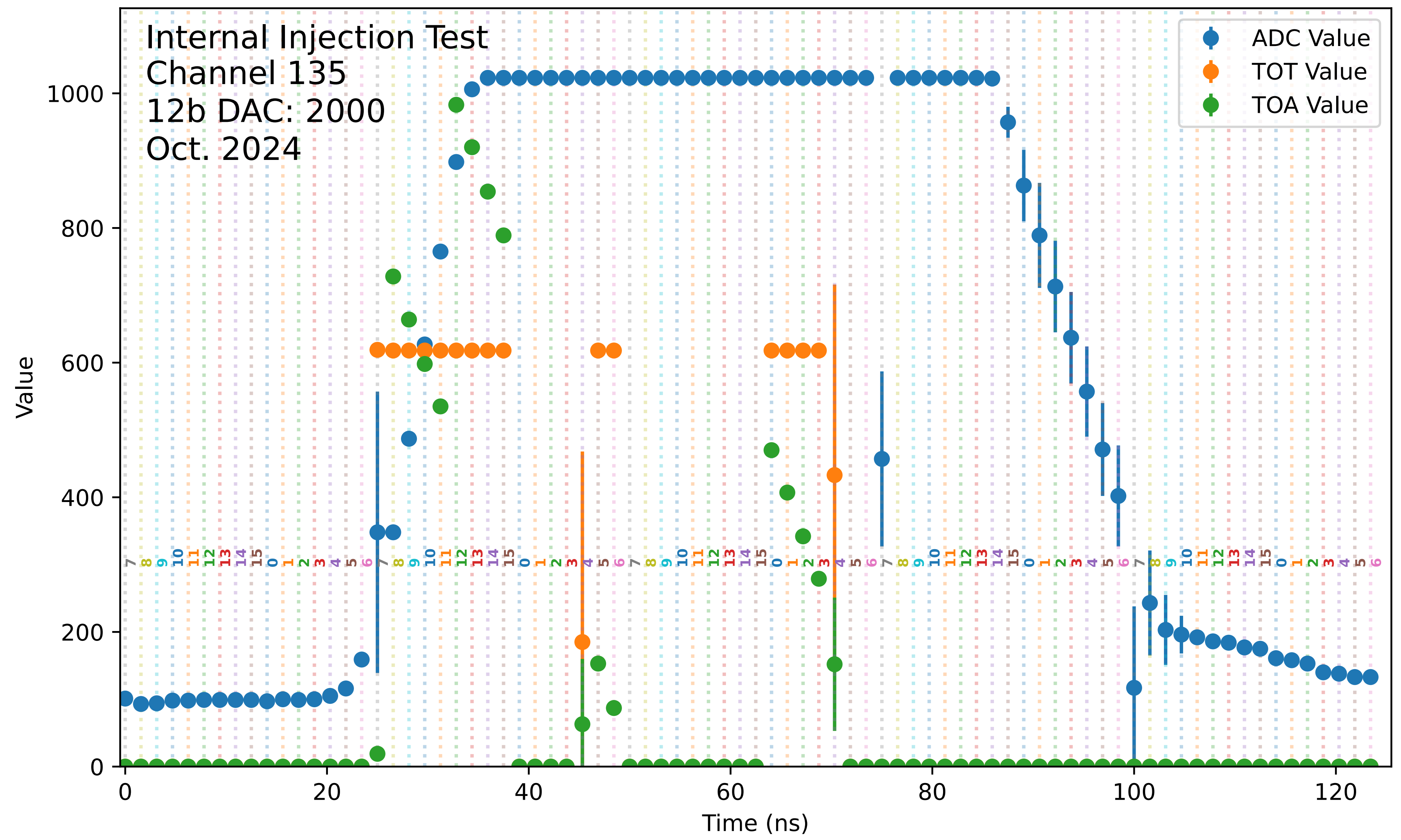
Internal injection and TOA





DESY test by Shihai Jia

It appears for clock phases 0,1,2,3,4, the ToA and ToT values will shift by one bunch crossing

- Structure stems from each TDC being composed of 3 stages:
  - 2-bit grey counter LSB ≈ 6.25 ns
  - Coarse 5-bit TDC LSB ≈ 200 ps
  - Fine 3-bit TDC LSB ≈ 25 ps

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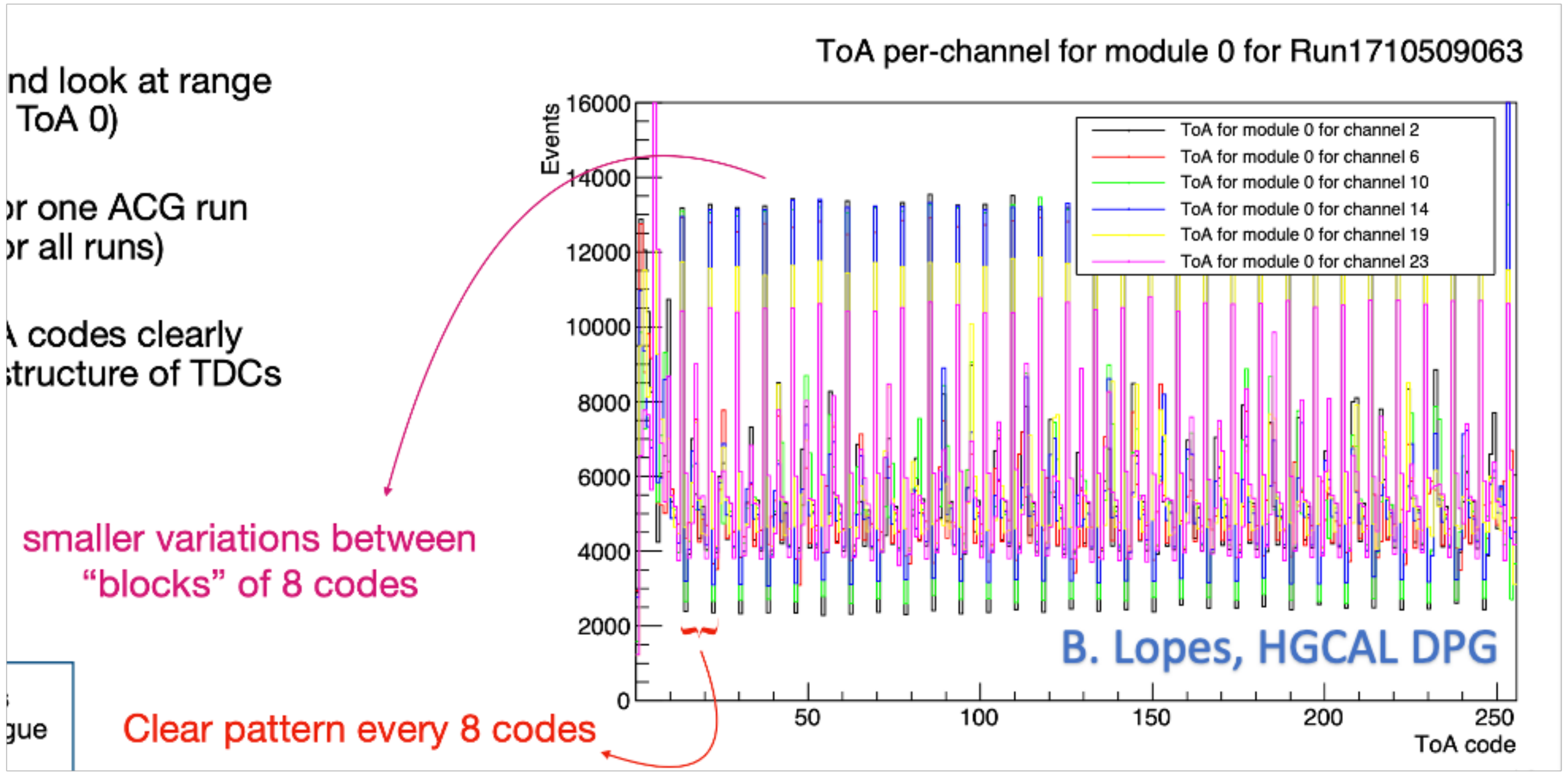
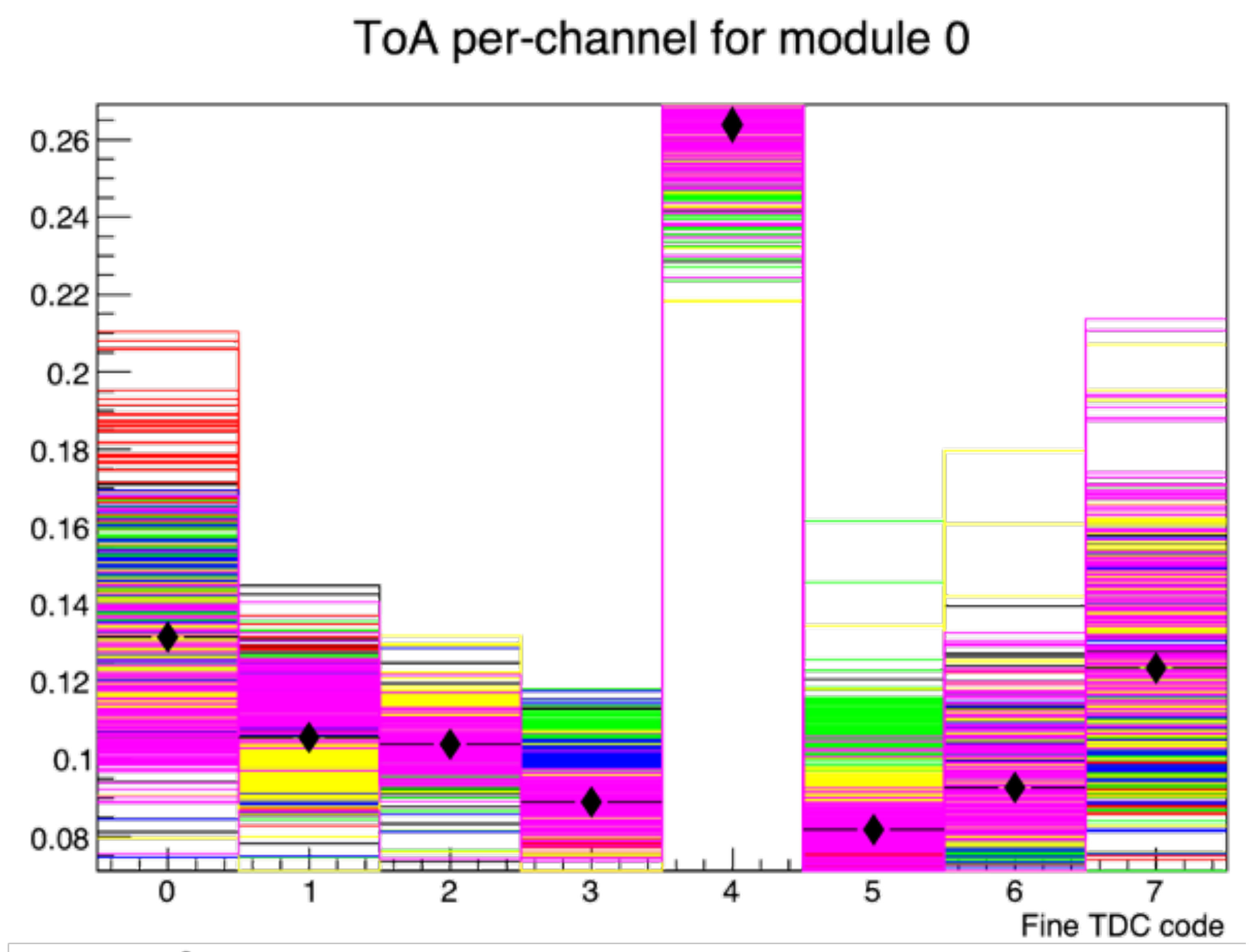
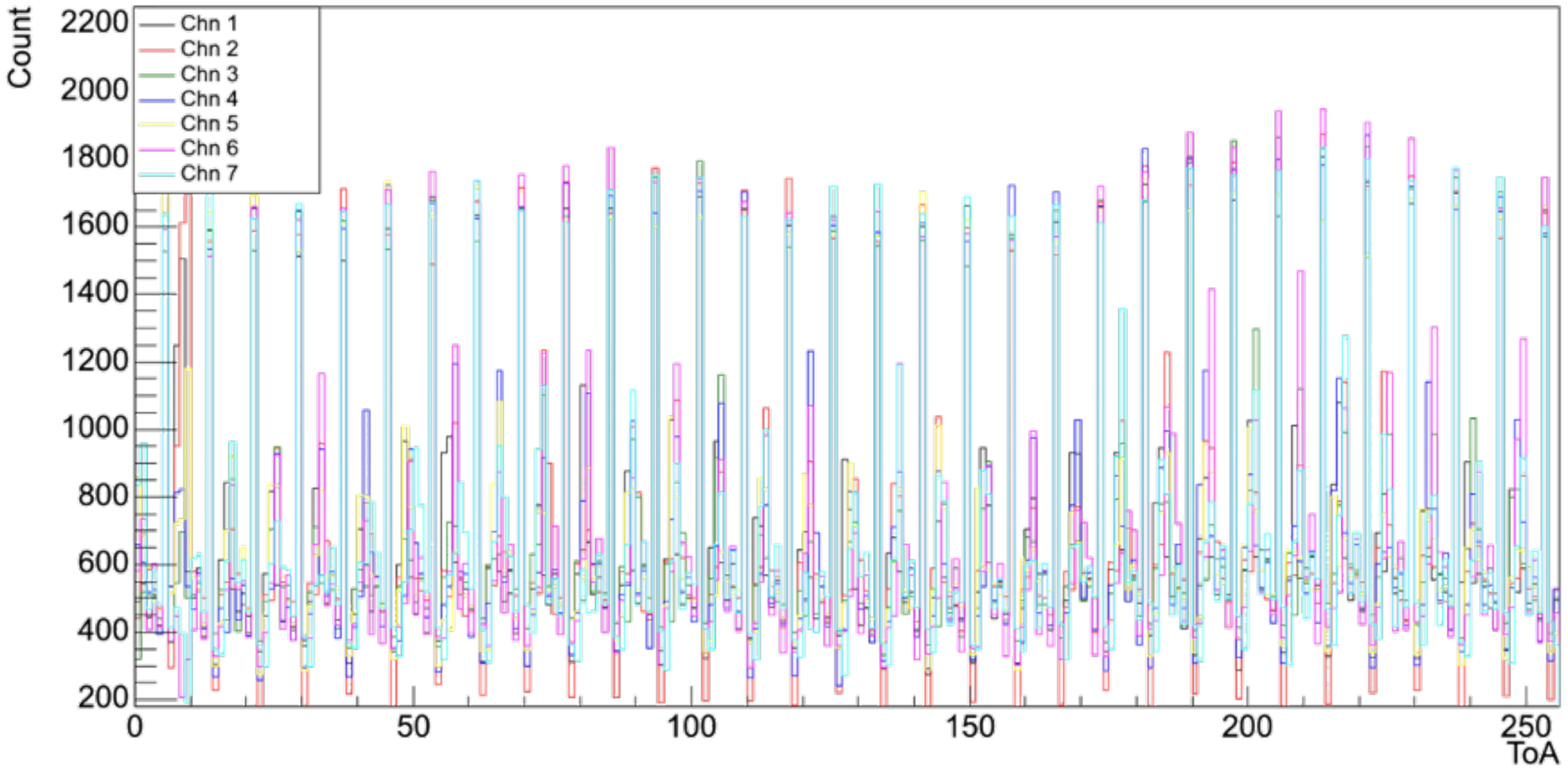
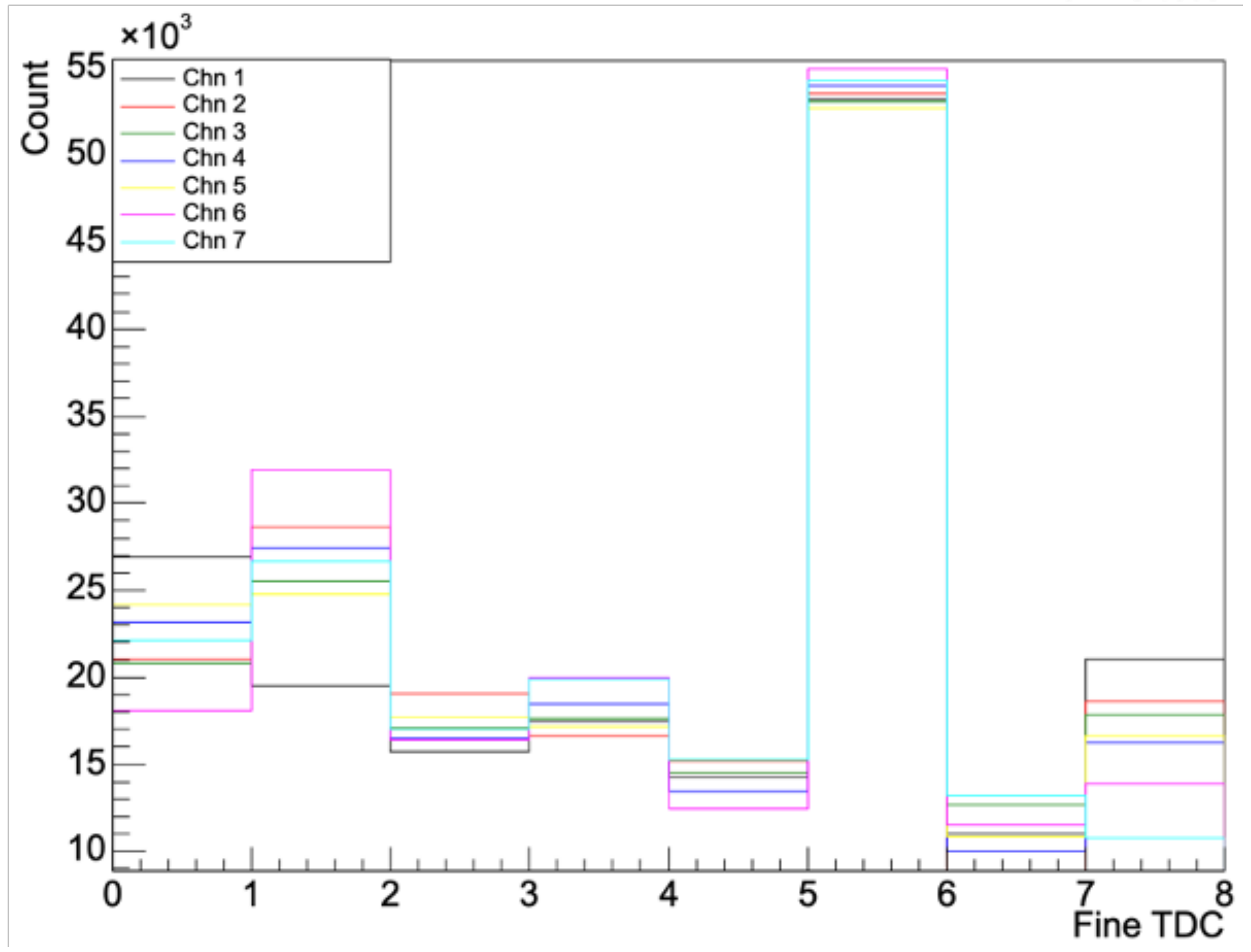
ToA calibration – fine TDC

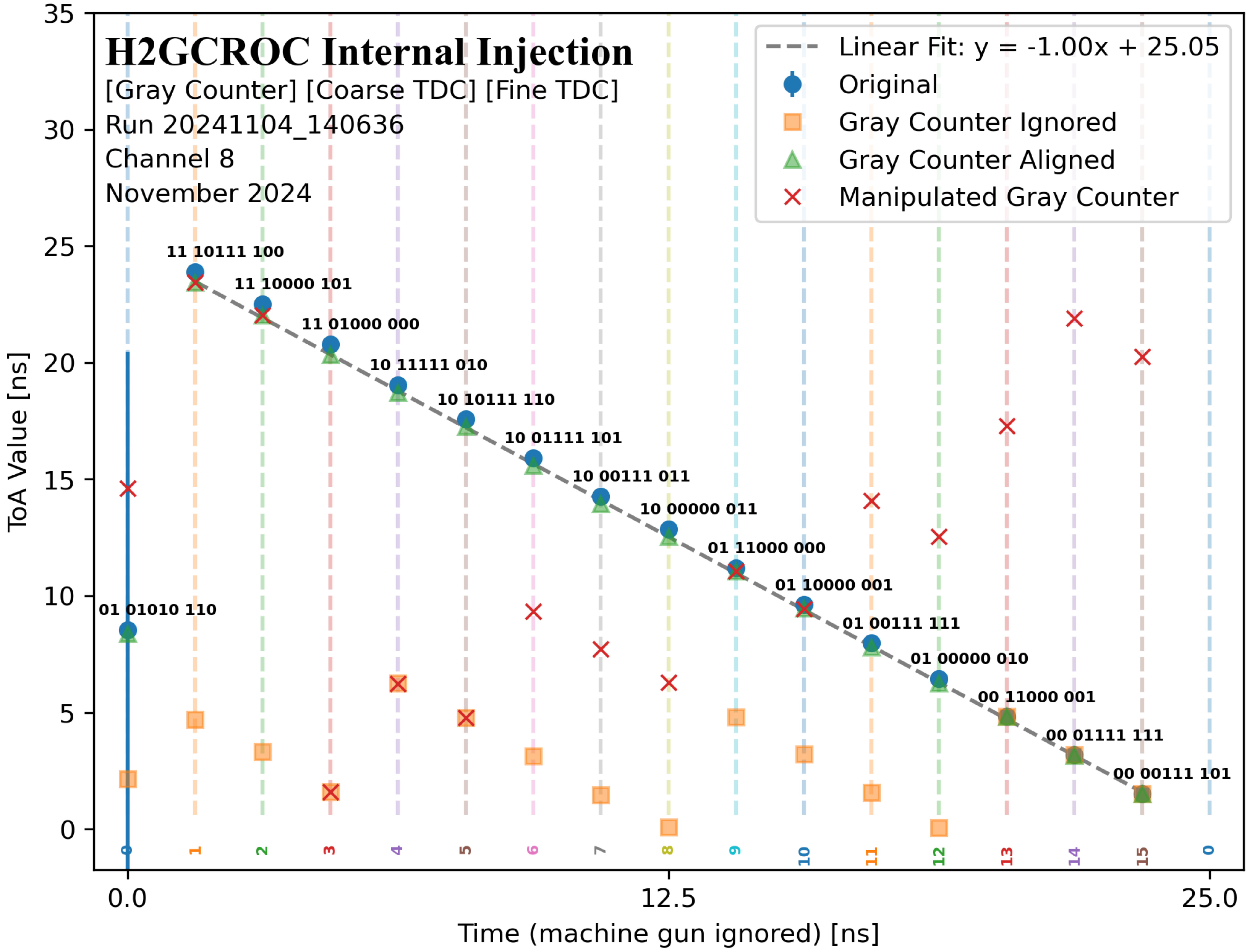






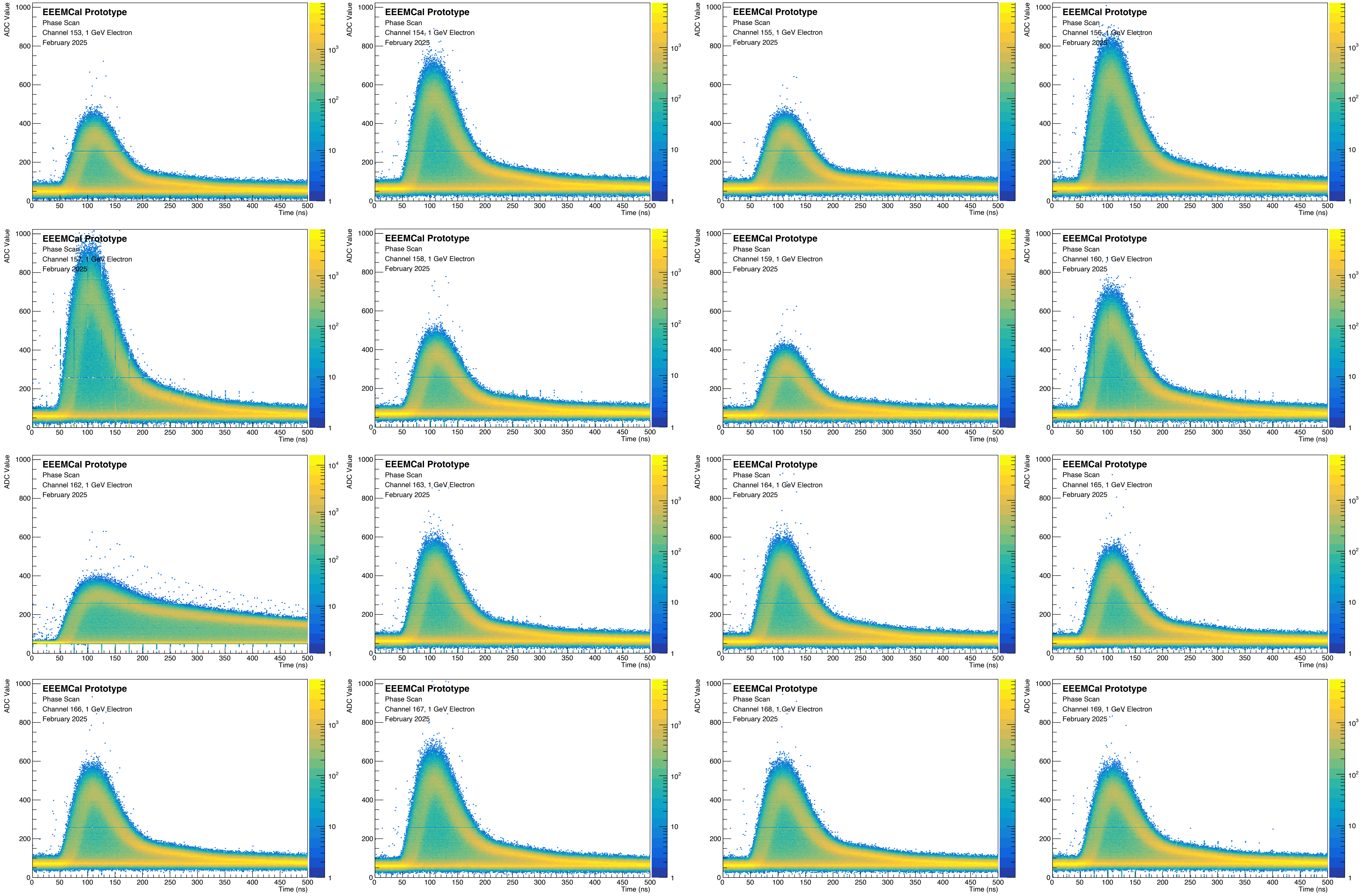


Calibrated TOA

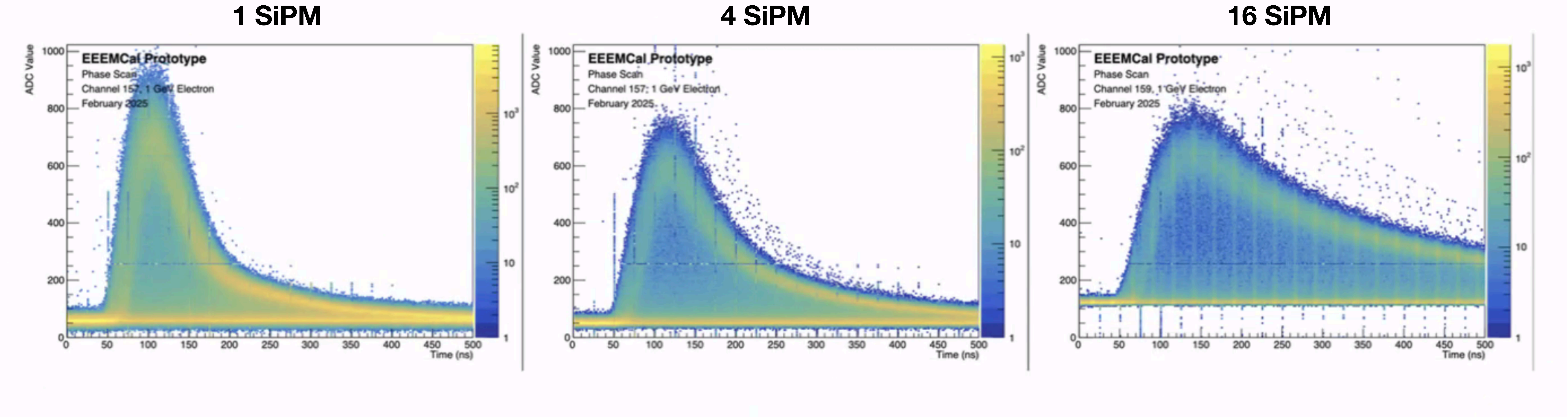


Very linear response once they are all calibrated well

EEMCal data (few channels, single SiPM [3x3mm2])



Different SiPM inputs



The first try was to connect the SiPM's in parallel (adding the capacitance):

- The SiPM signal is reconstructed, but it gets much more wider
  - TOT saturates at 200ns, so it would saturate much quicker in 16-SiPM connection
  - CALOROC1B will be a dual-ADC readout chip

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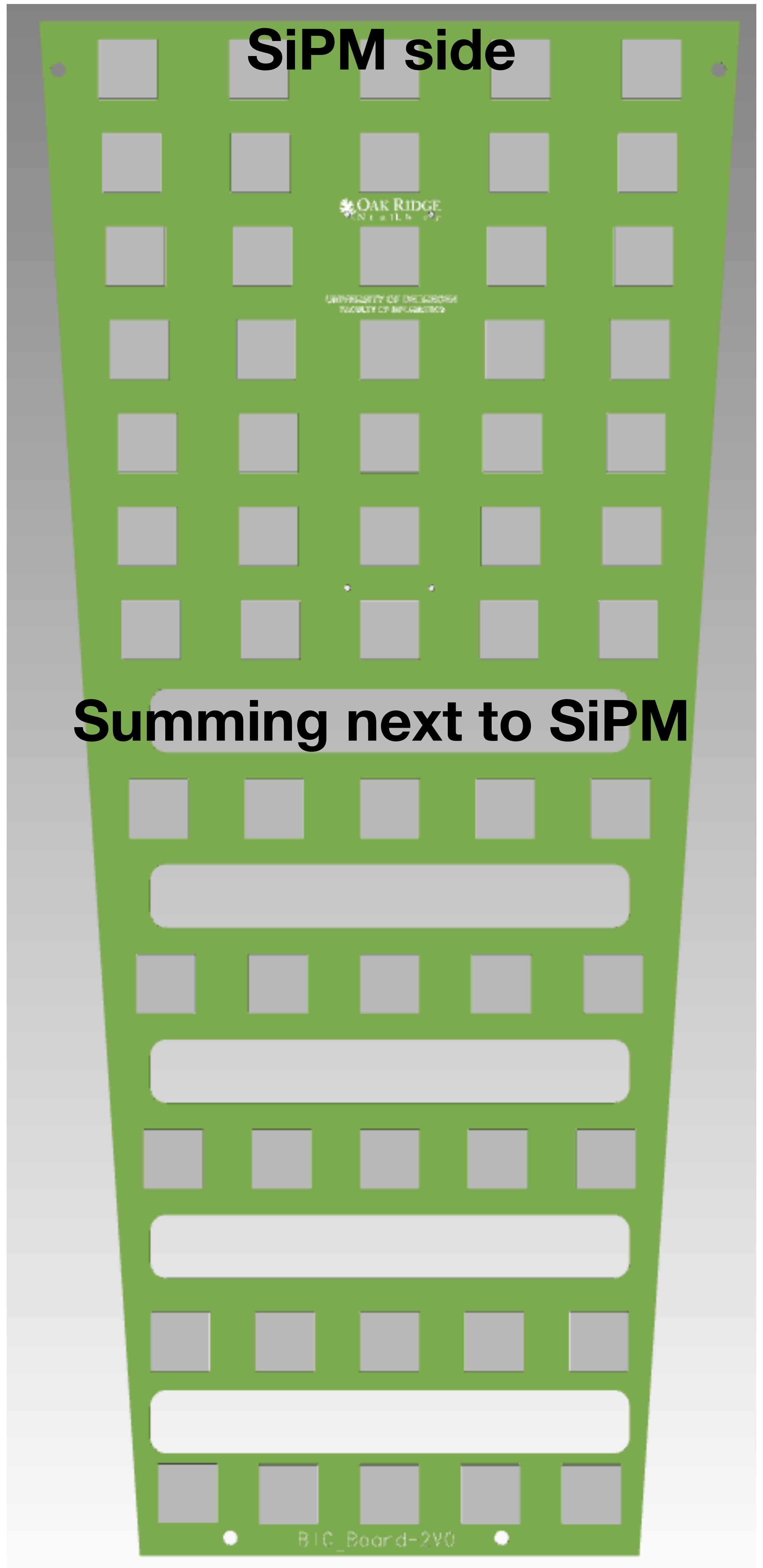
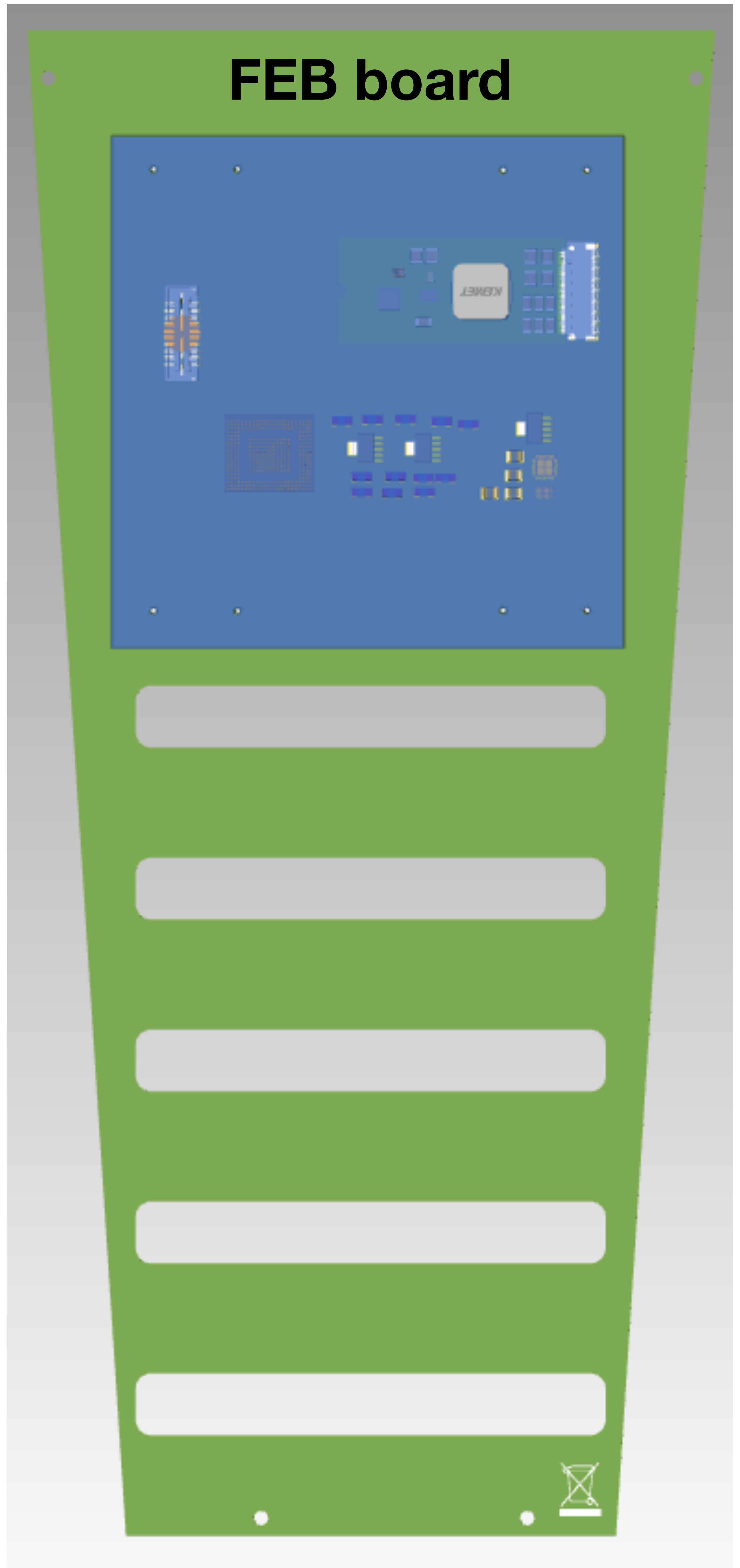
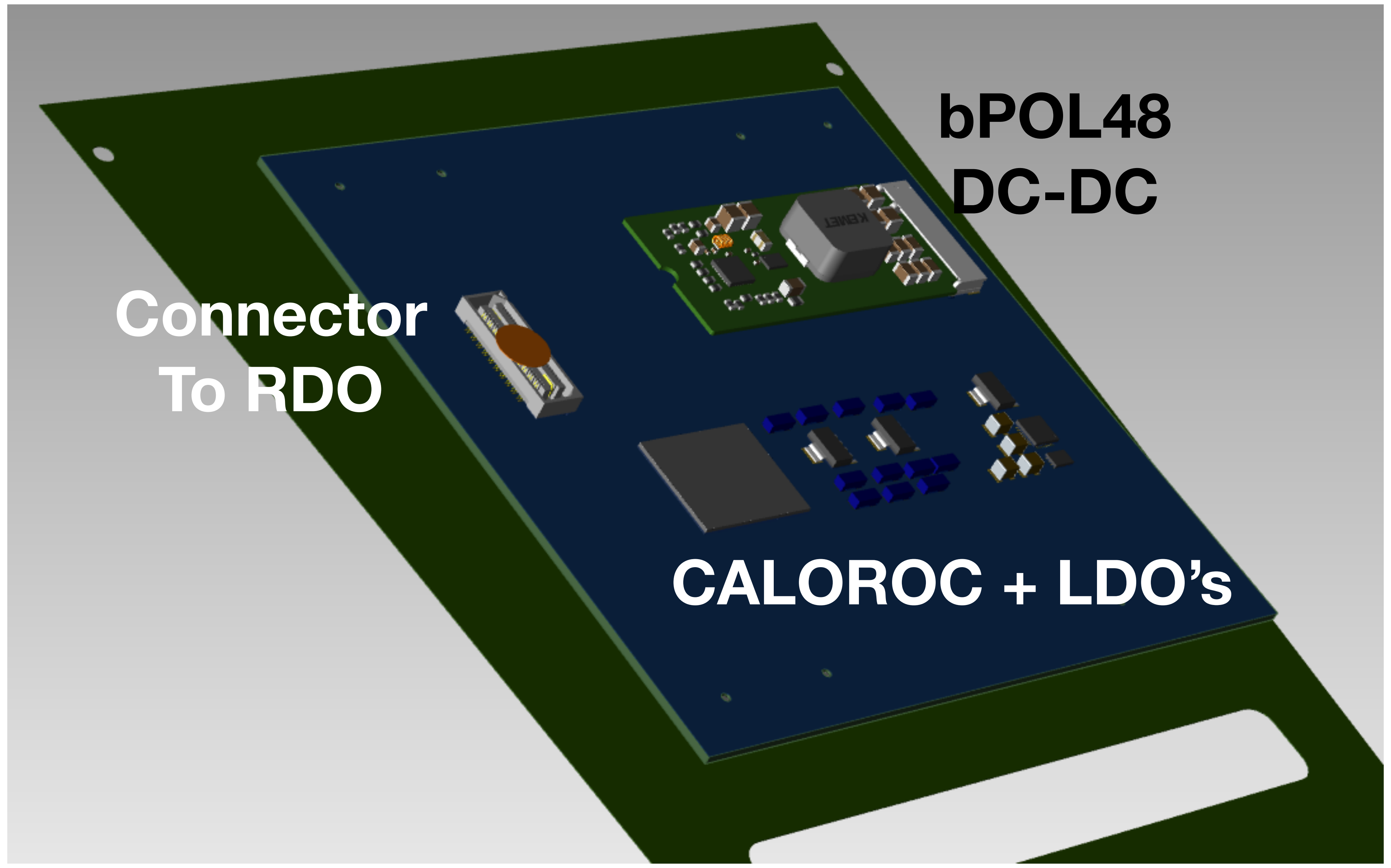
Front-End Board, first approach







Preliminary design of the FEB board:

- Implementing realistic geometry:
  - This can change according to requirements
- Cooling option between the SiPM board and FEB:
  - Keeping the SiPM's on constant T
  - Backward line could provide additional cooling for electronics
- Summing board on SiPM:
  - If it is passive, not generating additional heat
- Lot of real estate available:
  - Possibility to put another DC-DC to provide power to AstroPIX ETC board, etc.

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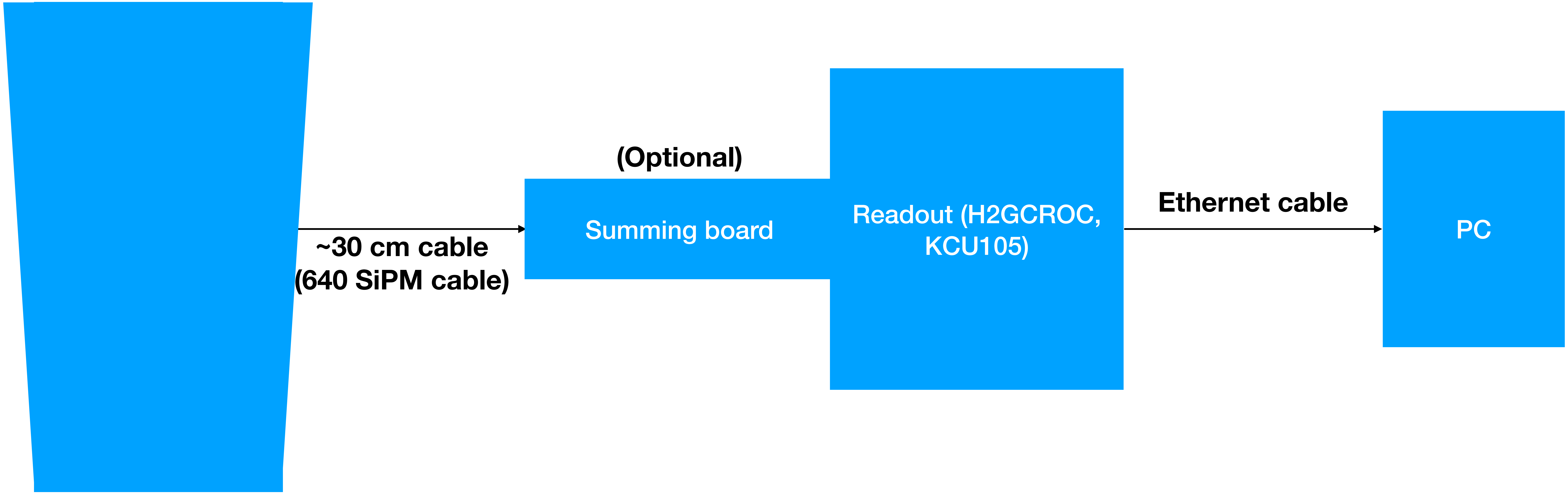
BabyECal testbeam effort - Effort



The suggestion for the testbeam effort:

- Have one board with SiPM only, nothing else
- Modular summing board (active, passive, all ideas can apply here)
- Readout:
  - Step 1 - readout every SiPM alone. 640 channels, that's only 10 chips.
  - Step 2 - find the best summing scheme

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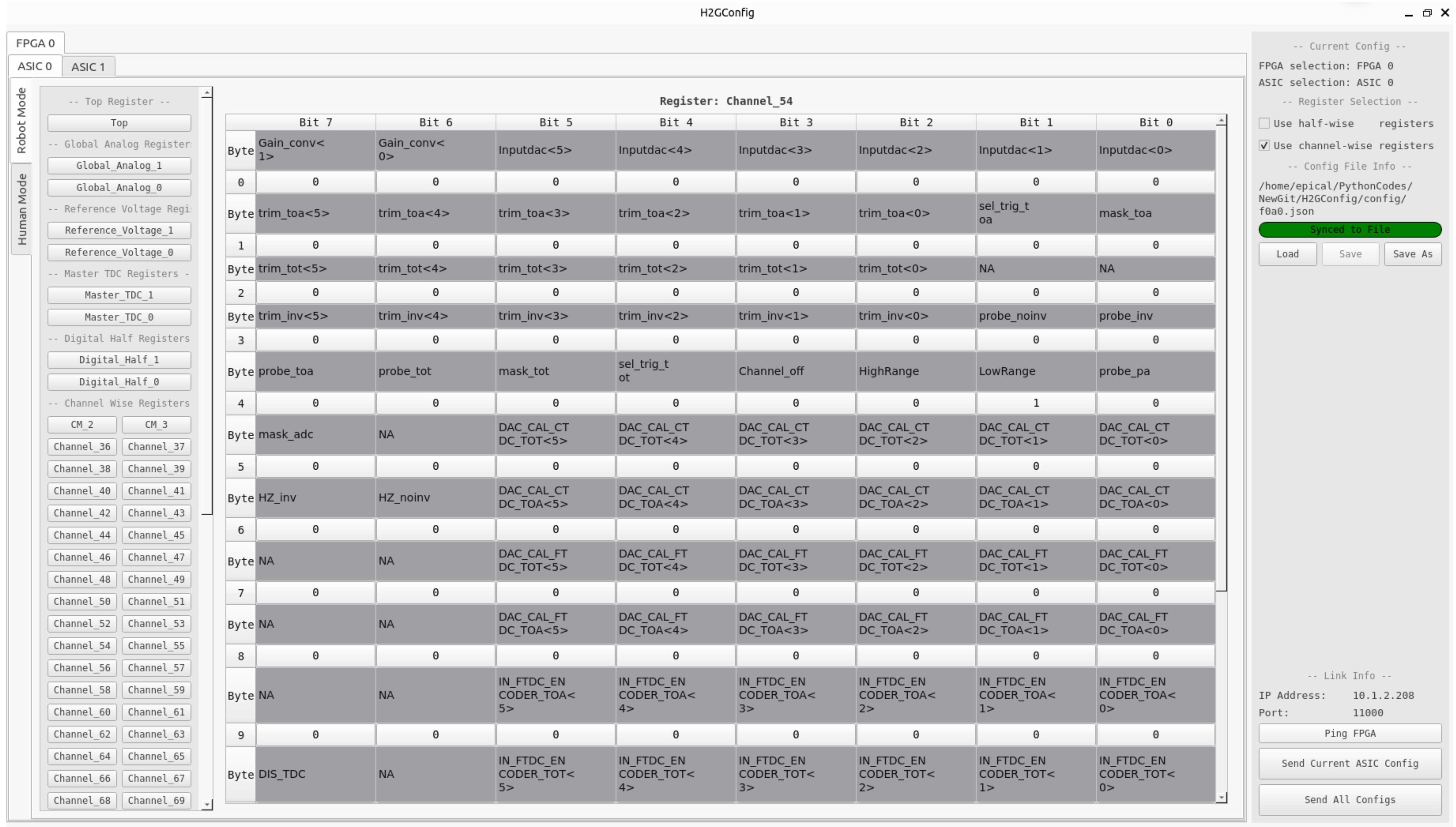
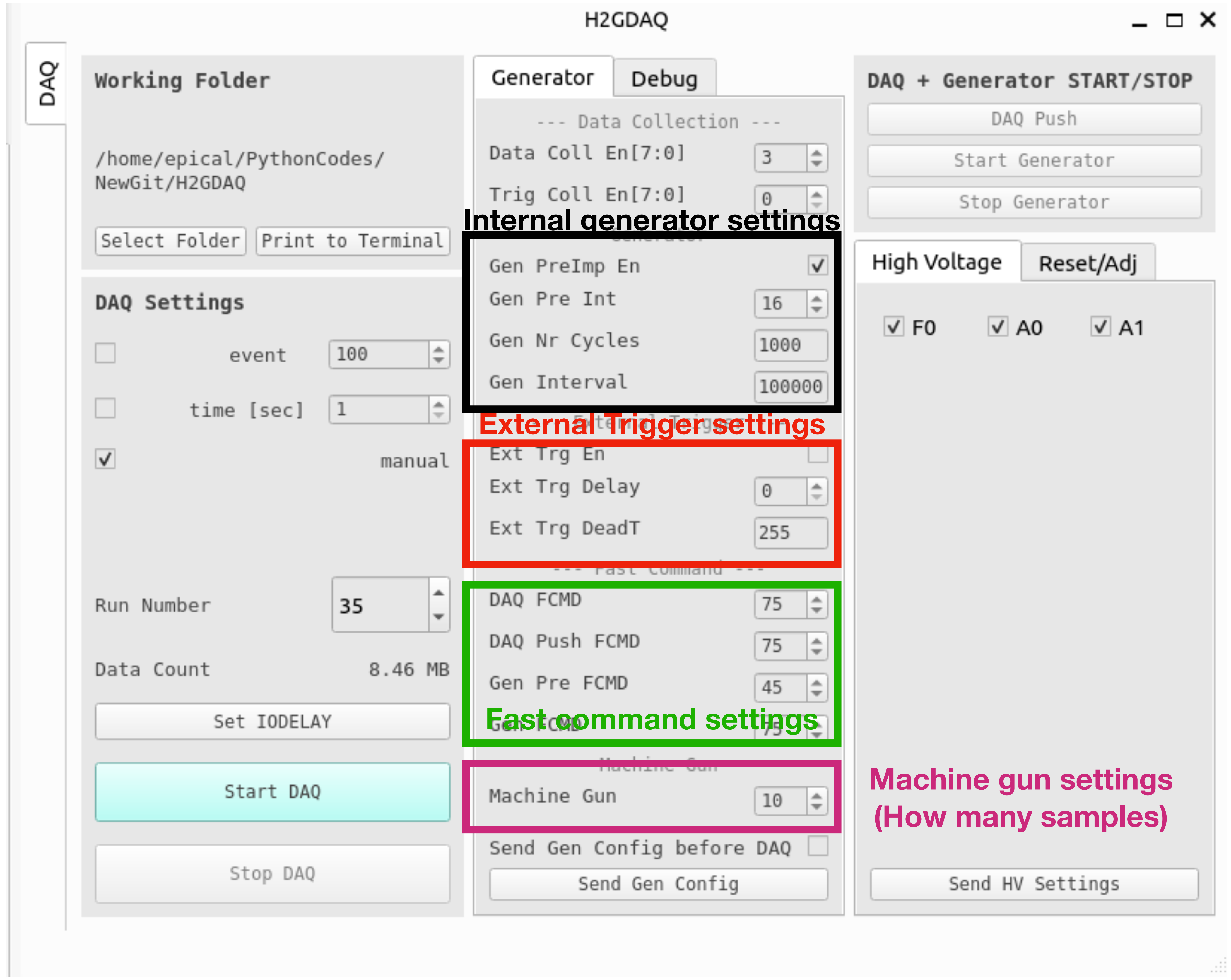
Software



Slow Control for the H2GCROC:
- N FPGA with 2 H2GCROC setup (1x2 in this case)
- All registers are settable and working



DAQ is very simple:
- File or terminal dump
- Generator settings - all in 40MHz
- External trigger
  - Ext. trigger delay - needs to avoid the UDP packet loss
- Daq push - 1 event
- HV on/off for the board
- Adjustment if there is a misalignment, debugging

Need to develop a fast calibration code which will enable fast settings of the ASIC

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Summary

Rapidly progressing with the prototype readout with the H2GCROC:

- We have now 6(blue)+10(green) protoboards with 32 chips available 2048 channels in total
- Firmware + software already available
  - Understanding the gain and preamp settings better
  - TOA calibration is better and better understood
  - Working on the summing boards
- We need to progress towards real readout tests:
  - We need a test with BIC prototype
  - This is giving feedback back to change settings on the CALOROC as needed
- End of the year:
  - We will get ~2x180 CALOROCs by end of the year
  - We are also working towards the RDO boards

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