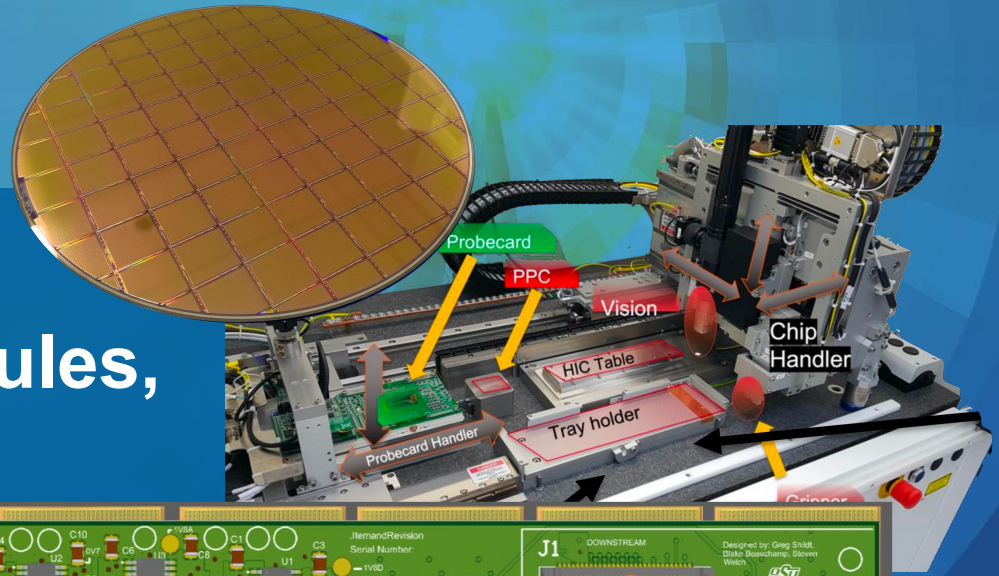
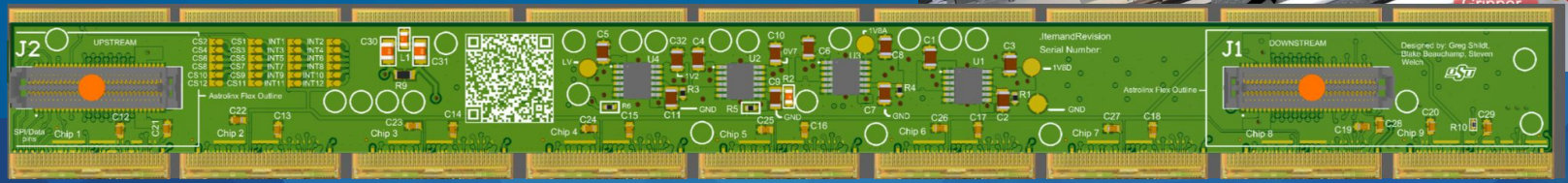
The ePIC Barrel Imaging Calorimeter

AstroPix Wafers, Modules, and Staves



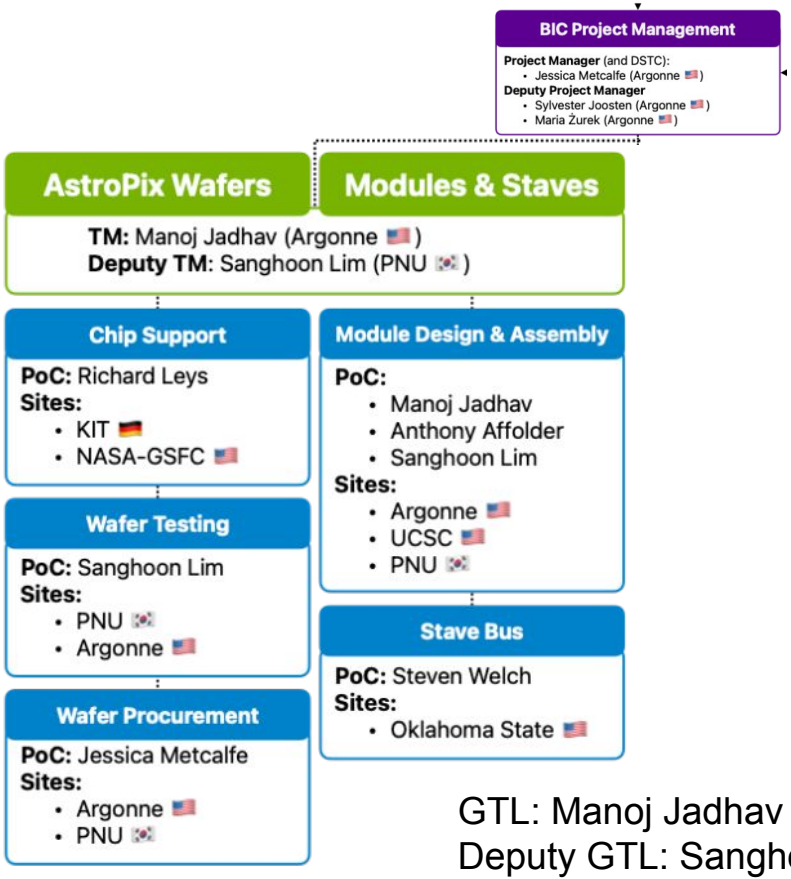


Manoj Jadhav
Argonne National Laboratory

5th BIC In-person Workshop
June 16-18, 2026

Green Team

GTL - AstroPix Wafers + BIC Modules and Staves



GTL: Manoj Jadhav
Deputy GTL: Sanghoon Lim

Work Package Scopes:

- **Chip Support**
  - Chip design
  - Version 5 for PREP and Version 6 for Production
- **Wafer Testing**
  - QC procedure
  - wafer/chip QC
  - Wafer dicing and metrology
- **Wafer procurement**
  - wafer procurement
- **Module/Stave Design and Assembly**
  - assembly, loading, and QC procedure
  - Handling and carrier toolings
  - Module assembly and QC
  - Stave loading and QC
- **Stave Bus (actually Module Hybrid-PCB - AstroLinx)**
  - AstroLinx design and fabrication (v3)
  - Update to AstroLinx for (Pre)Production (v5 and v6)
  - AstroLinx QC

Outline

- Test Article evolution - AstroPix versions, QC test stand, Module test article, readout PCB, Staves, handling and loading tools, QC procedure, assembly and loading procedure, production database

- Status overview - Ongoing activities on wafer/chip testing, Module and Stave Design, chip wirebonding and handling tools, readout PCB, 9chip board testing, assembly mockups

- PED/final design (90%) phase & deliverables → Spring/Summer 2026
  - detailed QC plan, preliminary production-like procedures (scaling)

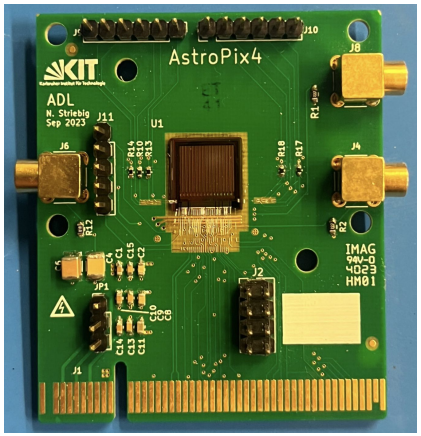
- Preproduction plans (PREP) (99%/100%)
  - practice of production

Test Article Evolution

AstroPix

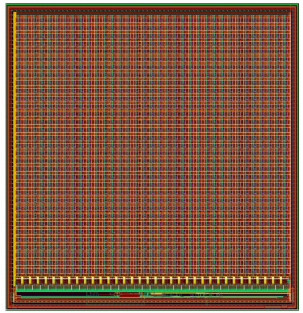
BIC PED
AstroPix v3 (1.87 cm × 1.96 cm)
First full size design
Pixel pitch: 500 µm
Pixel matrix: 35 × 35
Row/Column readout
0.88 mW/cm^2 analog, 12 mW digital
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4 (1 cm × 1 cm)
Final design engineering run
Pixel pitch: 500 µm
Pixel matrix: 13 × 16
Individual pixel readout
0.96 mW/cm^2 analog, 3 mW digital
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds

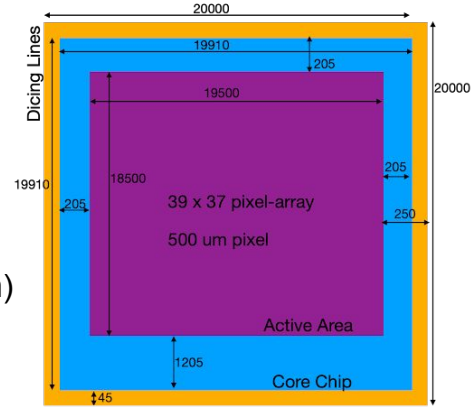


Oct 2026

BIC PREP
AstroPix v5 (1.87 cm × 1.96 cm)
Final design run
Pixel pitch: 500 µm
Pixel matrix: 36 × 34
Individual pixel readout
0.96 mW/cm^2 analog, 3 mW digital
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds



*Engineering run of v6 during PREP



BIC Final Chip Design
AstroPix v6 (2 cm × 2 cm)
Pixel pitch: 500 µm
Pixel matrix: 39 × 37
Individual pixel readout
2 mW/cm^2
3 timestamps, 3.25ns time resolution
TuneDAC for pixel-by-pixel thresholds

Test Article Evolution

Wafer/Chip QC Test Stand

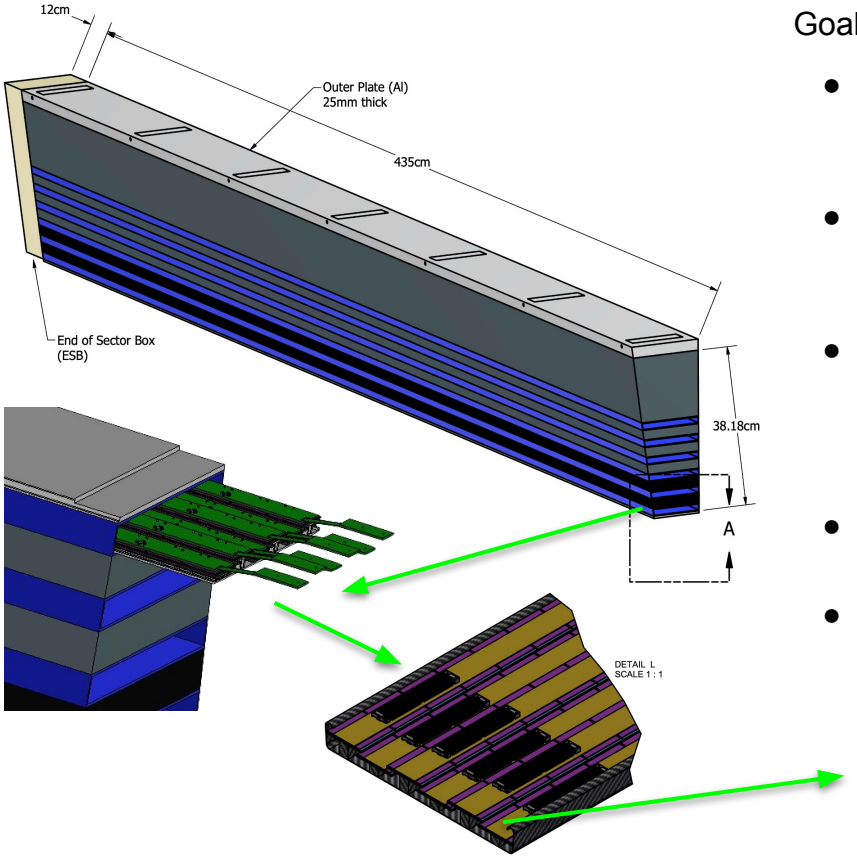
- Goal
  - Identify defective chips
  - Avoid rework and minimize efforts
  - Achieve best detector performance
- PED
  - **Chip QC test stand - Done**
  - **Design and fabricate probe card (v3) - Done**
  - **Adaptor Card for electric touchdown - Done**
  - Set initial QC procedure - In Progress
- Milestones
  - Commissioning of test stand
- PREP (Pre-Production)
  - Commissioning of Multiple chip-teststand (at 2 sites)
  - Finalize wafer QC procedure and develop testing FW/SW
  - Establish production workflow for AstroPix chips delivery
  - Test QC on ~5000 chips (85 wafers)

Chong Kim - AstroPix chip QA/QC
Wednesday, 8:30 am

Test Article Evolution

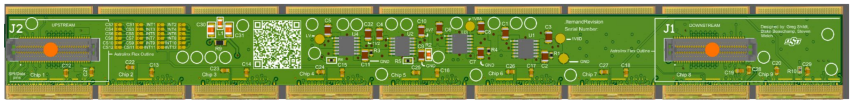
Modules and Staves

48 sectors
192 Trays
54 Staves/sector
2592 Staves
31104 Modules



Goal:

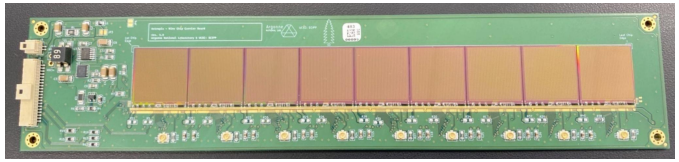
- Four imaging layers in a Sector — On-detector numbers
  - ~435 cm active length
  - Total 48 Sectors
- Tray is a structure holding the AstroPix Staves for a single layer (217.5 cm long)
  - Tray consist of 6-7-7-7 Staves (x2) in a sector
- **Stave consist of 12 AstroPix Modules**
  - Module is an electrically testable elementary unit consist of **9 AstroPix chips** with Hybrid-PCB readout (~18cm)
  - Total 31104 Modules
- Total ~360,000 AstroPix chips will be used to build the imaging layers
- All Trays will be built using same Modules, standardizing the loading procedure

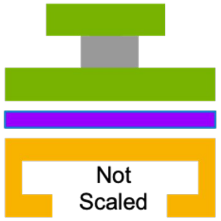


Test Article Evolution

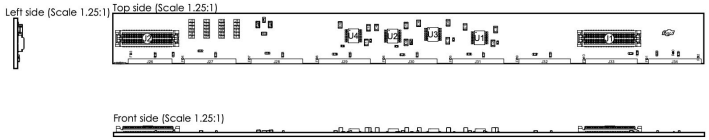
Modules and Staves

Bobae Kim - AstroPix multi-chip/layer testing
Thursday, 8:15 am



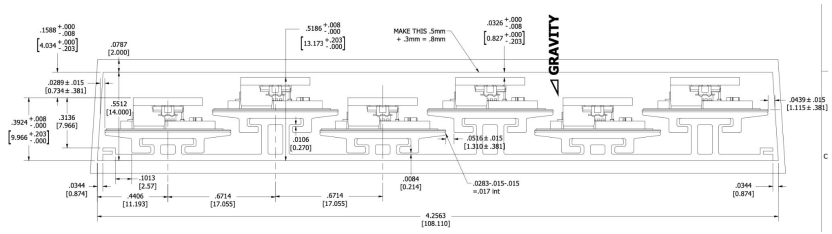


AstroLinx Flex 1.2 mm
Mated Connector 2 mm
AstroLinx 1.2 mm
Glue 0.1 mm
AstroPix 0.525 mm
Glue 0.2 mm
Module Baseplate 1 mm



PED:

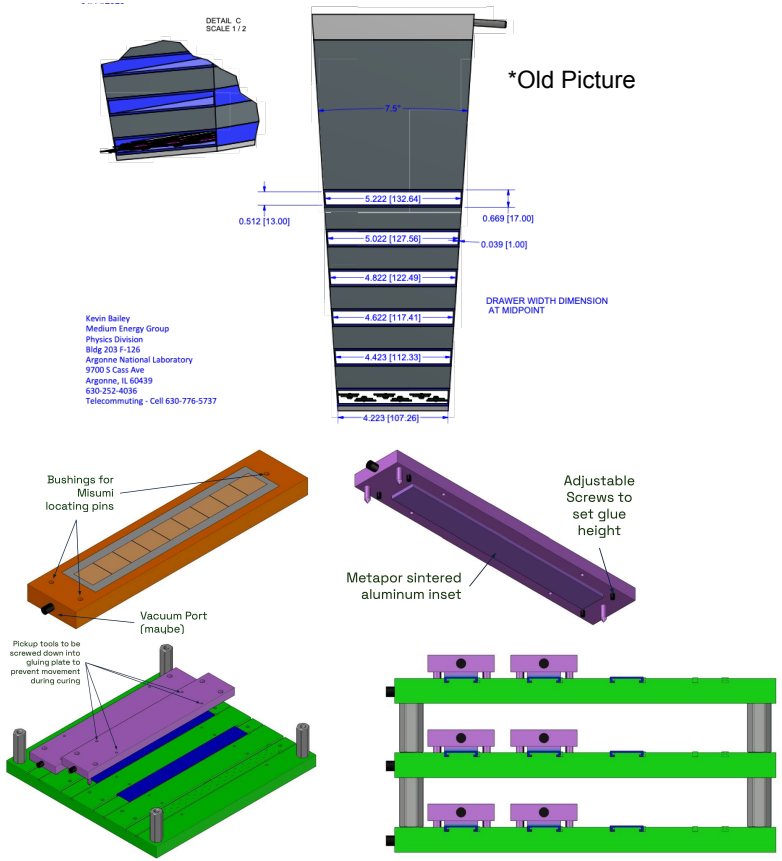
- Proof of principle: daisy-chaining - Done
  - Quadchip board testing
  - 9-chip PCB
- Build and validate design concept - mechanical support test articles for Modules and stave loading
  - evaluate and update the design - Under Fabrication
- Develop Hybrid PCB for module readout (v3) - AstroLinx - Done
- Module assembly mockups with dummy chips - In-progress
- Module assembly (6 modules) with v3 chips
- Module QC initial procedure
- Load them on Tray through Stave railing
  - - Lanky teenage BCAL



***Not updated**

Test Article Evolution

Modules and Staves



PREP:

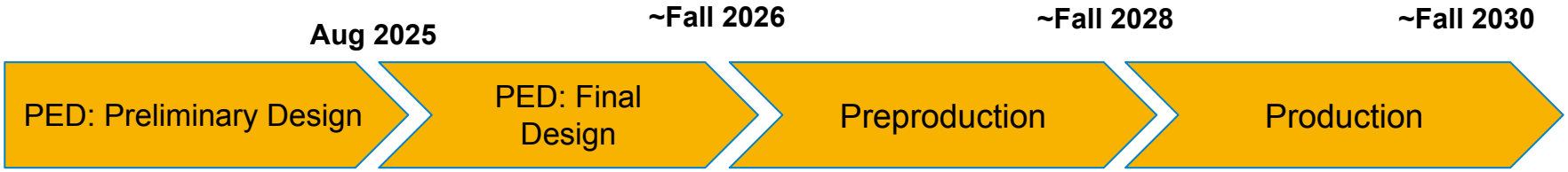
- Building half sector (~217 cm)
  - 4 layers of tracker (6+7+7+7 Staves) - Half Sector
  - Total 33 Stave - 450 Modules
- Finalize the assembly, loading, and QC procedure
- Update the Hybrid-PCB design for AstroPIx v5
- Design and fabricate handling/carrier tools - Done (v1)

  More Discussion during Module Tooling - Today 1pm

- **Assembly and Loading procedure**
  - assembly of 450 modules at 3 sites
  - loading modules to Tray
  - QC
- Development of electric and mechanical test articles for AstroPix v6 (final design)
  - Module assembly (v6 engineering run)
  - Stave loading and QC

PED Design and Pre-production Plans

Milestones - Wafer QC

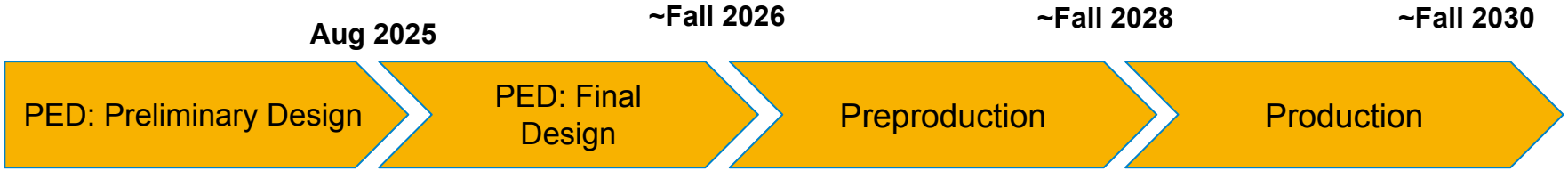


- *Fully commissioned chip test stand at PNU - July, 2026*
- QC testing of priliminary tests of AstroPix v3 chip - Aug, 2026
- *QC test procedure with v3 chips for Module - Aug, 2026*

- *AstroPix v5 delivery - October, 2026*
- Chip prober - July, 2026
- *Wafer QC procedure - Dec, 2026*
- *Wafer QC on first preproduction v5 wafer - Dec, 2026*
- *Start receiving diced QC'ed chips - March (first 6 wafers) - July 2026*
- *AstroPix v6 for Pre-Production submission - June 2027*

PED Design and Pre-production Plans

Milestones - Modules and Staves



- *Proof of Principle Daisy-Chained 9-chip Module PCB for PDR - done*
- AVAIL: 3 fully QC'ed 9-chip PCB board - done
- *Final sign-off on the AstroLinx v3 design - done*
- *First QC'ed v3 module - Aug, 2026*

- *Updated test articles (Mechanics) - Oct, 2026*
- v3 Module test articles (6 Modules) - Dec 2026
- *v3 Module loading on the Stave test articles Lanky-Teenager-BIC - Jan 2027*

- *Handling and Carrier tools ready for preproduction - Oct, 2026*
- Review AstroLinx PCB v5 - Sep 2026
- *REQD: Start receiving QC'd v5 AstroPix chips - Dec 2026*
- *Final Production pipline defined - May 2027*
- *Review of QC procedure - Sep 2027*
- *Start receiving QC'ed v5 modules - Feb 2027*
- *Preproduction phase 1 assembly completed (v5 chips) - Apr 2028*
- *Finish Loading of Staves - July 2028*
- *AVAIL: Remaining Trays ready for System Testing - Aug 2028*

BACKUP