5th BIC In-person Workshop, June 16-18, 2026

AstroPix Multi-layer/Multi-chip Testing

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U.S. DEPARTMENT of ENERGY
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AstroPix Imaging Layer R&D Milestones

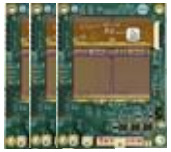
- AstroPix Multilayer/Multichip demonstration
- First beam-test operation of the 9-chip AstroPix prototype module (AstroLinx mock-up)
- Integration between H2GCROC (Calorimeter readout) and A-STEP board (AstroPix readout) using external common clock

AstroPix v3

Single chip

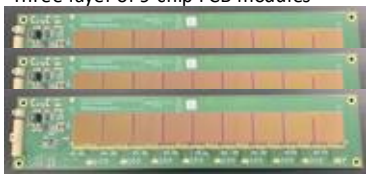
Quad-chip

Three-layer of quad-chips



9-chip prototype PCB module

Three-layer of 9-chip PCB modules



AstroPix v4

AstroPix v5: Chip delivery is expected in Oct. after the fabrication process.

+ ETC (Final AstroPix readout system, designed and developed by NASA)

Configuration of **AstroPix v4**	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (KEK, Dec.2025)

Configuration of **AstroPix v3**	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (FNAL, Jun.2024) (arXiv:2602.06084)
Three-layer of single-chips	Three GECCO boards + customized DAQ	1x3	✅ beam tests (CERN & KEK, 2025 summer) by Korean collaborators (arXiv:2605.07681)
Quad-chip	A-STEP FPGA board	2x2	✅ bench/beam tests (KEK, Dec.2025)
Three-layer of quad-chips	A-STEP FPGA board	3x(2x2)	✅ bench/beam tests (KEK, Dec.2025)
9-chip prototype PCB module	A-STEP FPGA board	1x9	✅ bench test/beam tests (KEK, May.2026)
Three-layer of 9-chips	A-STEP FPGA board	3x(1x9)	Ready to test; (beam test in Aug.2026)
Three-layer of quad-chips + Three-layer of 9-chips	Two A-STEP FPGA boards + external clocks	3x(2x2) 3x(1x9)	Ready to test; (beam test in Aug.2026)

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Multichip Testing Setup

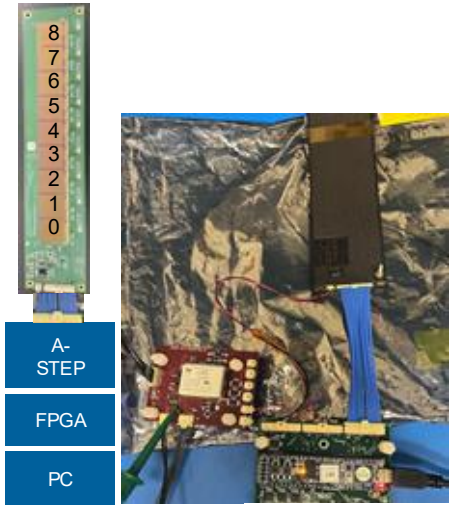
9-chip Test Article + AstroPix DAQ

9-chip Test Article

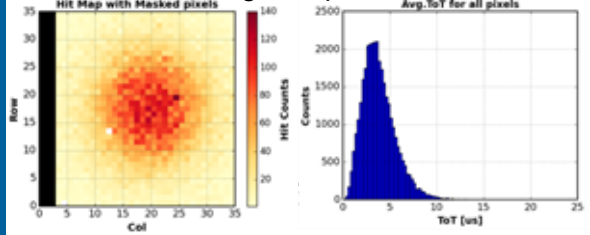
- PCB design based on single-chip/quad-chip carrier boards
- Mockup of the AstroLinx electronics
- Readout: **Daisy-chained 9 AstroPix chips** via SPI

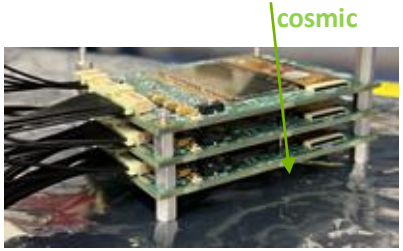
AstroPix DAQ: A-STEP board + CMOD FPGA

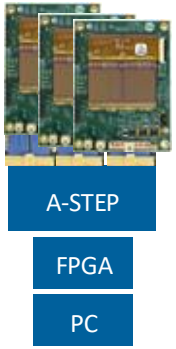
- Developed for NASA A-STEP sounding rocket payloads (ComPair-2 prototype), now also used for current performance evaluations (prototype of ETC)
- Supports up to three layers with quad-chip/9-chip modules
- Validated operation of a three-layer quad-chip configuration (up to 12 chips) by cosmic-ray tests as well as beam condition

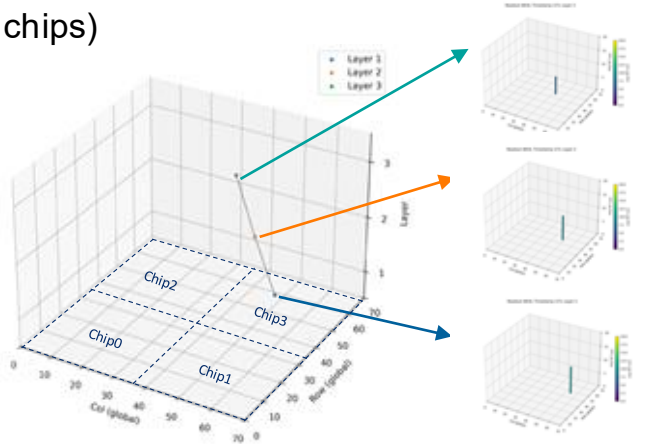


Reference: v3 single-chip Sr-90 test results







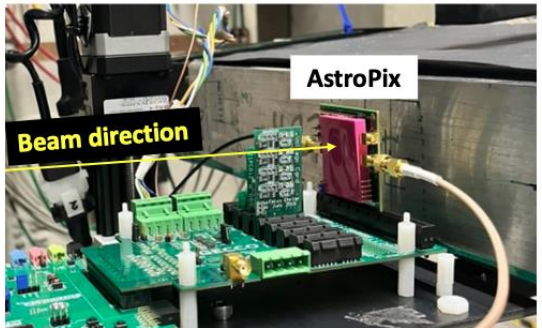


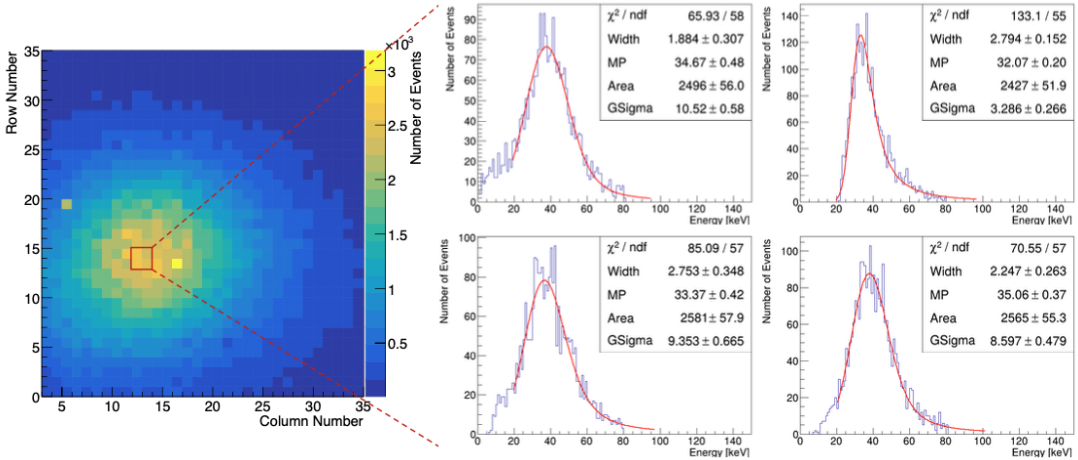
Beam Test Result at FTBF 2024

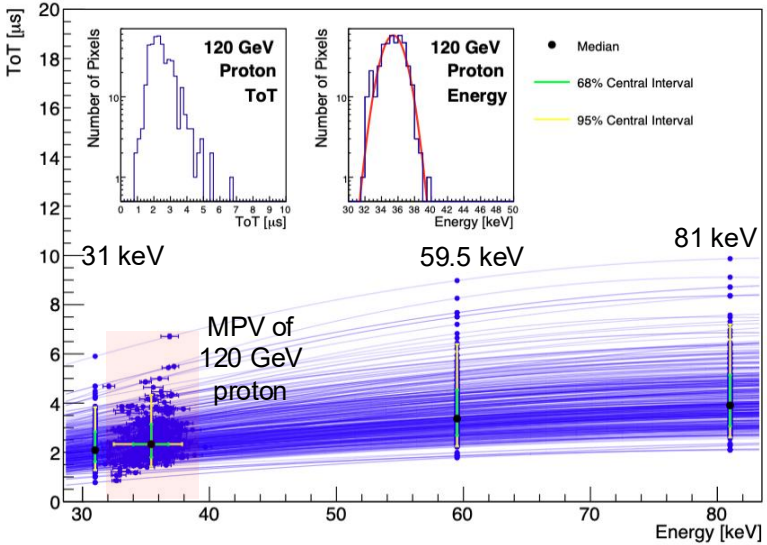
B. Kim, ArXiv: 2602.06084,
Submitted to NIMA

AstroPix v3 single chip with 120 GeV proton beam

- First 120 GeV proton response
- MIP response within dynamic range (25 keV~200 keV)
- All distributions are well described by a Landau–Gaussian convolution
- MPV of MIPs across all pixels = 34 ± 1.9 keV,
  corresponding to the effective depletion depth ~ 128 ± 8 um



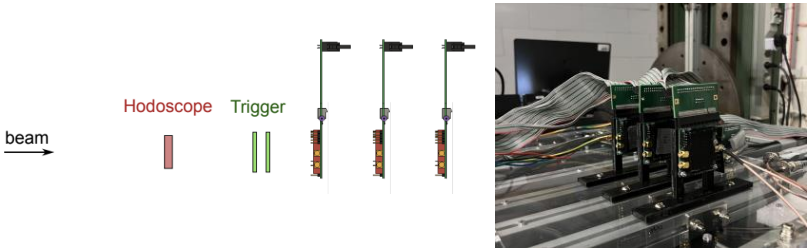


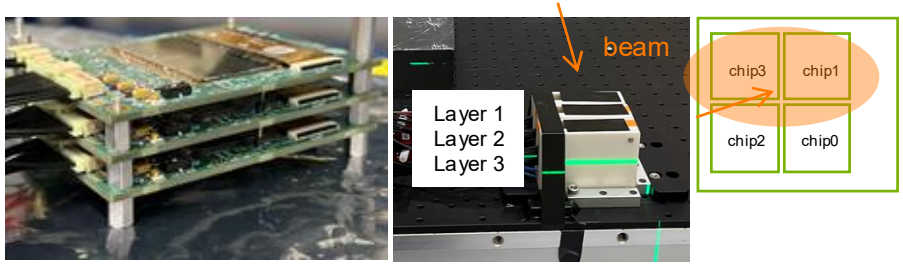


→ **AstroPix v3 meets EIC requirement for MIP detection with sufficient dynamic range.**

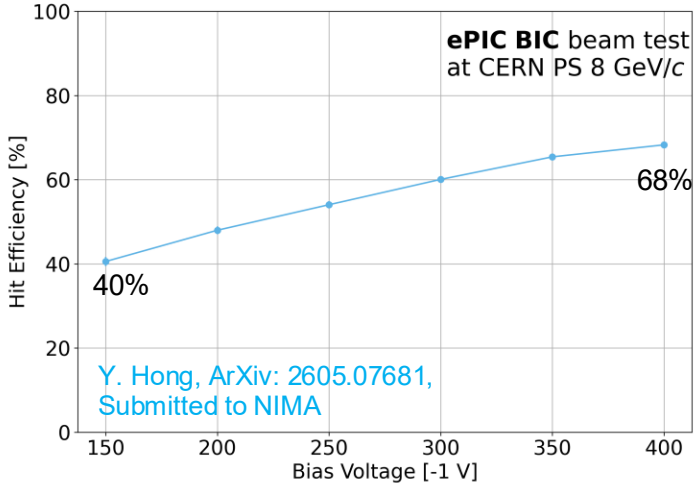
Beam Test Result at KEK/CERN 2024/2025

Three AstroPix v3 single chips and quad-chips with e- beam

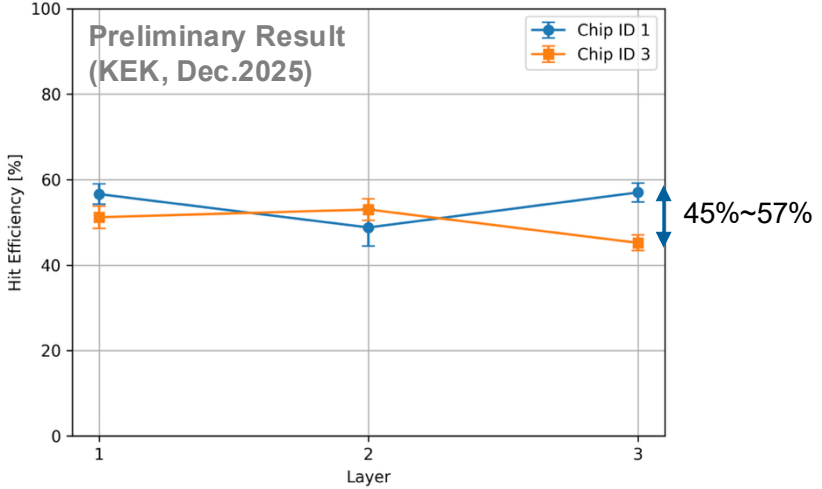




- Hit efficiency as a function of bias voltage (-150 to -400 V) with three AstroPix single-chips



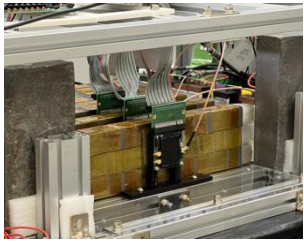
- Hit efficiency per layer using three AstroPix quad-chips Bias voltage = -150V



→ **AstroPix v3 shows hit efficiencies of 40–68%, and further improvements are expected in AstroPix v5.**

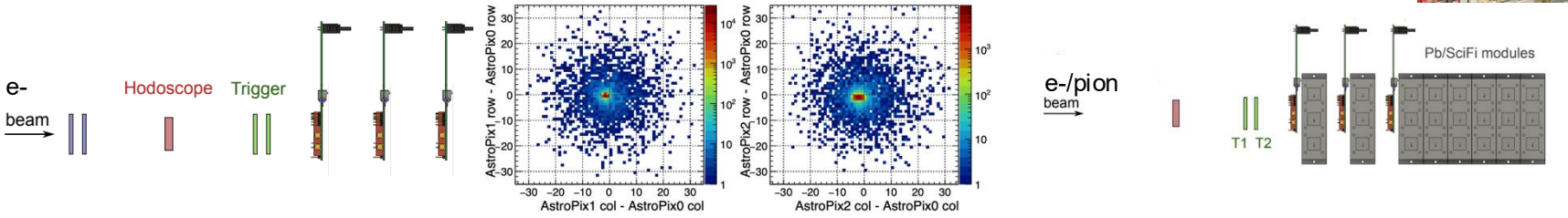
Beam Test Result at KEK/CERN 2025

Y. Hong, ArXiv: 2605.07681, Submitted to NIMA



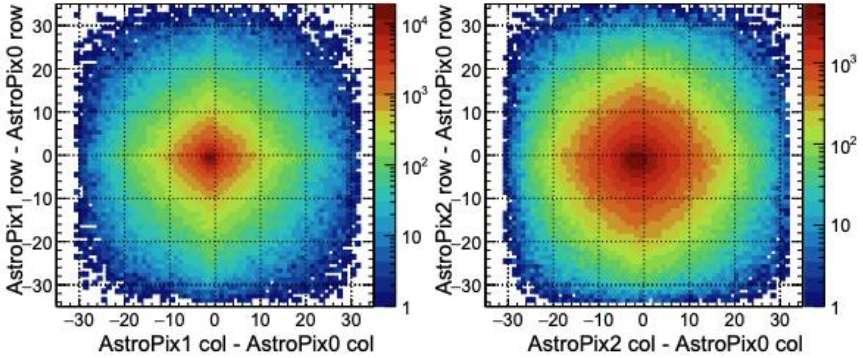
Three AstroPix v3 single chips interleaved Pb/SciFi modules

- Goal: investigated the capability of AstroPix to measure EM shower development

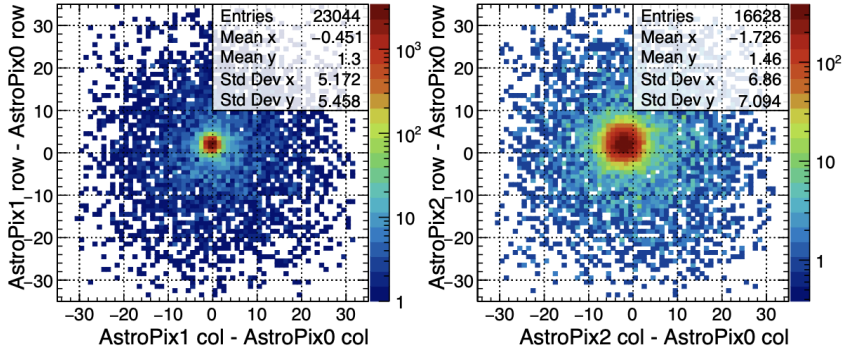


- Position residuals between the first (reference) AstroPix-v3 layer

AstroPix+Calo@4.5GeV **electron beam**



AstroPix+Calo@2GeV **only hadrons**



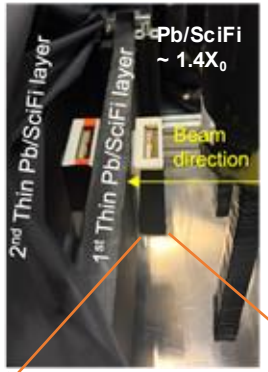
→ **AstroPix measurements provide a quantitative characterization of EM shower development.**

→ **Distinct position residual patterns are observed for electrons and pions, providing discrimination power between them.**

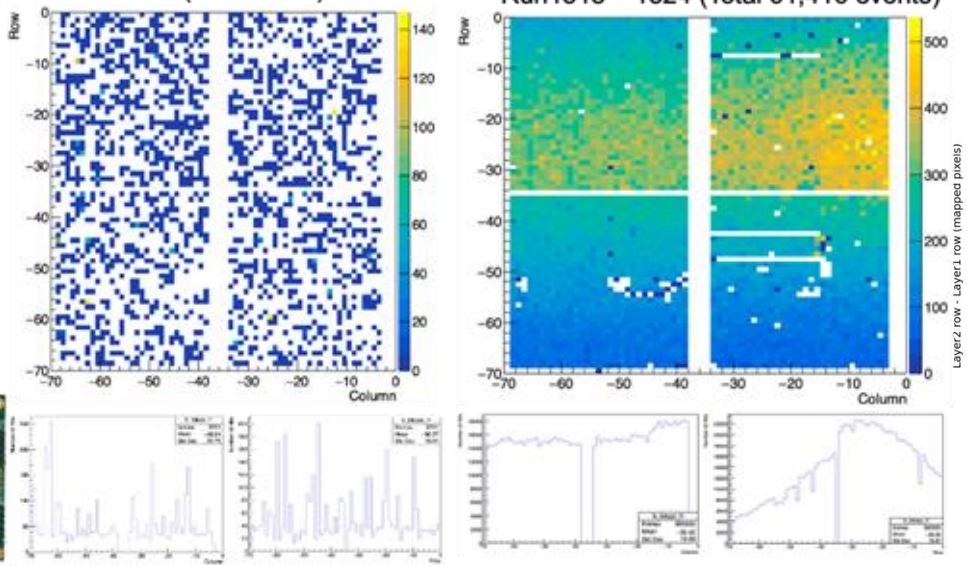
Beam Test Result at Hall D 2026

Two AstroPix v3 quad chips interleaved Pb/SciFi modules

- Confirmed the stable operation up to ~1.2 kHz beam rate at KEK beam test last year; **promising stable operation under Hall D beam conditions.**

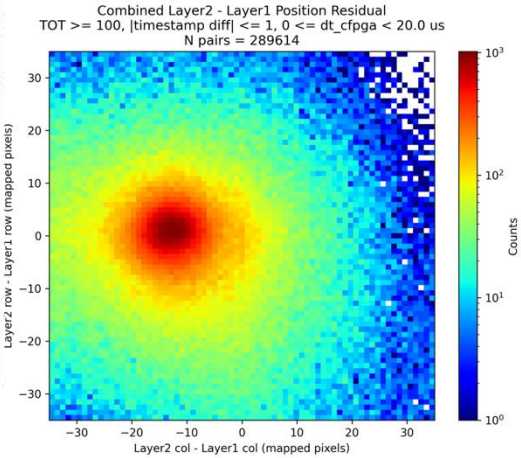


- 1st layer of AstroPix quad-chip: beam profile
  - No beam (cosmic run)
  - Run1318 – 1324 (Total 61,416 events)



- Position residual plot

500 MeV electron @ hall D



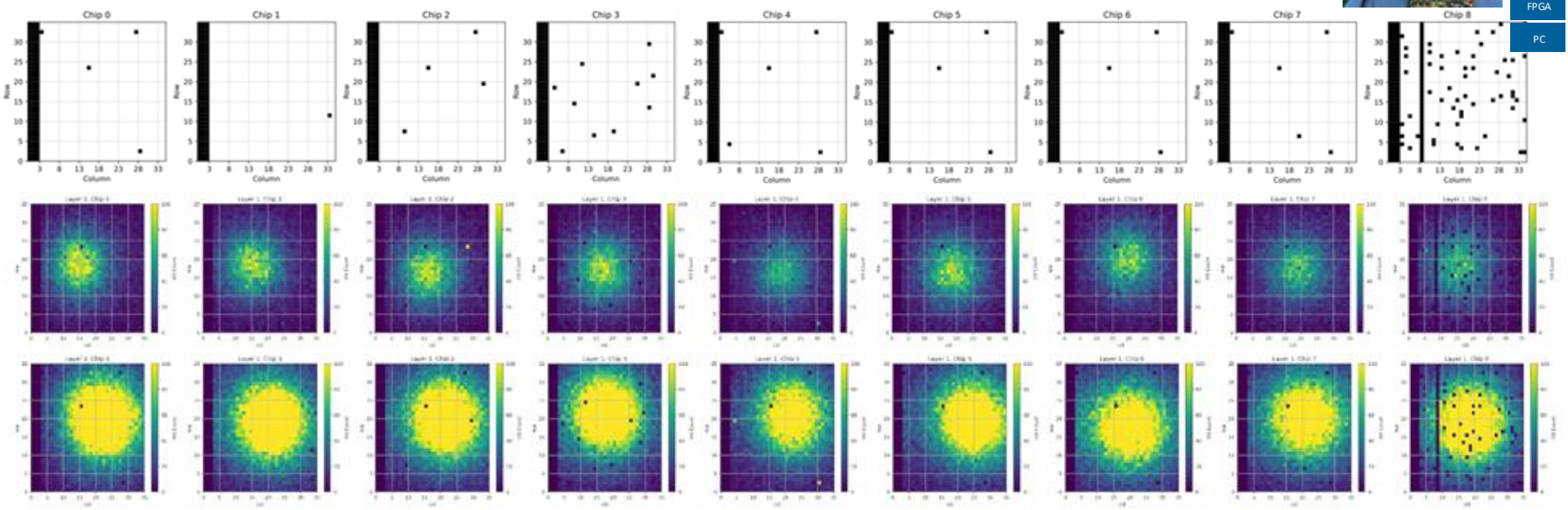
Work In Progress

→ **The quad-chips shows a position residual pattern consistent with the single-chip measurements.**

9-chip Module: Bench Test Result

B.Kim,
PoS(VERTEX2025) 031, 2025

- Benchmarking electric design of AstroPix Module for BIC: proof of concept with module readout design (mock up of AstroLinx)
- **Noise scan -** pixels with noise rate ≥ 1 Hz were masked
  - **Achieved 99% active pixel yield** for all chips (except chip 8: 91.9%)
- **Source test with Sr-90**
  - Results consistent with v3 single-chip performance, confirming proper operation

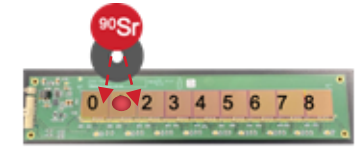


→ **Demonstrated stable operation and validated daisy-chained readout** of the prototype module.

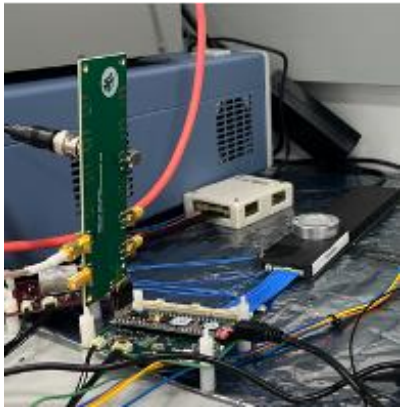
9-chip Module: Data Rate Results

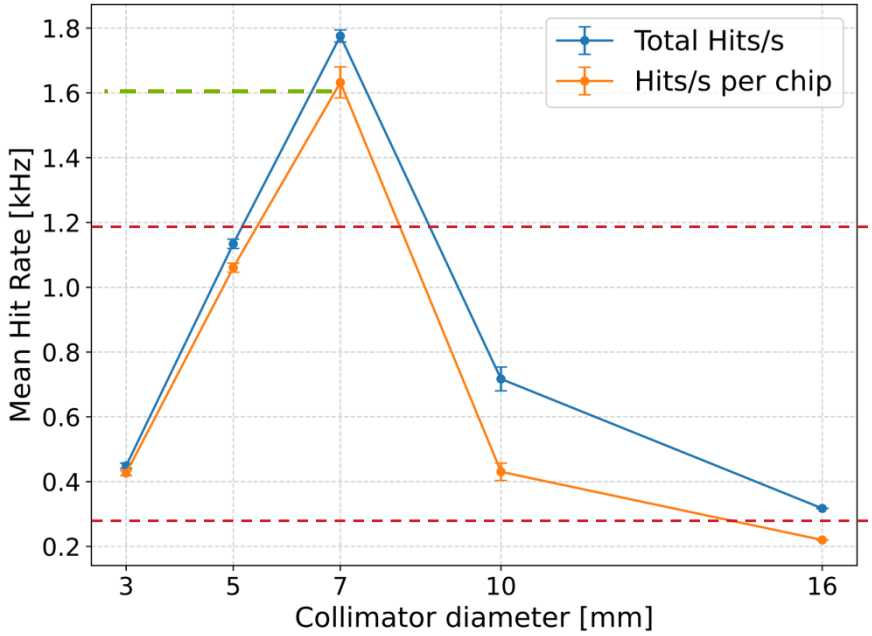
B.Kim,
PoS(VERTEX2025) 031, 2025

- Goal: Validate the capability to read out data from the 9-chip prototype with the current setup
- Maximum hit rate with the current setup:
  - **Per 9 chips:** ~1.7 kHz
  - **Per chip:** ~1.6 kHz



Collimator: 3/5/7/10/16 mm diameters





Saturation limit with collimators > 7 mm, where stable data-taking is no longer possible.

~1.18 kHz per chip: **Max**. expected data rates for imaging layers, taking into account DIS, electron, and proton beam backgrounds

Based on **Tommy's simulation result**

~285 Hz per chip: **Avg**. expected data rates for imaging layers

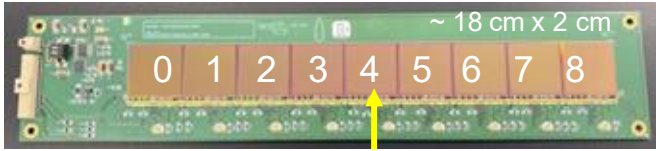
→ **The per-chip measurement on the 9-chip prototype**, under the current setup, **meets imaging-layer data-rate.**

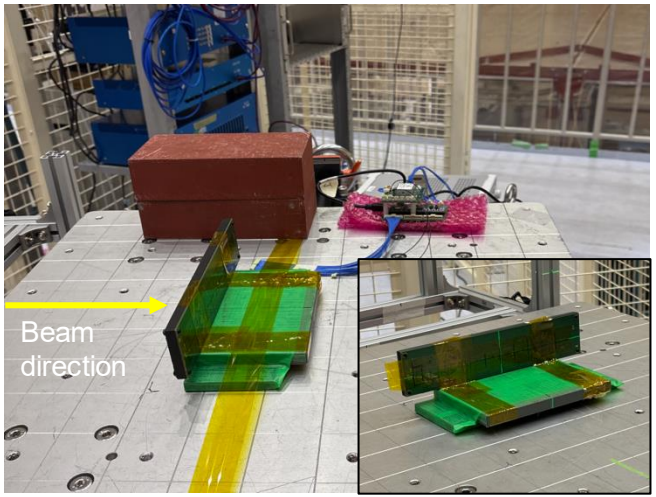
→ **Operation in realistic beam conditions is promising:** ~1.18 kHz per chip is **expected on ~2–3 chips.**

9-chip Module: Beam Test Result at KEK 2026

J. Park, B. Kim, J. Bok

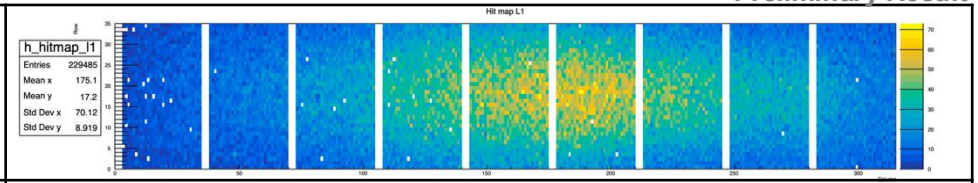
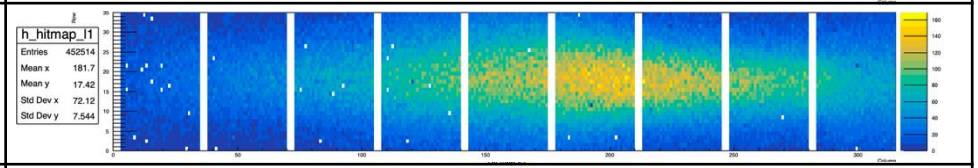
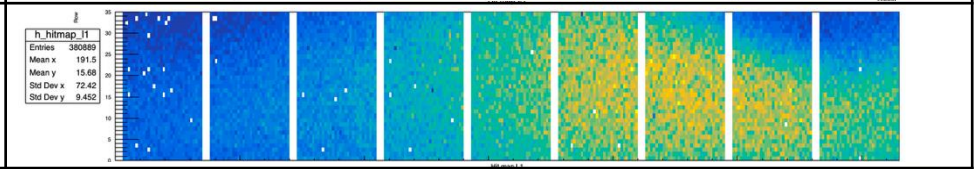
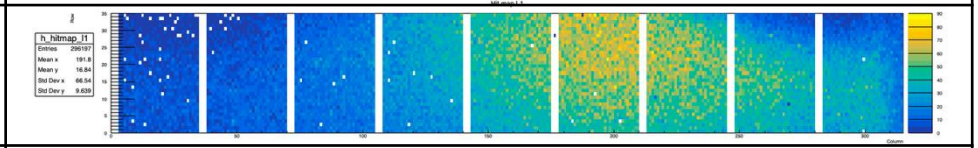
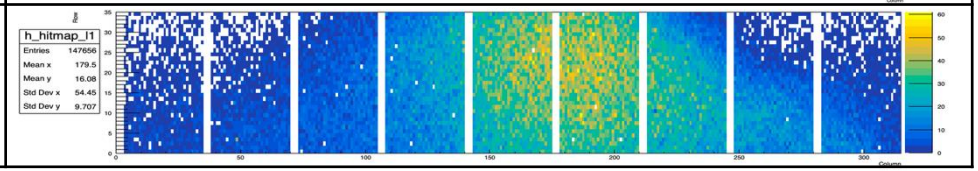
Operational verification under beam conditions





- Electron beam energies 1–5 GeV
- Stable data-taking up to a **2.7 kHz beam rate**

Preliminary Result

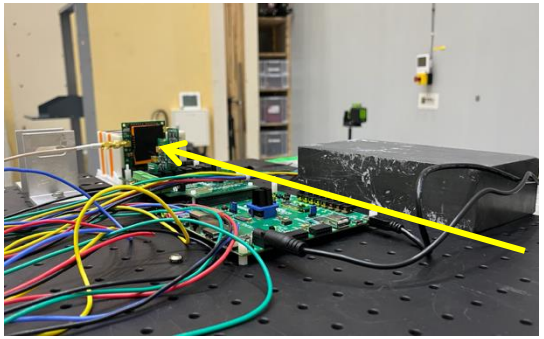
1 GeV (~1.3 kHz)	
2 GeV (~2.3 kHz)	
3 GeV (~2.7 kHz)	
4 GeV (~2.3 kHz)	
5 GeV (~1.2 kHz)	

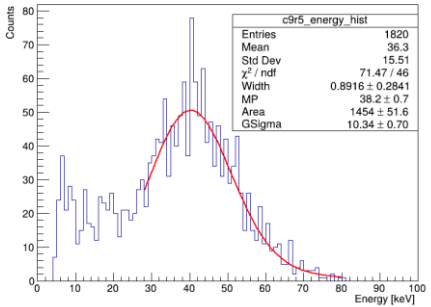
→ **The first beam test of the 9-chip prototype module showed stable operation up to 2.7 kHz beam rate.**

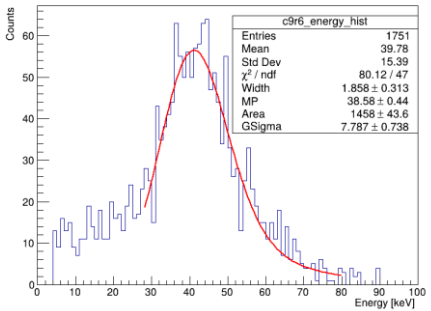
AstroPix v4 Single-chip Test Result

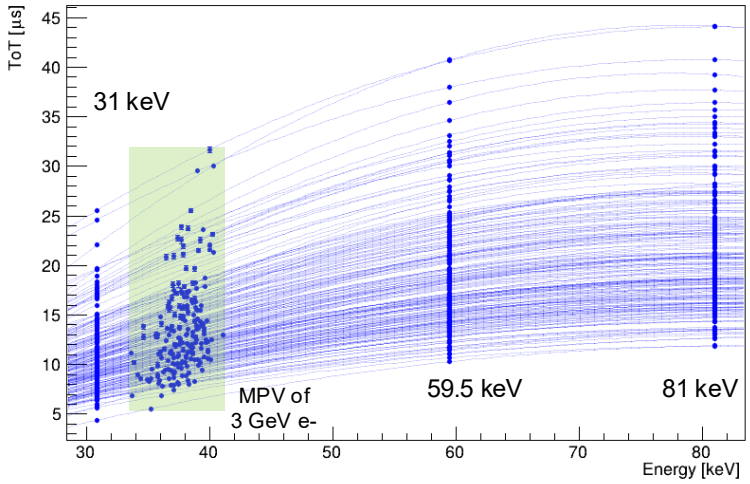
Beam test at KEK in Dec.2025

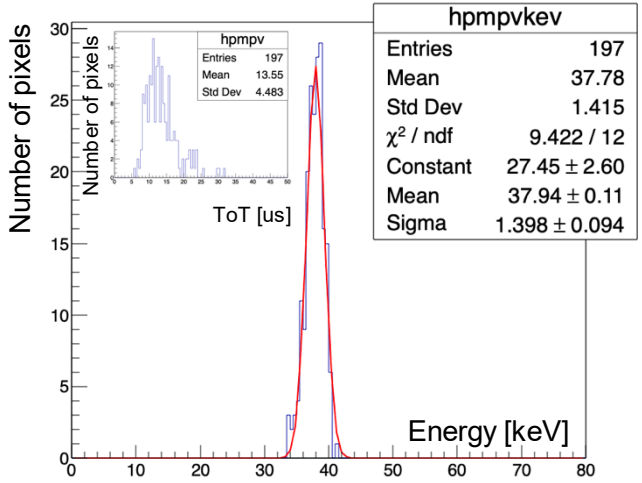
- Total 203 pixels except for 5 masked pixels: **92.8%** pixels of AstroPix v4 sensor (13*16 pixel matrix)
- Used -175 V bias voltage and 140 mV threshold; 3 GeV electron beam
- Energy distribution per pixel fitted with Landau convoluted with Gaussian function
- MPV of MIP = 37.9 ± 1.4 keV, corresponding effective depletion depth of 142 ± 5 um
- 1.4/37.9 = 3.7% pixel-to-pixel variation











→ AstroPix v4 meets EIC requirement for MIP detection with sufficient dynamic range.

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Summary

- AstroPix v3 multi-layer/multi-chip testing has been performed:
  - Demonstrated the AstroLinx proof of concept with a 9-chip prototype module
  - Demonstrated the feasibility of the current setup as an AstroPix imaging layer.
  - Reported the results at the FY25 PDR.

- Remaining AstroPix v3 tests toward the final design review
  - v3 AstroLinx
  - Module test article → Half-stave test article (6 modules daisy-chained via AstroLinx) → Stave

- AstroPix v3 multi-layer/multi-chip system under preparation for upcoming beam tests

- AstroPix v4
  - Performed MIP response study at KEK using the same procedure as AstroPix v3.

- AstroPix v5
  - Chip delivery is expected in **Oct**. after the fabrication process.
  - Single chip performance test + GECCO board
  - Multi-layer/Multi-chip + v5 AstroLinx + ETC board

Back up

AstroPix Development Timeline

Not shown:
Early CD4 (Oct 2032)
CD4 (Oct 2034)

We are here

FY19 Q3 Q4 | FY20 Q1 Q2 Q3 Q4 | FY21 Q1 Q2 Q3 Q4 | FY22 Q1 Q2 Q3 Q4 | FY23 Q1 Q2 Q3 Q4 | FY24 Q1 Q2 Q3 Q4 | FY25 Q1 Q2 Q3 Q4 | FY26 Q1 Q2 Q3 Q4 | FY27 Q1 Q2 Q3 Q4 | FY28 Q1 Q2 Q3 Q4 | FY29 Q1 Q2 Q3

- AstroPix v1: Design & Fabr. → Test
- AstroPix v2: Design & Fabr. → Test
- AstroPix v3: Design & Fabr. → Test → **Test Prototype** for BIC and NASA space mission
- AstroPix v4: Design & Fabr. → Test
- AstroPix v5: Design & Fabr. → Test
- AstroPix v6: Design & Fabr. → AstroPix v6 (production) → Production Fab.

v3 has comprehensive test program:
bench test and beam test, irradiation test,
quad-chip readout for NASA payload mission (A-STEP)
nine-chip prototype module test,
integration with Pb/SciFi for ePIC
(R&D studies and test article production)

First v5 wafers used for preproduction

EIC Project Milestone
New AstroPix version

ePIC BIC Timeline

- Design and generic R&D
- Final design and EIC R&D
- BIC Preproduction
- BIC Production

CD0 | CD1 | CD3a | CD3b | CD2/3 | Start of BIC installation at BNL

*from v5 fabrication, fabrication foundry changed TSI into AMS

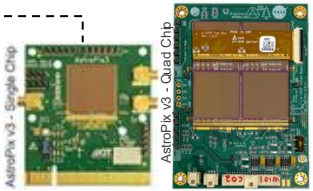
AstroPix v1

HV-CMOS MAPS based on ATLASPix3, designed for the AMEGO-X NASA mission, optimized for power dissipation and energy resolution
NIMA 1019 (2021) 165795

0.45 x 0.45 cm² chip, 175 µm pixel pitch
18 x 18 pixel matrix
Power dissipation 14.7 mW/cm²

AstroPix v2

1 x 1 cm² chip, 250 µm pixel pitch
35 x 35 pixel matrix
Row/column readout
Power dissipation 3.4 mW/cm²



AstroPix v3

First full-size chip

First full size design: 1.87 cm × 1.96 cm
Row/Column readout
Pixel pitch: 500 µm
Pixel matrix: 35 × 35
0.88 mW/cm² analog, 12 mW digital
2.5 MHz timestamp, 200 MHz ToT

AstroPix v4

Final design but smaller size

1 x 1 cm² chip, 500 µm pixel pitch
13 x 16 pixel matrix
Individual pixel readout
3 timestamps, 3.25 ns time resolution
TuneDAC for pixel-by-pixel thresholds

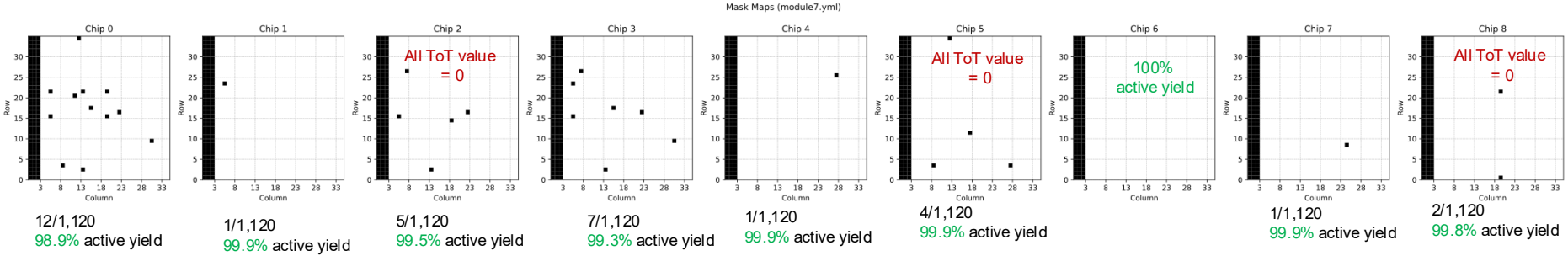
AstroPix v5
pre-production chip
1.87 x 1.9575 cm² chip, 500 µm pixel pitch
Design identical to v4 (with bug fixes)

AstroPix v6
production chip
2 x 2 cm² chip, 500 µm pixel pitch
Design identical to v5 (with bug fixes)

*Dec 2031 - ready for installation at BNL

Module 7: mask map & Sr90 source test

At ANL



12/1,120
98.9% active yield

1/1,120
99.9% active yield

5/1,120
99.5% active yield

7/1,120
99.3% active yield

1/1,120
99.9% active yield

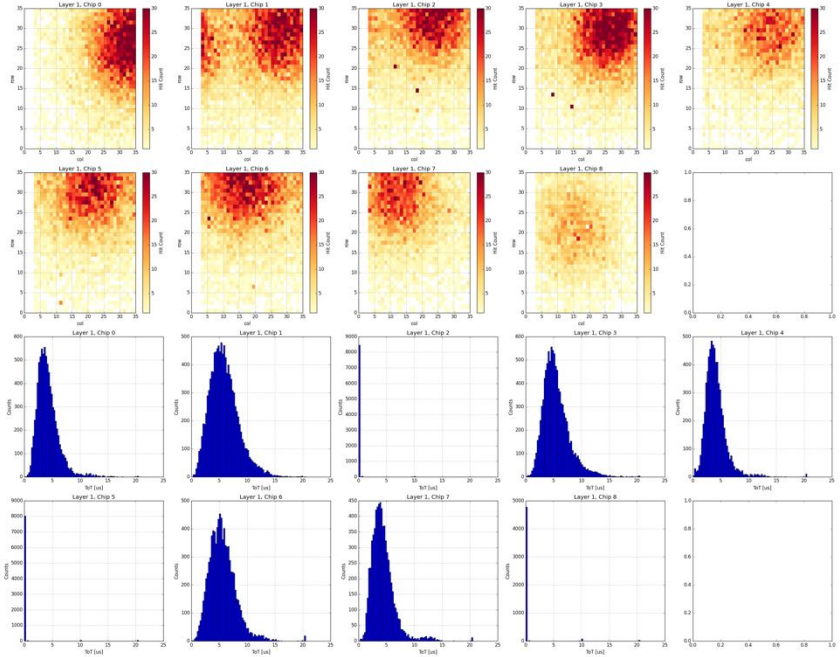
4/1,120
99.9% active yield

1/1,120
99.9% active yield

2/1,120
99.8% active yield

- 100% active yield at 6
- Need to check chip 2, 5, 8 observed with all ToT = 0

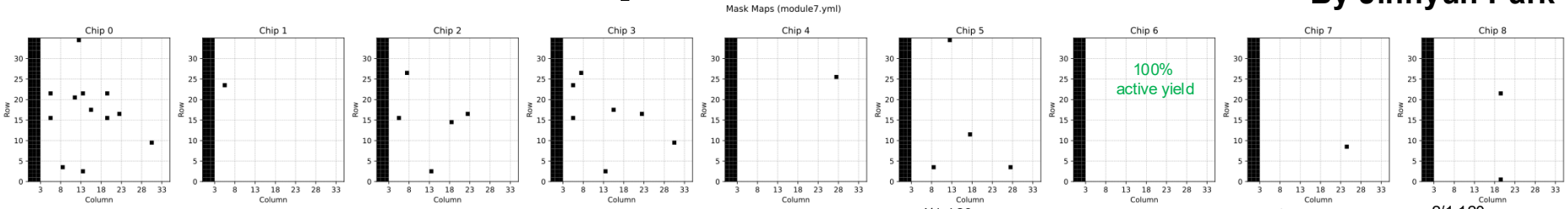
Based on official commit **b9d9722 (Jun 9, 2025)**
https://github.com/bobae0124/astep-fw/tree/quad-9chip-datareview
quad-9chip-datareview branch



- 0.27 A @5.3V
- 10 uCi Sr90 with 5 mm collimator
- Data-taking rate (compared with 4,096 max buffer)
  - Noise < 100
  - Sr-90 < 600
- 90 s data-taking, 10 s each chip
- Well-aligned with source positions
- Observed 0 ToT value from chip 2, 5, 8

Module 7: mask map & Sr90 source test

At PNU
By Jinhyun Park



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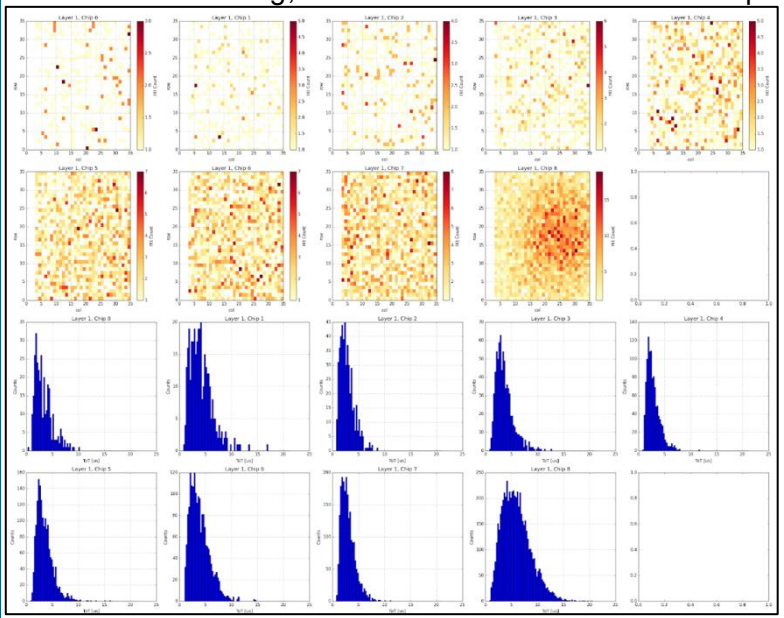
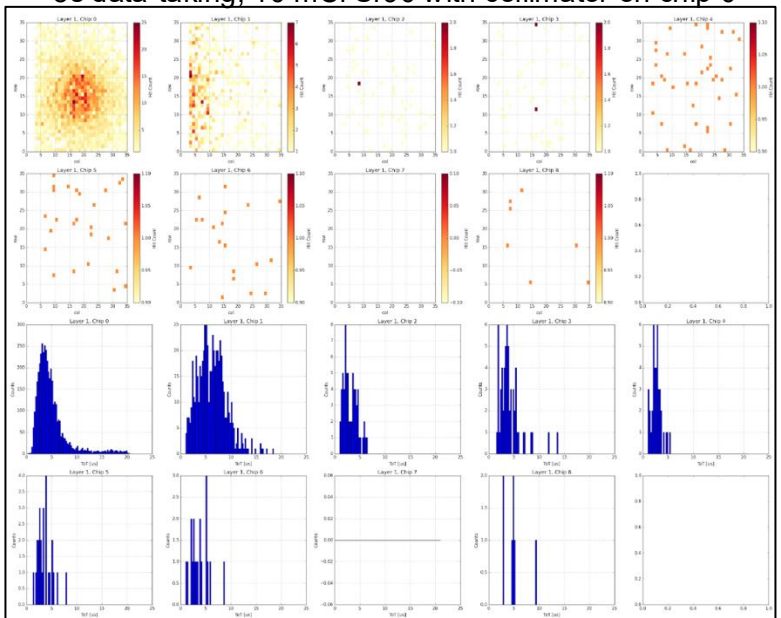
- 1 min data-taking; 10 mCi Sr90 with collimator on chip 8



- 5s data-taking; 10 mCi Sr90 with collimator on chip 0

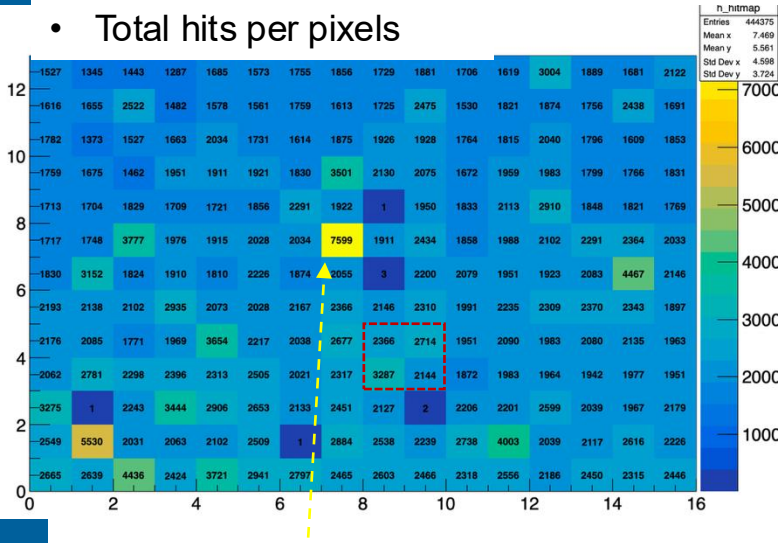


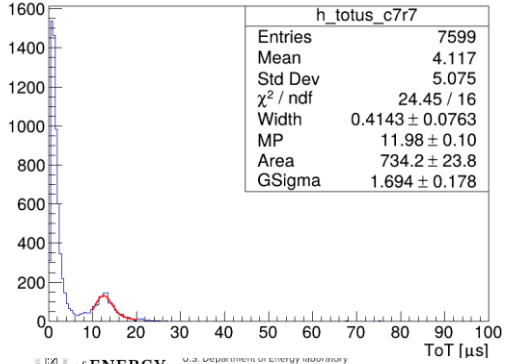
Based on official commit **ac972e0 (Aug 8, 2025)** https://github.com/bobae0124/astep-fw/tree/ext-clock ext-clock branch

Argonne NATIONAL LABORATORY

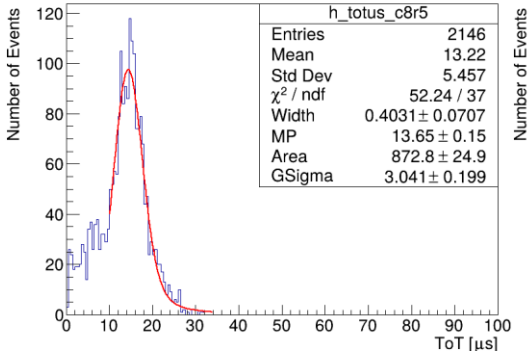
V4 3 GeV electron; fitting results

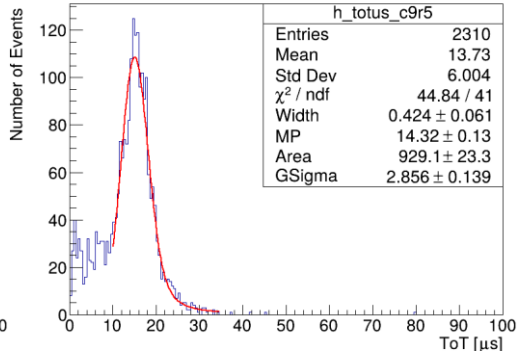
- Total hits per pixels

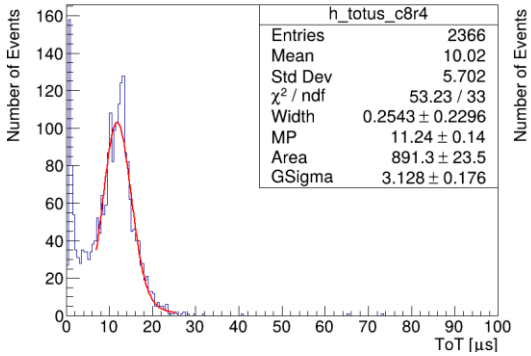


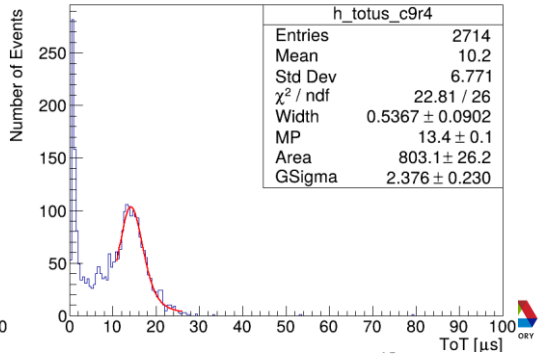


- Total 203 pixels except for 5 masked pixels
- ToT distribution per pixel fitted with Landau convoluted with Gaussian function
- Fitting results for all pixels : (link)





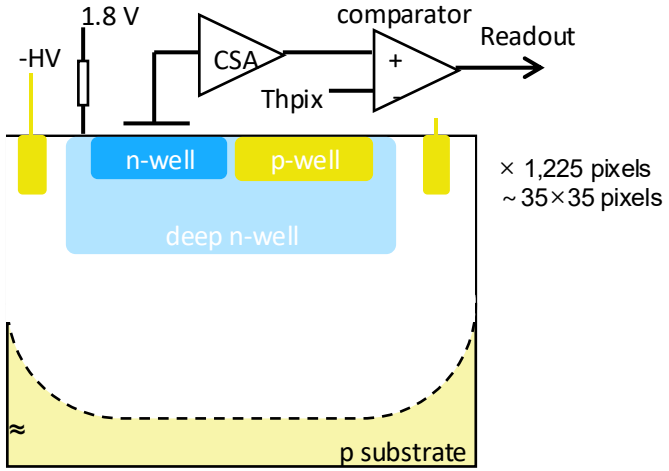




Overview of AstroPix

High-voltage CMOS monolithic active pixel sensor (HV-CMOS MAPS)

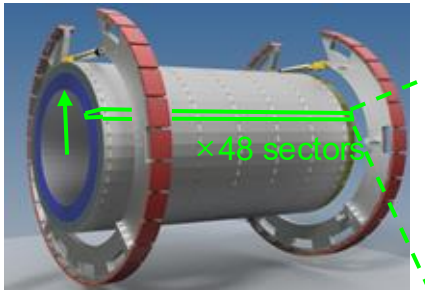
- based on ATLASpix3 [arXiv:2109.13409]
- Originally developed for space-based missions, specifically for gamma-ray astrophysics
  - NASA AMEGO-X space mission and ComPair2 project
- Use as the imaging layers in the barrel imaging calorimeter for nuclear physics applications.

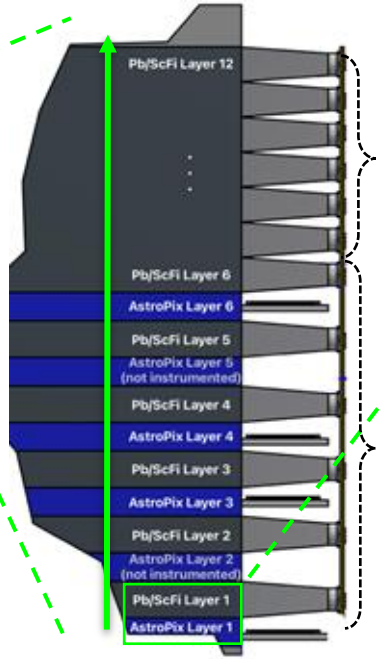


https://arxiv.org/abs/2407.05947

- **Astropix v3 single chips**
  - 2×2 cm^2 -size with 35 × 35 pixel matrix
  - 500 µm pixel pitch, 725 µm thickness
  - Time stamp clock: 8-bit at 2.5 MHz (400 ns)
  - ToT (Time over Threshold) clock: 12-bit at 200 MHz (5 ns)
- **Astropix v4 single chips**
  - 1 x 1 cm^2 -size with 13 × 16 pixel matrix
  - 500 µm pixel pitch
  - Individual pixel readout
  - 3 timestamps, 3.25 ns time resolution
  - TuneDAC for pixel-by-pixel thresholds

Structure of Imaging Layer with AstroPix in BIC

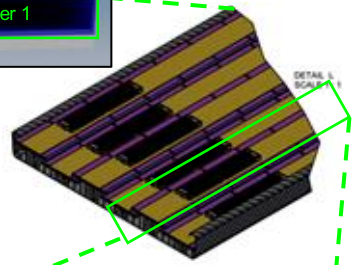




Large **back section of Pb/ScFi**

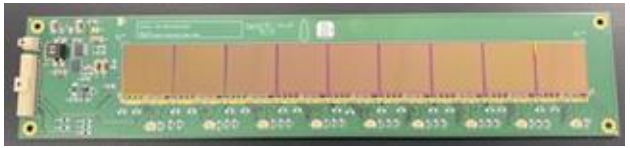
4(+2) imaging layers with AstroPix sensors interleaved with **5 Pb/ScFi layers**

Astropix Layer + Pb/SciFi Layer



Tray
Structure holding the AstroPix staves for a single layer (217.5 cm long). Consists of 6-7 staves.

Stave
Consists of 12 modules.

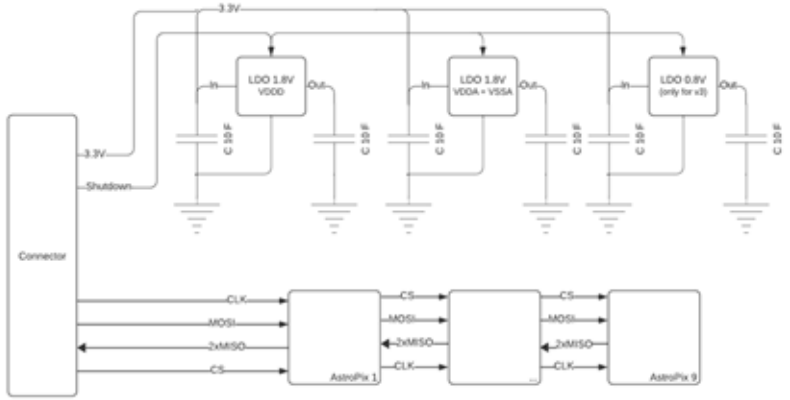


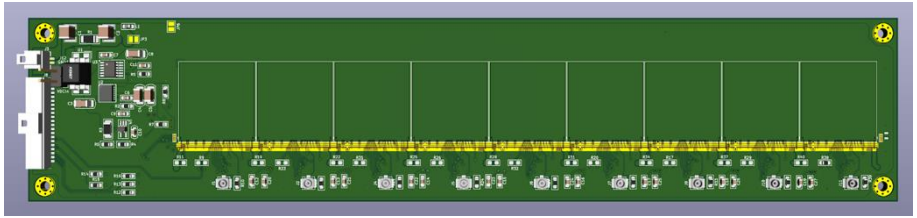
AstroPix Module
9 AstroPix sensors daisy-chained together on PCB.

- 4 imaging layers in a Sector
  - Total 48 Sectors
  - 435 cm active length
- Total 279,936 AstroPix chips will be used to build the imaging layers in BIC.
  - Total 31,104 modules
- All Trays will be built using same modules, standardizing the loading procedure
- The first prototype module, built with v3 sensors for initial testing.

AstroPix 9 Chip PCB Test Module

- Similar design to quad chip board (no busbar required)
- Nine AstroPix Chips, **Daisy-chained on the Module**
- Each Module plugs into its adjacent Module
- All Modules will be **controlled by the End-of-Tray Card**
- The broadcast commands/data readout through **SPI protocol**
- One main HV line (~500V) and one (or 2) LV line (3.3V)
- Voltage Regulators (LDO) to regulate power on each Module
    - Analog and digital power of 1.8V at Module
- 4 **differential data SPI (Clk, MOSI, 2MISO)** common for stave
- One **single-ended Chip-select SPI** per Module
- Approximately **24 I/O + GND** Pins per Stave
    - Exploring connector options (radiation hard, smaller size)



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