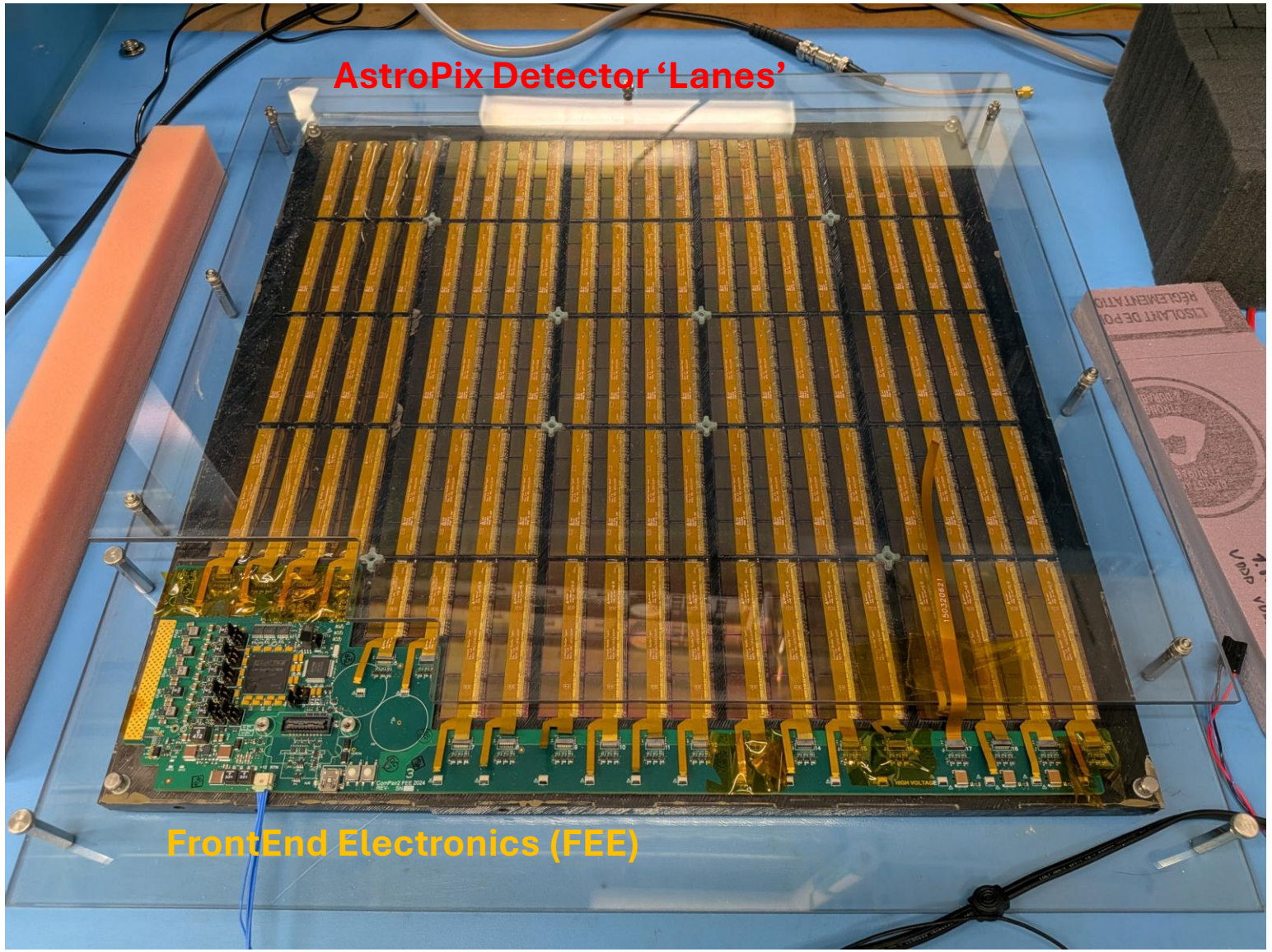
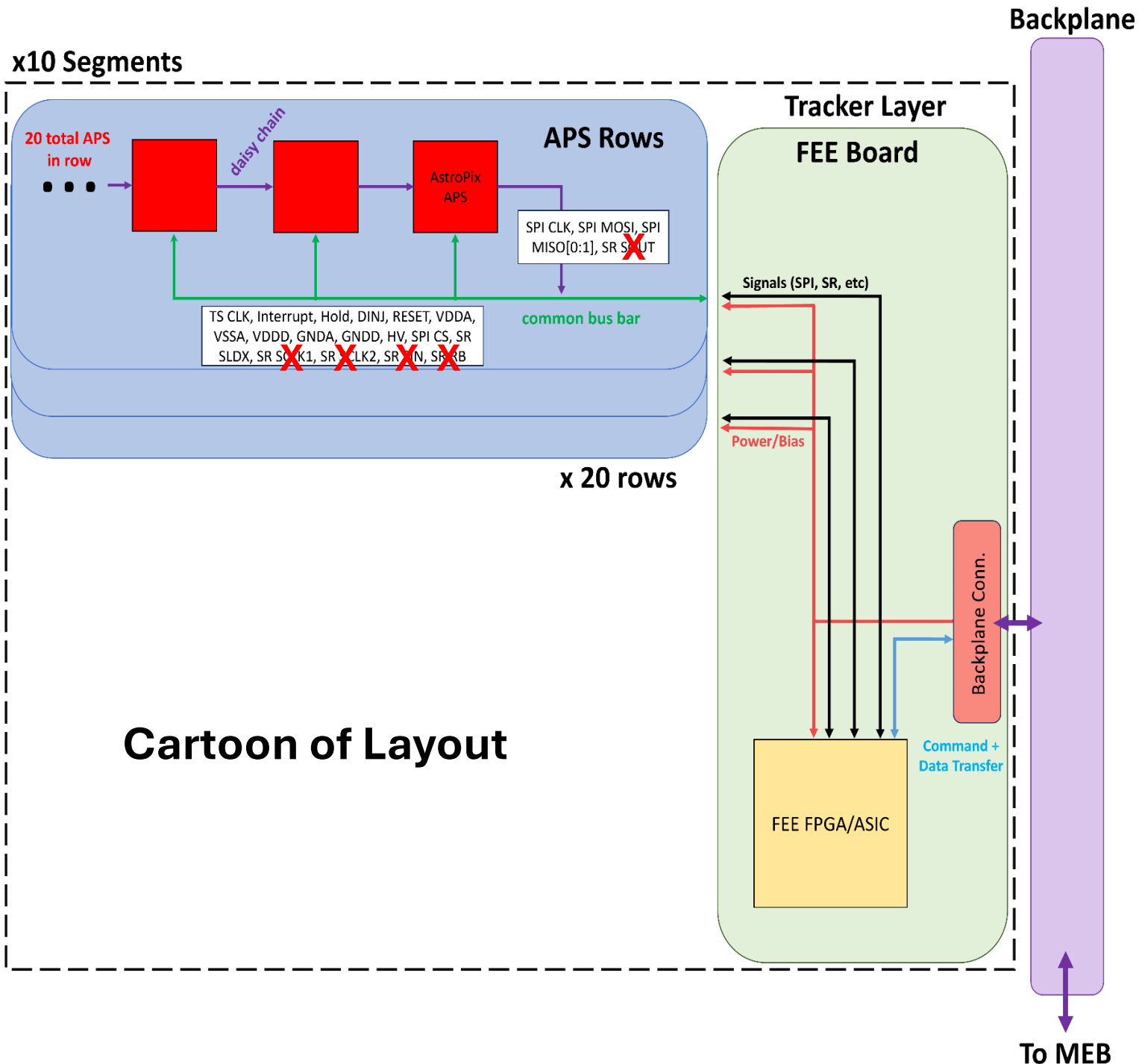
AstroPix-ComPair Interface

BIC Workshop 06/17/26

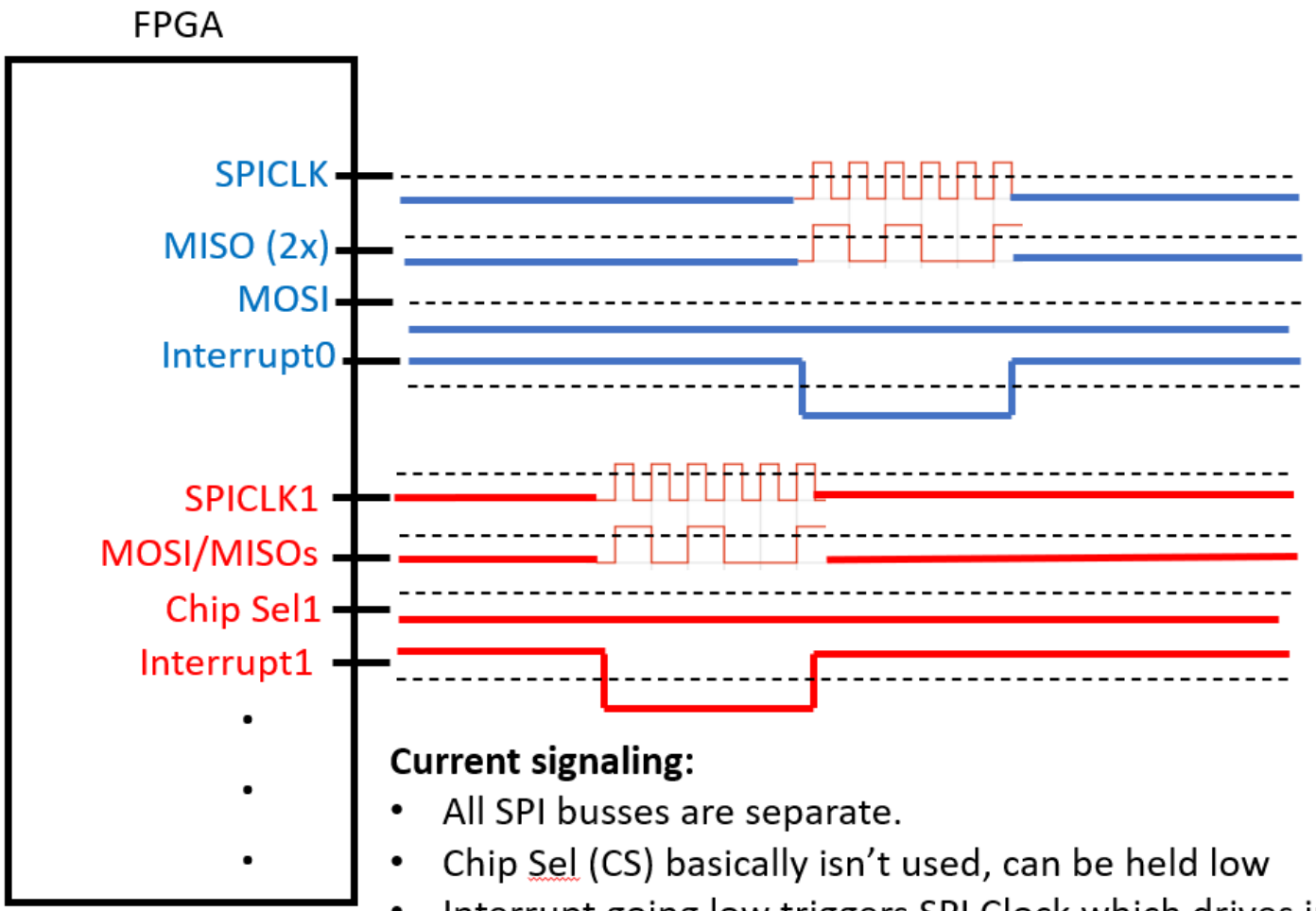
Background:

- Design implemented Compton-Pair Telescope (ComPair) Balloon Experiment
- Serves as prototype for future NASA instruments and BIC
- 20 Lanes of 18-20 AstroPix Detectors, 380 detectors total.
- Powered via flexprint PCB ‘Bus Bars’
- Science Data daisy-chained chip-to-chip then to Bus Bar.




Backplane
x10 Segments
Tracker Layer
FEE Board
APS Rows
20 total APS in row
daisy chain
AstroPix APS
SPI CLK, SPI MOSI, SPI MISO[0:1], SR SOUT
TS CLK, Interrupt, Hold, DINJ, RESET, VDDA, VSSA, VDDD, GNDA, GNDD, HV, SPI CS, SR SLDX, SR SCLK1, SR CLK2, SR IN, SR RB
common bus bar
x 20 rows
Signals (SPI, SR, etc)
Power/Bias
Backplane Conn.
Command + Data Transfer
FEE FPGA/ASIC
Cartoon of Layout
To MEB

Signal Chart:



Current signaling:

- All SPI busses are separate.
- Chip Sel (CS) basically isn't used, can be held low
- Interrupt going low triggers SPI Clock which drives individual readouts
- 3 Buses, 6 lines each (5SPI + Interrupt) = 18 total
- Ok for us but ultimately may be hard to scale to large areas with many parallel daisy chains

20x Interrupts, 20x CS per Layer

FEE for AstroPix v3 and v5:

- Simplified power, 1.8V is common and no VminusPix
- Options for differential SPI interface with AstroPix.
- Simplified Clock (SE or differential)
- New Timestamp Reset

BUS BAR IO	V3 Lines	V5 Lines	
POWER			
VDDA - 1.8V	1	1	
VDDA - 1.2V	2	2	
VDDD - 1.8V	3		
COMMON GROUND	4	3	
High Voltage	5	4	
VminusPix (V3 Only)	6		
DIGITAL IOS			
TS Clock	7	5	
TS Clock N		6	
Interupt	8	7	
Hold	9	8	
Digital Injection	10		
Chip Reset	11	9	
TS Reset		10	
ToT Clock (P for V3 ONLY LVDS)	12		
ToT Clock (N for V3 ONLY LVDS)	13		
SPI CLK	14	11	
SPI CLK N		12	**Can likely not use*
SPI CS	15	13	
SPI CS N		14	
SPI MOSI	16	15	
SPI MOSI N		16	
SPI MISO0	17	17	
SPI MISO0 N		18	
SPI MISO1	18	19	
SPI MISO1 N		20	
Analog Thermal Line	19		