EPIC BIC ETC

Evolving Concept

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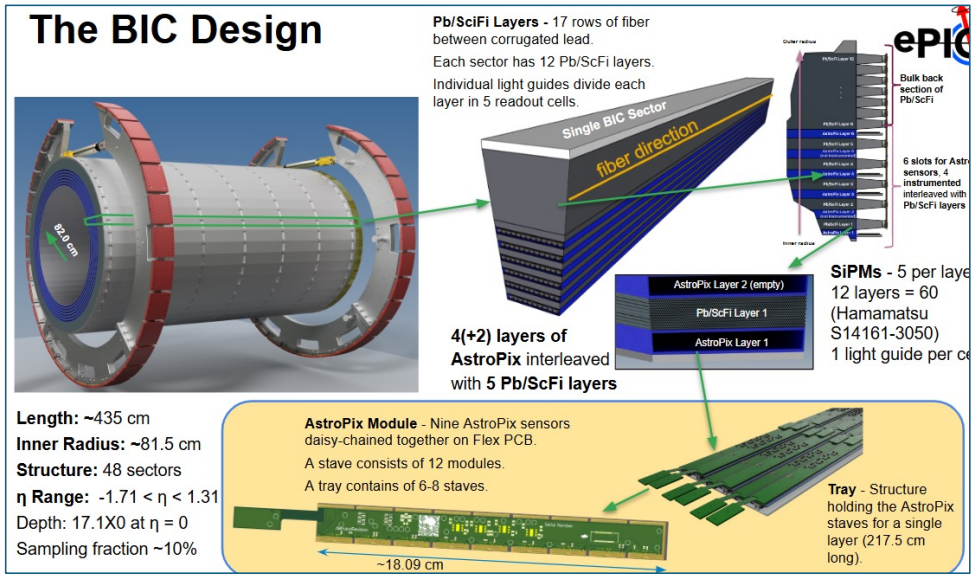
Compair2 FEE / BIC Prototype

- Using compair2 FEE as BIC prototype
  - Need BIC specific requirements
    - Radiation SEL, SEFI, TiD
    - IO and Power
    - Data rates
    - Buffering
- Form factor and power expected to change
  - Baselined at 1 ETC / FPGA per tray, 4 per ESB (End Sector Box)
  - 1 fiber link per ESB (currently using 100Mbit RGMII)

Context



Per side (two sides total):

48 sectors / side * 2 sides = 96 sector blocks = 96 ESBs

(6+7+7+7) staves/sector = 27 staves / ESB

12 modules / stave * 27 staves / (sector side) = 324 Module/ESB

9 asics/module * 12 mod/stave = 108 asics / stave

108 asics/stave * 6 staves = 648 asics / 6-tray

108 asics/stave * 7 staves = 756 asics / 7-tray

324*96 = 31104 modules per BIC

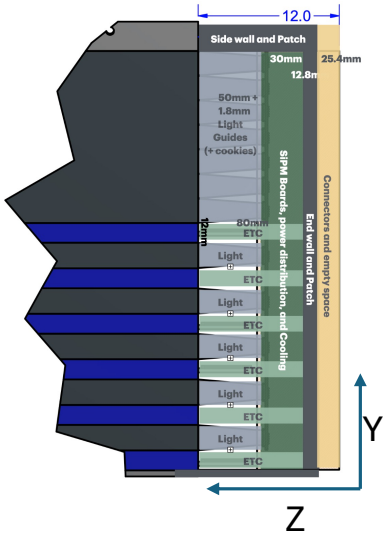
9*324*96 = 279936 ASICS per BIC

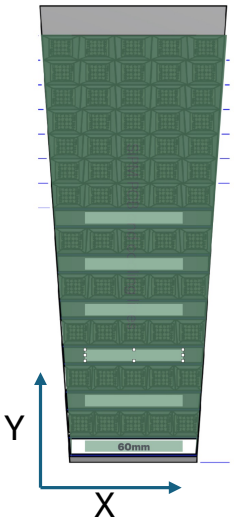
If 4x ETC per ESB, 384 ETCs per BIC

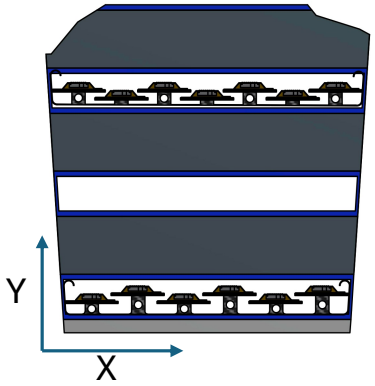
ETC Design Specifications (Per 1x Sector of 96)

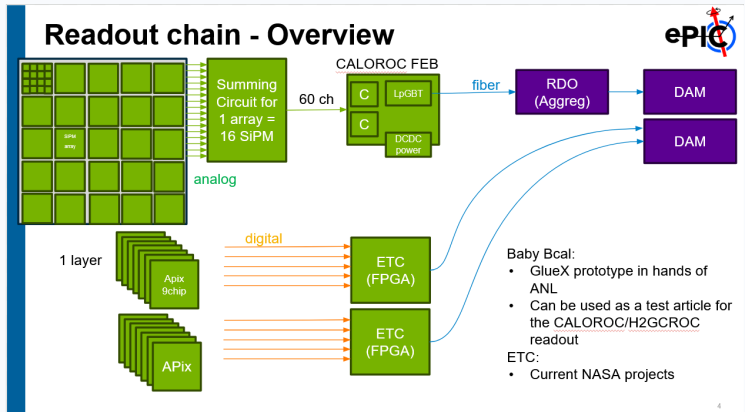
- ?? Interface 4x trays each with unique orientation of 6-7-7-7 staves 12 modules deep
  - Fanout 5V to each stave (438mA each at 1.8V and LDO 5.0V) 9V
    - 2.6~3.1 A per tray, 11.826A per ESB at 1.8V
  - Fanout HV Bias to each stave
    - 100nA per asic, 10.8uA per stave, 64-75uA per tray, 291uA per ESB
  - Interface each stave to FPGA
    - Unique IO FPGA to STAVE = MOSI, INTERRUPT, CS[11:0] = 14x
    - Non unique FPGA to STAVE = HOLD, 2.5MHZ, INJECT, SYNC_RST, ASIC_RSTn, SPI CLK = 6x
    - Unique STAVE to FPGA = MISO[1:0], INTERRUPT = 3x
  - Tray IO
    - 6+(14 + 3)*Stave = 108 per 6.stave.tray, 125 per 7 tray stave
  - ESB to ASIC IO
    - 108 + 3*125 = 483 IO assuming nothing common across trays

First iteration of questions









Assumptions based on PDR concept

- 1x ETC per tray, dimensions ~ 80mm x 60mm
- Each tray has unique placement and qty 6-8 staves.
- Stave location relative to ETC may shift in X and Y axis.
  - Unique Y-axis within a tray are accounted for using rigid-flex connection
  - Do X axis shits within a tray require a unique ETC per layer?
- Each ETC has SFP? fiber link to DAM

Questions:

- Power Interface, Power Budget per ETC, and power passthrough per stave? Yes
- High voltage passthrough? Yes
- Data rate per ETC (Additional memory for buffering needed? Peak streaming rate? Expected peak and average bits per second)
- Is fiber to DAM bi-directional, any other signals or interfacing? VTRX+ could aggregate for all ETCs in an ESB
- Parts Requirements and Reliability Class
  - Radiation (TID in krad, SEL Immunity in MeV), Exists but need to find
  - Thermal (Operating Temperature, Power Dissipation Budget, thermal path to ambient)
- Materials (Outgassing / contamination)
- Total IO count per Stave? Total per ETC? 100 per 6.stave.tray, 116 per 6 tray stave, 448 per ETC
- Housekeeping monitors
- Mounting holes? Wedge locks? Glue?

Rough diagram of ETC