5th BIC In-person Workshop, June 16-18, 2026

AstroPix-H2GCROC Synchronization

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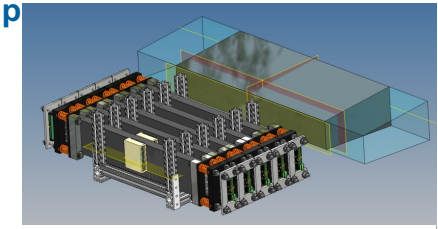
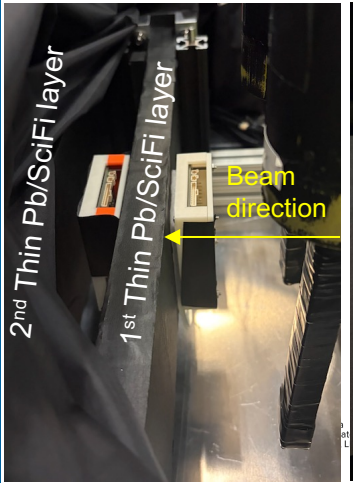
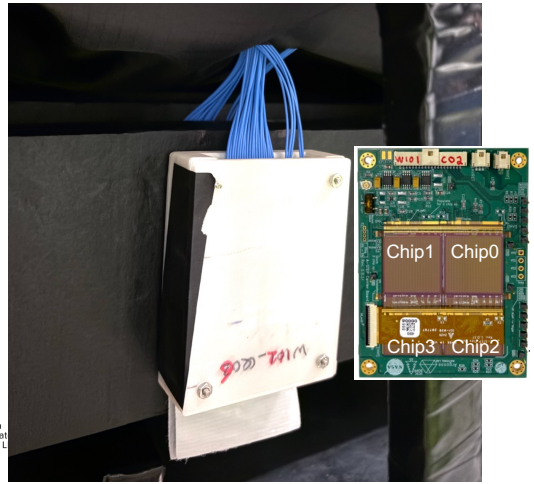
Hall D Beam Test: AstroPix setup

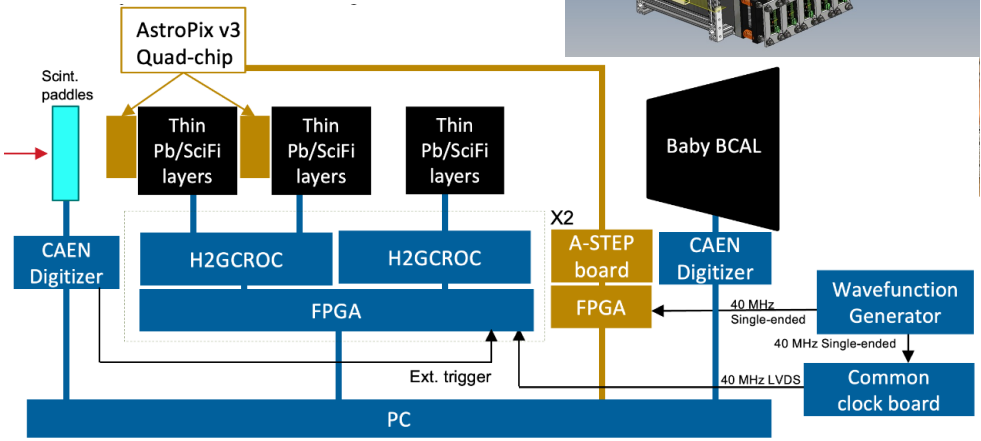
- Two Quad-chips + A-STEP (Astropix multichip/multilayer prototype readout system)
  - ✅ Confirmed the stable operation up to ~1.2 kHz beam rate at KEK beam test last year; promising stable operation under Hall D beam conditions.
  - W112Q06 + W101Q12 (chip0 malfunctional)
- AstroPix active area cover lower area of SFILs+H2GCROC
  - First integration of the Pb/SciFi and AstroPix readout systems under beam conditions at the 2026 Hall D beam test.
    - Common 40 MHz external clock distributed to both independent DAQ systems

→ How to define coincident events across AstroPixs and three SFILs using FPGA timestamp



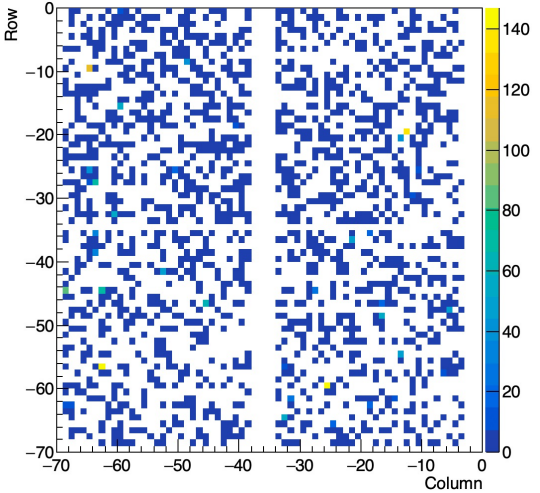


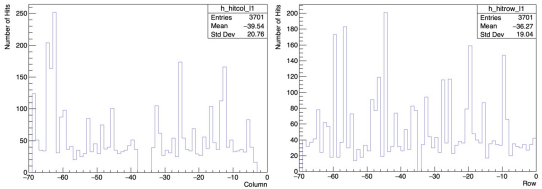




Hall D Beam Test: Beam profile measurement

- No beam (cosmic run)

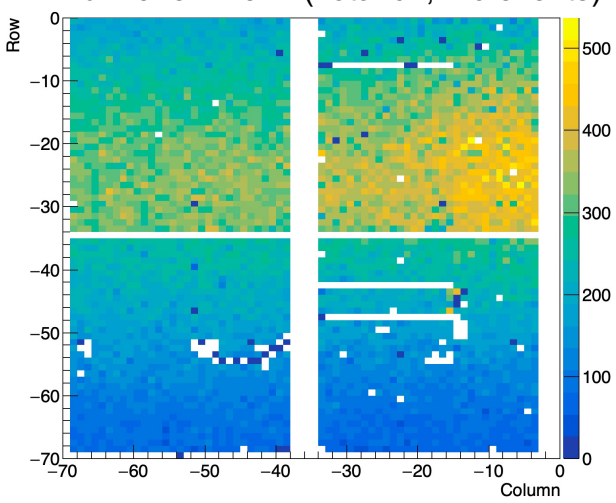


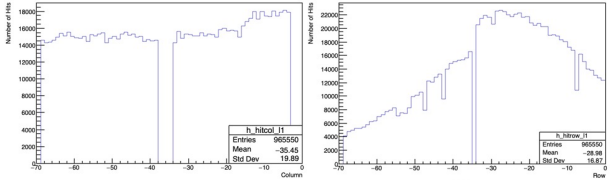


Run 1181-1191 (No beam (cosmic run))

- Expected cosmic-muon statistics: ~1,300 muons in a $4\ \mathrm{cm} \times 4\ \mathrm{cm}$ sensor over 2 h 44 min (~ $1\ \mathrm{cm}^{-2}\ \mathrm{min}^{-1}$, $\cos^2\theta$ distribution).

- Run1318 – 1324 (Total 61,416 events)

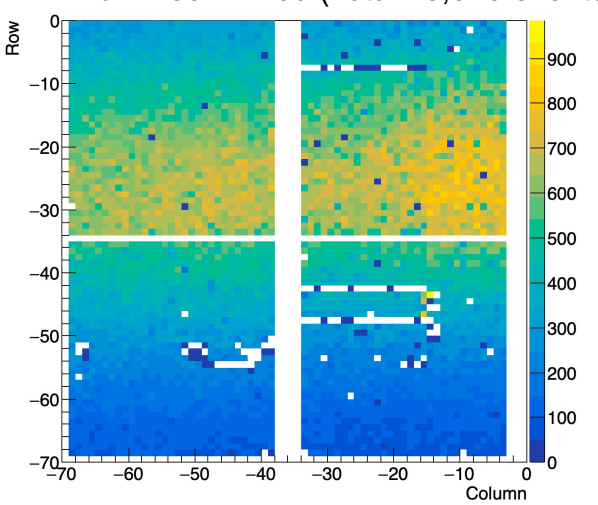


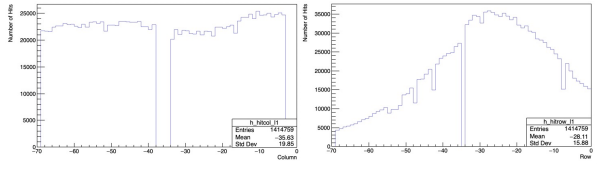


Run 1318-1324

- Hit map over 2 hours 20 mins of data-taking (5/13 6:45~9:06 AM)
  - ~ 100.6 Hz per matched hit
- <I> = 17.89~26.06 nA
- PS field: 0.190 T (~100A setting)
- Rad: JD70-107 55um 45/135 deg
- PSrad: HOME (out of beam) @ 0.000 mm
- TPOL: C (Be ~750μm?) @ 101.667 mm

- Run2483 – 2489 (Total 23,520 events)

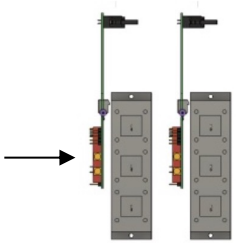




Run 2483-2489

- Hit map over 47 mins of data-taking (5/28 20:37~21:24)
  - ~ 100.6 Hz per matched hit
- <I> = 27.97~35.56 nA
- PS field: 0.244 T (~100A setting)
- Rad: JD70-107 55um 45/135 deg
- PSrad: HOME (out of beam) @ 0.000 mm
- TPOL: C (Be ~750μm?) @ 101.667 mm

Hall D Beam Test: interleaved with Pb/SciFi layer

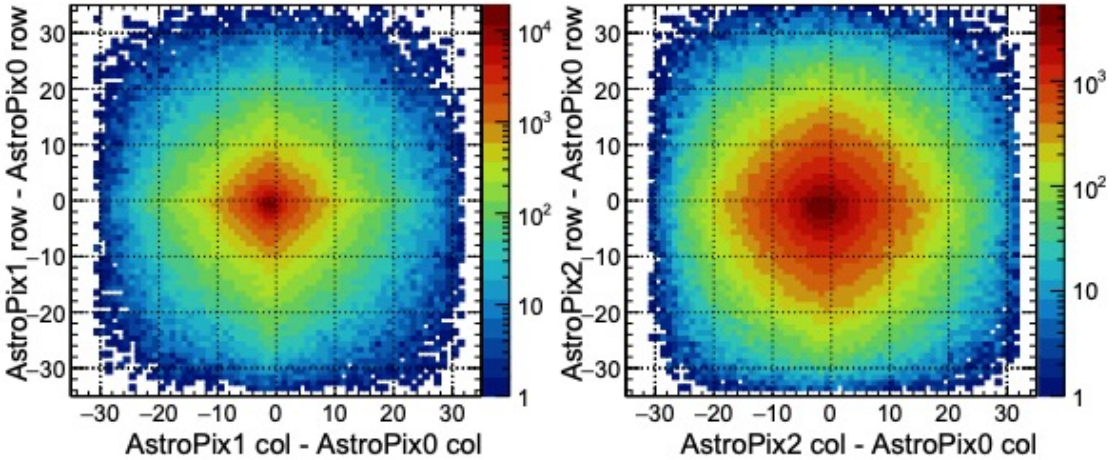


- Thin Pb/SciFi layer ~1.4 X_0

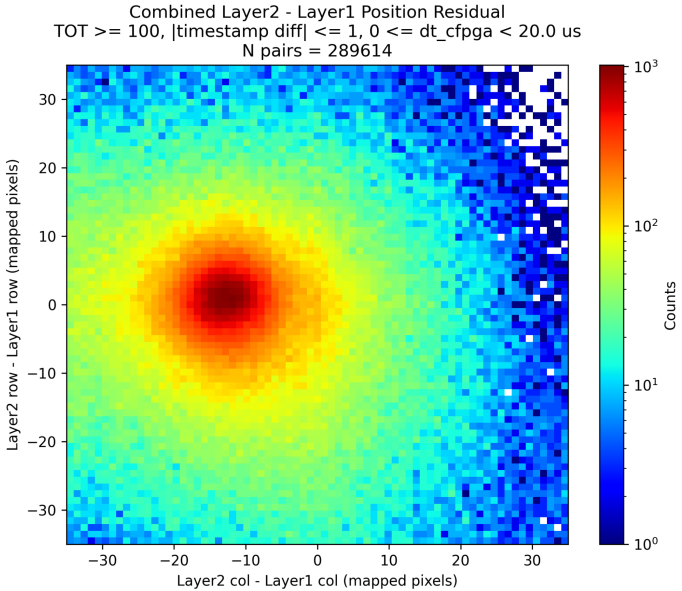
Applied cut

- Selected Layer-1 seed hits with ToT > 0.5 μs due to reduce noise
- Matched Layer-2 hits with |ΔAstroPix timestamp|≤1 (sharing AstroPix timestamp clock among all AstroPix layers)
- Required 0≤ΔFPGA timestamp<20 μs

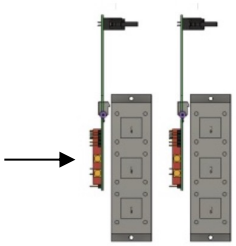
Three-layer of single chips with interleaved Pb/SciFi layer at KEK; 4.5 GeV electron beam (Y. Hong, ArXiv: 2605.07681, Submitted to NIMA)



500 MeV electron @ hall D



Hall D Beam Test: interleaved with Pb/SciFi layer



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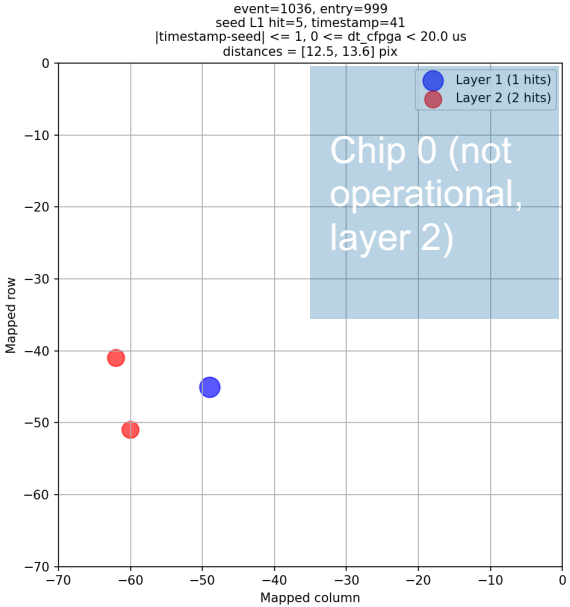
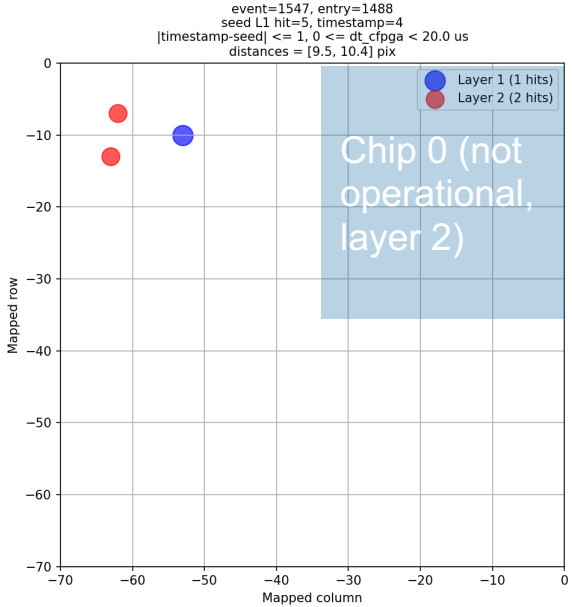
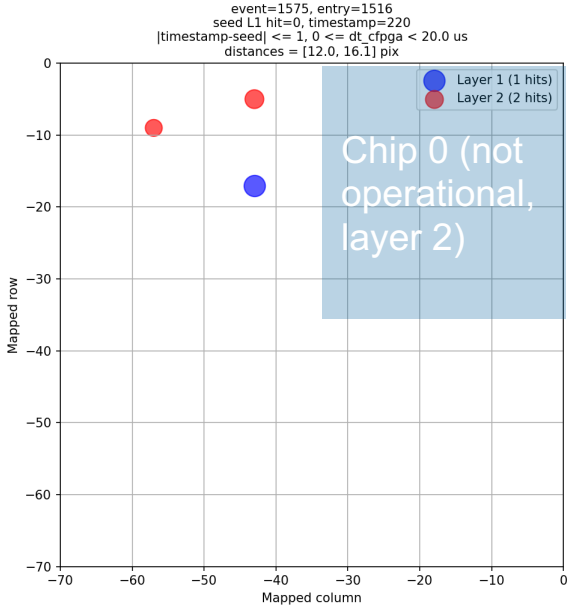




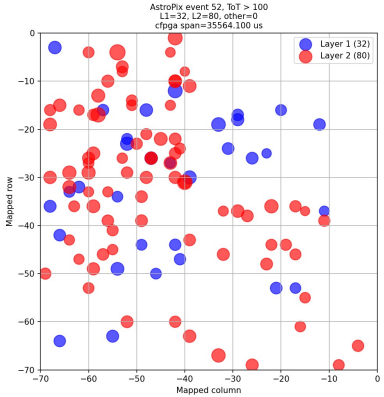


Hall D Beam Test: Synchronization

- Key Considerations for Synchronization
  - Common 40 MHz external clock distributed to both independent DAQ systems
  - FPGA timestamp clocks: 160 MHz for H2GCROC (6.25 ns/tick) and 40 MHz for AstroPix (25 ns/tick)
  - Different readout architectures
    - SFIL + H2GCROC: external-triggered event-based readout
    - AstroPix: self-triggered streaming readout
  - Time alignment between DAQ systems
    - FPGA timestamp offset
    - Trigger and buffering latency differences

- FPGA timestamps converted to acquisition time and validated against the overall data-taking duration
- Example plots: Candidate AstroPix event block (~35 ms) and a selected KCU0 waveform from three SFILs
- Ongoing work: timing corrections for true event coincidence matching

Work in Progress



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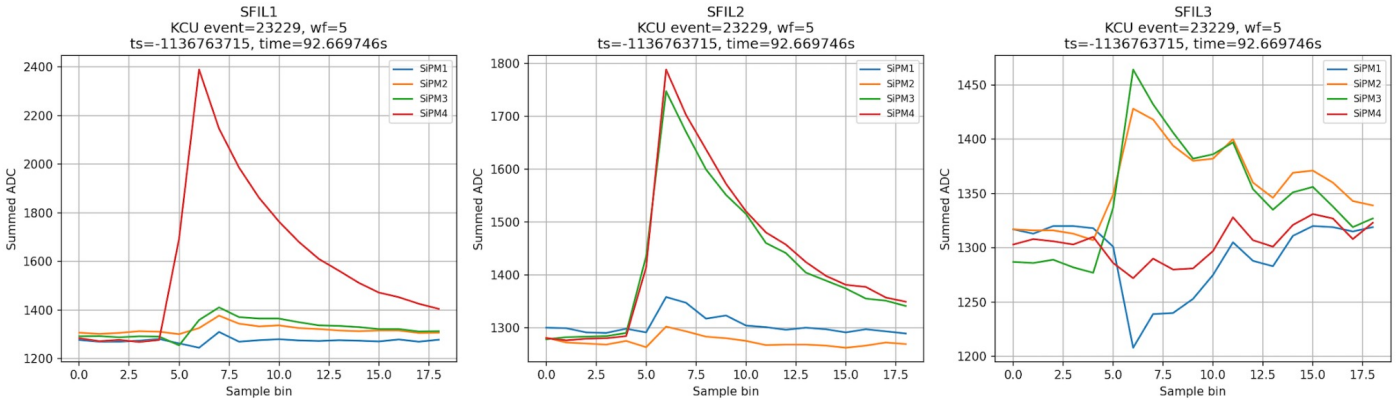
Work in Progress



Synchronization: AstroPix using KEK beam test

FPGA timestamp study using 3-layer of quad-chips beam test at KEK in Dec. 2025

- Share AstroPix timestamp clock among 3-layer of quad-chips: applying |ΔAstroPix timestamp|≤1 for finding coincident events
  - 2.5 MHz for AstroPix timestamp (400 ns/tick, 8 bits), 40 MHz for FPGA timestamp (25 ns/tick, 32 bits), 200 MHz (5 ns, 12-bit) for ToT clock
- Observed the correlation between difference fpga timestamp and ToT among layers
  - → Different FPGA bitfiles were used for the KEK and Hall D beam tests; Recheck the FPGA timestamp tick using the Hall D data

→ Applying timing cut: $dt_{Correct}$ = Δfpga_ts - Δtot < 20 us

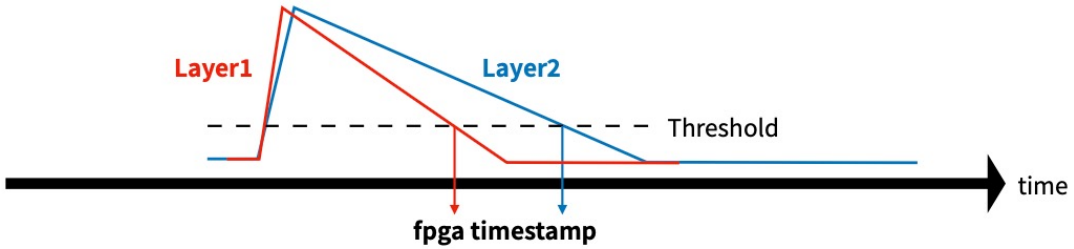
→ For finding coincident events: 1st layer Hit, $\mathbf{t_{arrival}}$ **= fpga_ts – tot**

What makes fpga timestamp different?

By Y. Hong

fpga timestamp seems to record the timing when the SPI signal comes out

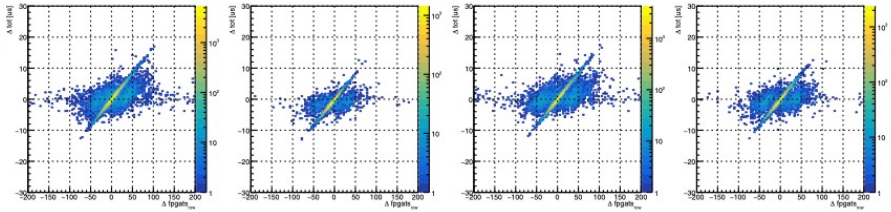
SPI dead time equivalent to ToT(Time over Threshold)

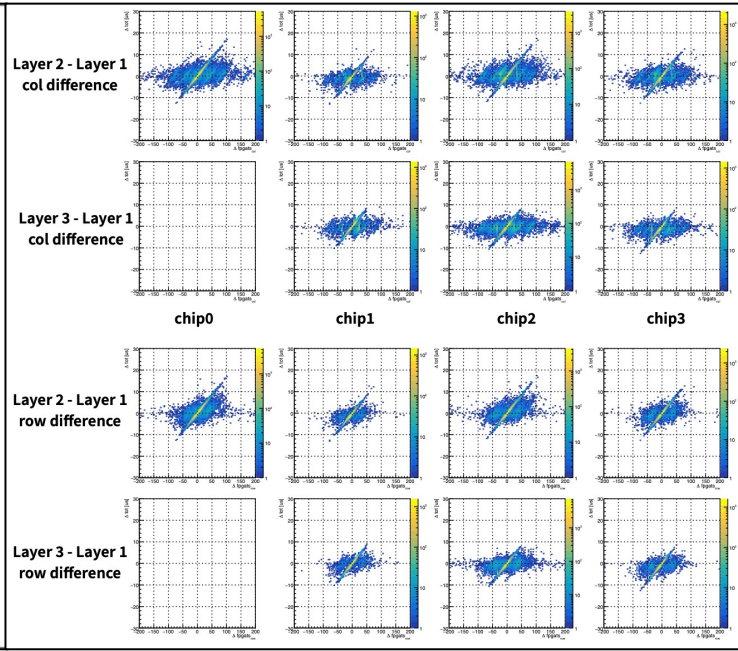


x: row fpga timestamp difference

y: tot difference

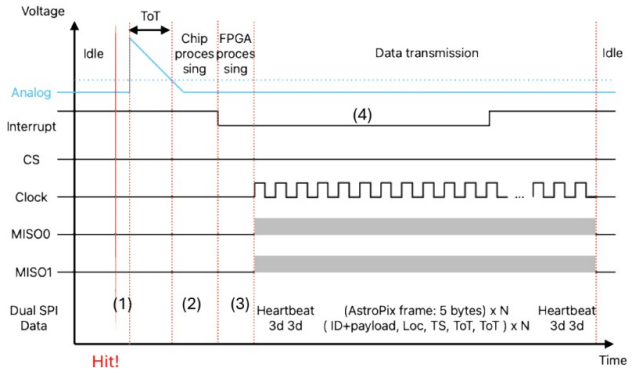
btw. Layer1 & Layer2





Synchronization: AstroPix and H2GCROC

Autoread choreography (wildly not to scale)



(1) Delay before analog signal starts to rise ~40 ns (measured with digital injection)
(2) Chip processing: 1.5 to 2.5 µs
(3) FPGA processing: ≲ 1 µs, depends on FPGA clock?
(4) Interrupt is low for 11 to 12 clock cycles

Slide from Adrien

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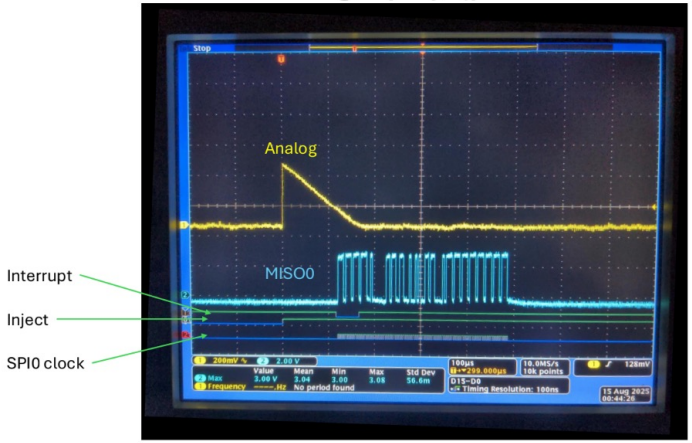
Autoread choreography (partial, but to scale)



300 mV injection
CMOD board
W08Q05 chip 1
150 mV threshold

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AstroPix (by Adrien)

- the chip TS is set at the end of the ToT period. (not 100% certain yet)
- the absolute time of an event in AstroPix should be: "chip_TS - ToT - constant +- jitter" within a +-100 us window, and the FPGA TS is only used to differentiate 100us windows.
- FPGA TS = last rollover time + chip TS + ToT + data_transfer_time((chipID + 1)*8) + constant
- Last rollover time = (FPGA TS - ToT - transfer_time) % (chip TS rollover period)
- Trigger absolute time = Last rollover time + chip TS

H2GCROC (by Norbert)

- KCU timestamp is expected to provide an absolute time reference independent of chip ID.
- No chip-dependent timing correction is expected, since the data-transfer delay is identical for all chips.
- The KCU timestamp should already represent the absolute event time, in principle.

→ Once the absolute time is available from Astep + AstroPix, we can directly compare it with the KCU timestamp.

Back up