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AstroPix Perspectives

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U.S. DEPARTMENT of ENERGY
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AstroPix Imaging Layer R&D Milestones

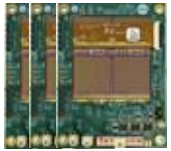
- AstroPix Multilayer/Multichip demonstration
- First beam-test operation of the 9-chip AstroPix prototype module (AstroLinx mock-up)
- Integration between H2GCROC (Calorimeter readout) and A-STEP board (AstroPix readout) using external common clock

AstroPix v3

Single chip

Quad-chip

Three-layer of quad-chips



9-chip prototype PCB module

Three-layer of 9-chip PCB modules

AstroPix v4

AstroPix v5: Chip delivery is expected in Oct. after the fabrication process.

+ ETC (Final AstroPix readout system, designed and developed by NASA)

Configuration of **AstroPix v4**	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (KEK, Dec.2025)

Configuration of **AstroPix v3**	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (FNAL, Jun.2024) (arXiv:2602.06084)
Three-layer of single-chips	Three GECCO boards + customized DAQ	1x3	✅ beam tests (CERN & KEK, 2025 summer) by Korean team (arXiv:2605.07681)
Quad-chip	A-STEP FPGA board	2x2	✅ bench/beam tests (KEK, Dec.2025)
Three-layer of quad-chips	A-STEP FPGA board	3x(2x2)	✅ bench/beam tests (KEK, Dec.2025) (two quad-chips, Hall D, Jun. 2026)
9-chip prototype PCB module	A-STEP FPGA board	1x9	✅ bench test/beam tests (KEK, May.2026)
Three-layer of 9-chips	A-STEP FPGA board	3x(1x9)	Ready to test; (beam test in Aug.2026)
Three-layer of quad-chips + Three-layer of 9-chips	Two A-STEP FPGA boards + external clocks	3x(2x2) 3x(1x9)	Ready to test; (beam test in Aug.2026)

What We've Done with AstroPix v3

MIP response (support muon ID with sufficient dynamic range in all layers)

B. Kim, ArXiv: 2602.06084, Submitted to NIMA

- V3 Single-chip (-150 V and 200 mV threshold): 34 ± 1.9 keV in 25 keV~200 keV using 120 GeV proton at FNAL (6.2024)
- V4 Single-chip (-175 V and 140 mV threshold): 37.9 ± 1.4 keV using 3 GeV electron at KEK (12.2025) Manuscript in preparation

Hit efficiency

- Three-layer of single-chips : bias voltages from -150 V to -400 V → 40~68% ← Y. Hong, ArXiv: 2605.07681, Submitted to NIMA
- Three-layer of quad-chips : bias voltage of -150 V → 45%~57% (per layer, per chip)

Measure EM shower development

- Three-layer of single-chips interleaved with Pb/SciFi modules: using electron and pion beam at KEK and CERN (2025)

Stable operation under beam condition (readout capability with the current setup)

- Three-layer of quad-chips: stable data-taking up to 2.4 kHz at KEK (12.2025)
- 9-chip prototype module: stable data-taking up to 2.7 kHz at KEK (5.2026)
- The per-chip measurement on the 9-chip prototype (~1.6 kHZ) meets imaging-layer data-rate. (~1.18 kHz per chip: Max. expected data rates for imaging layers, taking into account DIS, electron, and proton beam backgrounds)

Integration between H2GCROC and A-STEP board using external common clock

- Two layer of quad-chips: beam test at Hall D (3~6.2026); Event matching based on absolute timing using FPGA timestamps is ongoing.

What's left/gain for upcoming Aug. beam test?

(AstroLinx and v5 not available until Aug.)
Three-layer of quad-chips + Three-layer of 9-chips

- event display of shower imaging
  - limited by v3 hit efficiency and readout
- e/π separation using both Pb/SciFi and AstroPix information
  - Korea team working on it using beam test data collected by customized DAQ at KEK and CERN (2025)

Can we make more 9-chip prototype module (or Quad-chip)? How many? (*Quad-chip: mainly for NASA space mission)

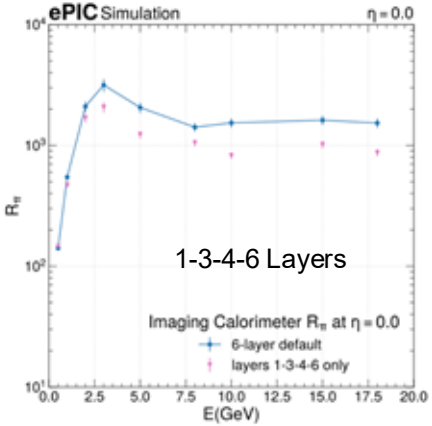
How many AstroPix 9-chip module/quad-chips can we send/use CERN beam test as well as Hall D?

→e/π separation study (AI-ready beam test data as well), data collected by H2GCROC and A-STEP board

→Last chance to take pion beam?

→Validate 1-3-4-6 layers configuration?

- → Required two A-STEP at least
- → Among AstroPix setup, synchronization using 40 MHz external clock
- → Required very low beam rate!

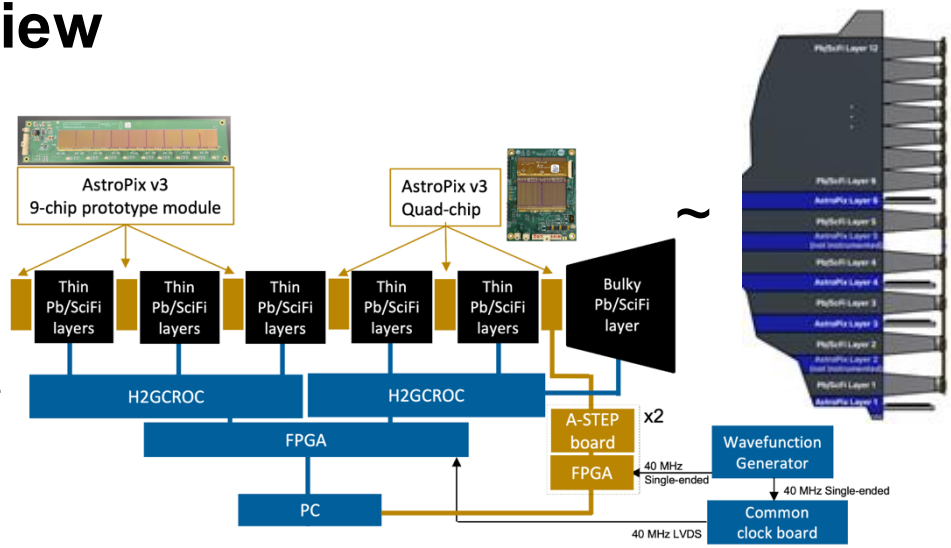


or 2-3-4-6 layers?

Toward the Final Design Review

Future Beam Test

- Near-full-sector prototype
  - 6 Pb/SciFi layers
  - 6(4) AstroPix multichip layers
- Energy resolution/Timing resolution
- e/π separation using both Pb/SciFi and AstroPix info.
- 3D shower imaging validation



- Remaining items toward the final design review
  - AstroPix v3
    - AstroLinx
    - Module test article → Half-stave test article → Stave
  - AstroPix v5
    - Chip delivery is expected in Oct. after the fabrication process.
    - Single chip performance test + GECCO board
    - Multi-layer/Multi-chip + ETC board