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# Status report of the eRD109 project on SALSA chip development

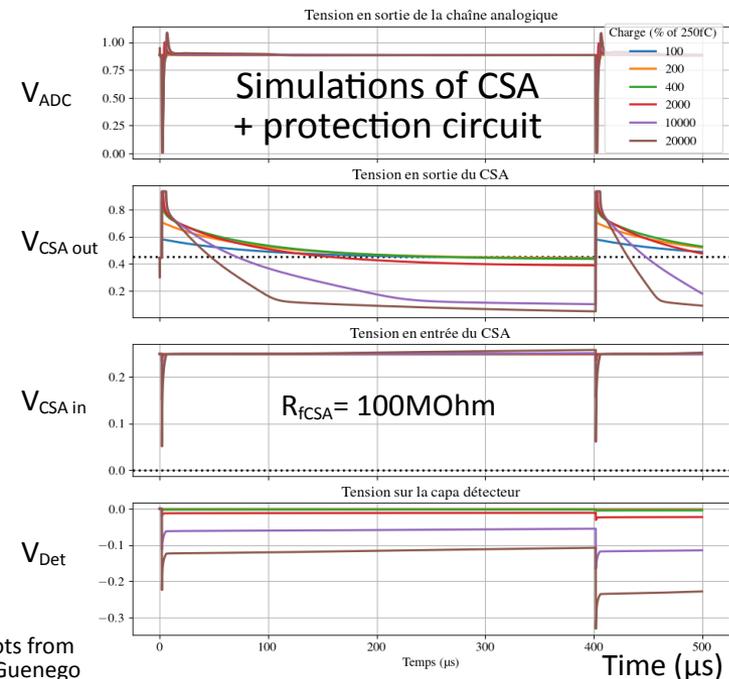
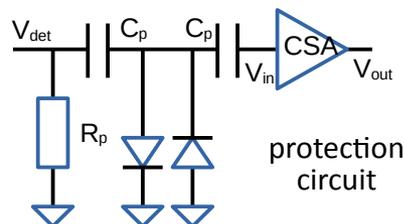
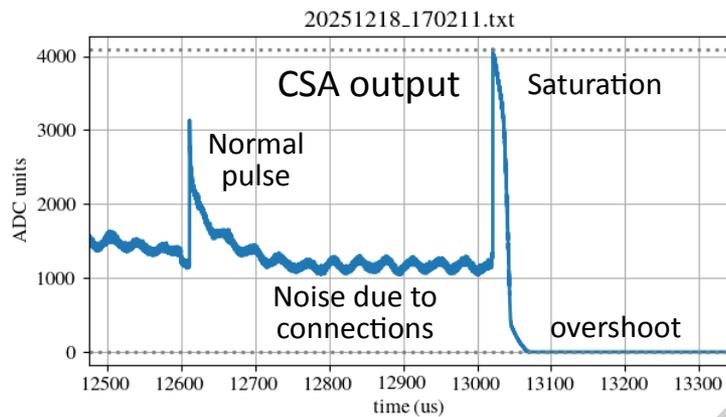
Damien Neyret (CEA Saclay IRFU) for Sao Paulo  
University and CEA IRFU teams  
EPIC DAQ/electronics WG meeting  
12/2/2026

## PRISMEv1 prototype (PLL test chip)

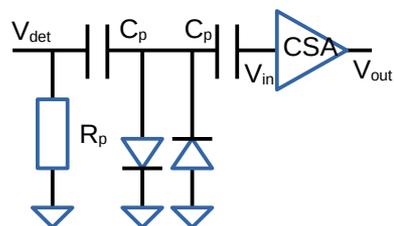
- Used to do tests of high-speed links and CDR decoding (implemented in PLL)
- Radiation tests postponed again by CERN → May-June (idem for SALSA1). Also searching for another radiation facility but not easy to find calibrated gamma source

## SALSA1 prototype

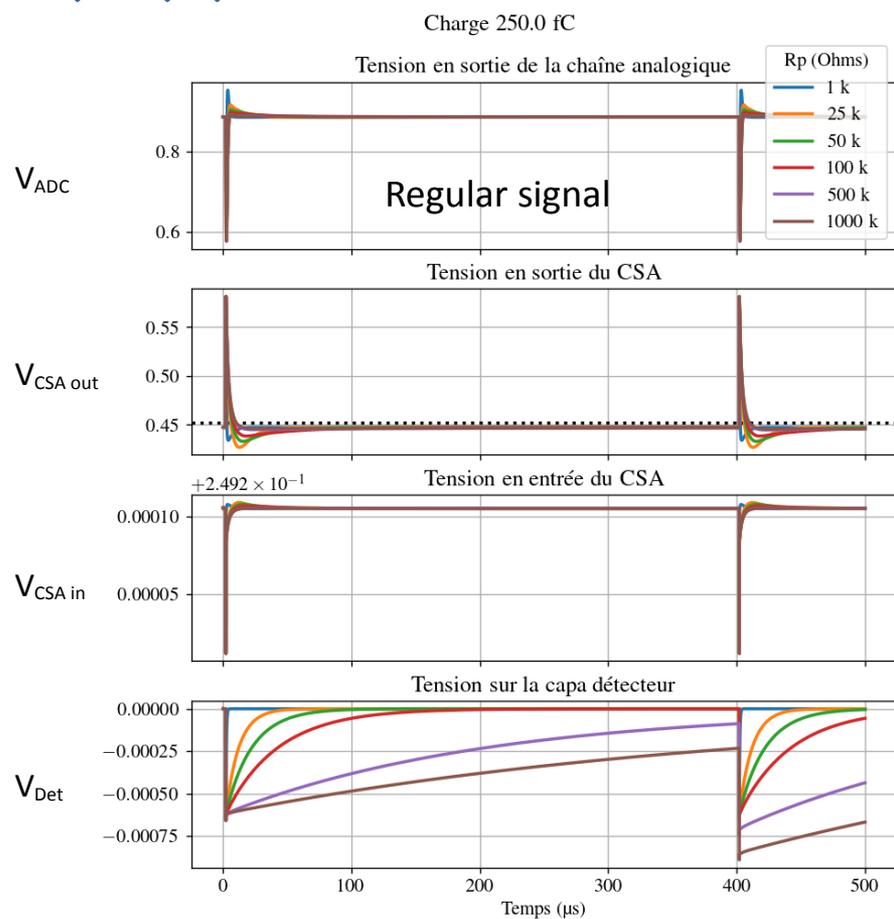
- Tests on SALSA1 connected to real MPGDs with 1 MM strip connected to 1 channel
- Tests with  $^{55}\text{Fe}$  source and cosmics, also with some sparks
- Study on effects of sparks and large signals (large HV on detector) on CSA charge amplifier
- Overshoots observed in CSA, likely due to protection circuit effects, reproduced in simulations



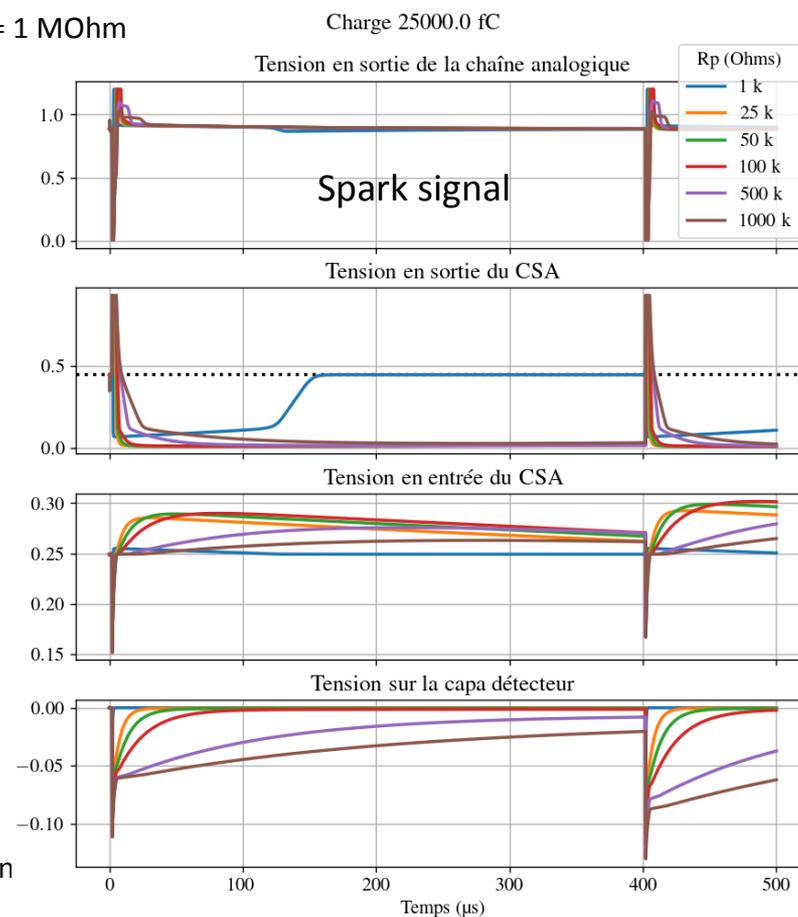
Plots from B. Guenego



## Simulations of CSA + protection circuit with different $R_p$ resistors



$R_{fCSA} = 1 \text{ MOhm}$



Time<sup>3</sup> ( $\mu s$ )

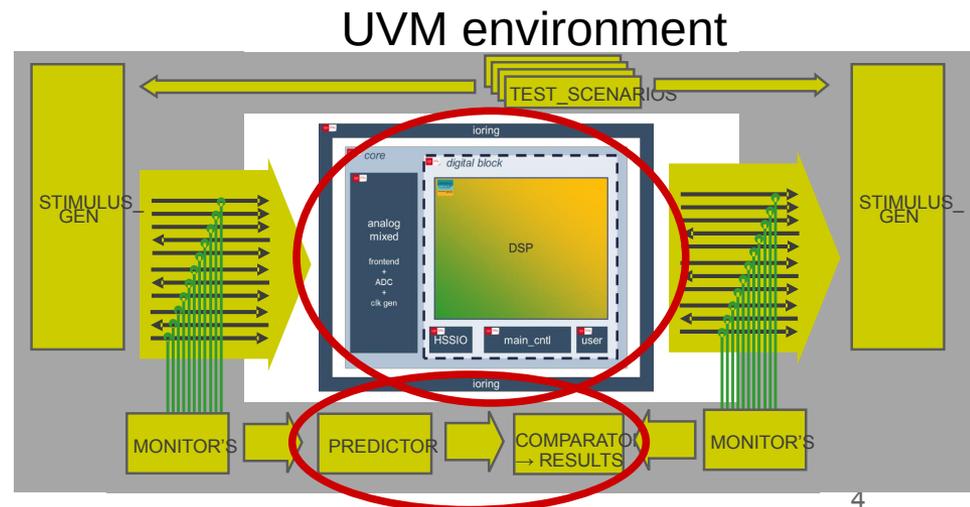


## SALSA2 development status

- DSP verification ongoing, starting to use real signals from SALSA1 tests
- Integration in rest of digital environment ongoing, still some interface discrepancies to manage
- Behaviors of fast synchronous commands defined. Management module development ongoing
- Updates to be done on states of main state machine, work ongoing
- Input link synchronization state machine with traditional interface done, work on unified interface postponed as not priority (not used at ePIC)
- Some simplifications done on clock manager, to speed up verification steps
- Floor plan: integration of analog part ongoing; evolution of pin-out definition to integrate start-up configuration pins
- UVM environment: work still ongoing on integration of DSP; + integration of code simulating front-end part

## Timeline

- Still a lot of works ahead:
  - code validation
  - integration of all modules, validation
  - digital layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission foreseen 1<sup>st</sup> semester 2026, but could be optimistic
- Tests from end of 2026 or beginning 2027
- Distribution to users in 2027





## ■ eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming 1<sup>st</sup> semester 2026
- Beginning of SALSA2 tests → 2<sup>nd</sup> semester 2026 or beginning of 2027

## ■ eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 1<sup>st</sup> semester 2026
- SALSA3 submission → 1<sup>st</sup> semester 2027
- Performance evaluation → 2<sup>nd</sup> semester 2027 - 1<sup>st</sup> semester 2028

## ■ Very next steps

- SALSA1 tests → Tests on MPGD prototypes, TID tests in May or June hopefully...
- PRISMEv1 chip → TID tests in May or June
- SALSA2 development → in progress