FCFD status

Artur Apresyan

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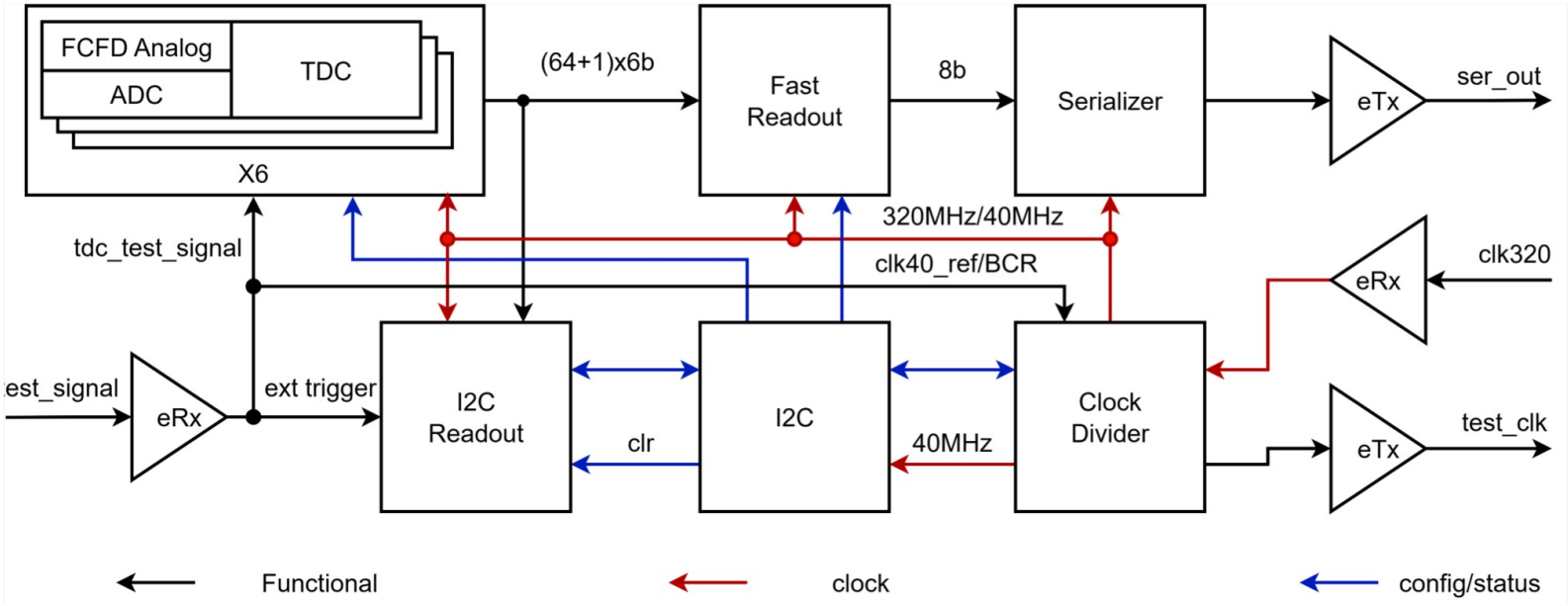
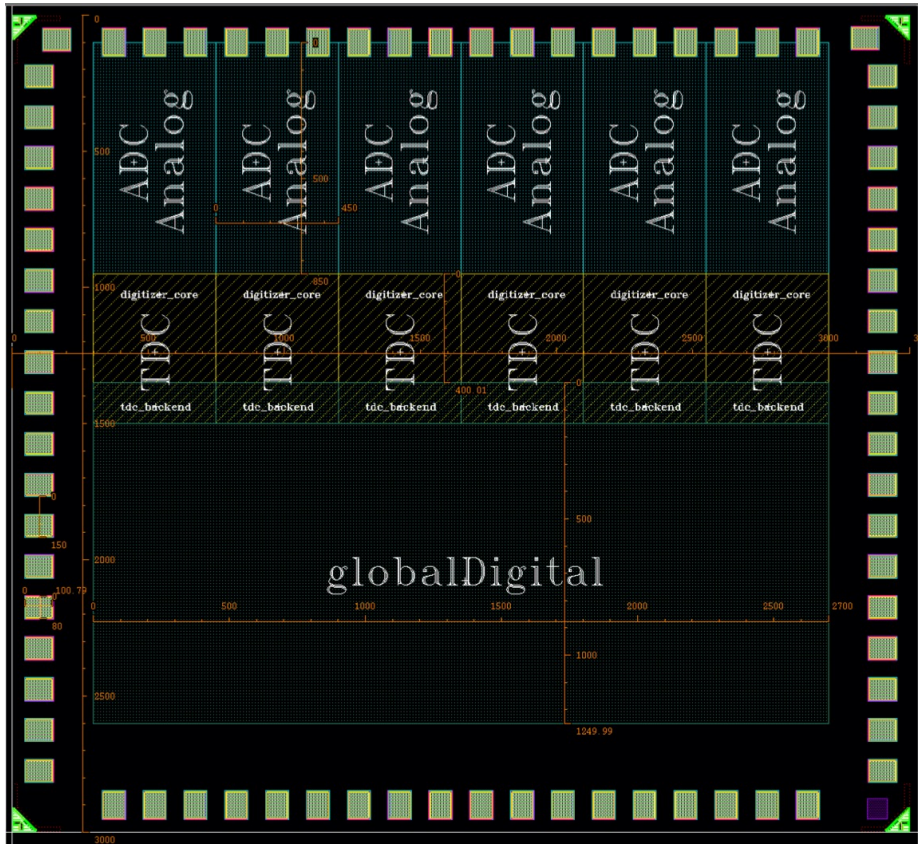
Design status for FCFD1.2

- Timeline for submission is fixed now
  - Tape-out on April 19
- Pre-submission design review was held on Feb 5
  - Review committee report will be circulated soon



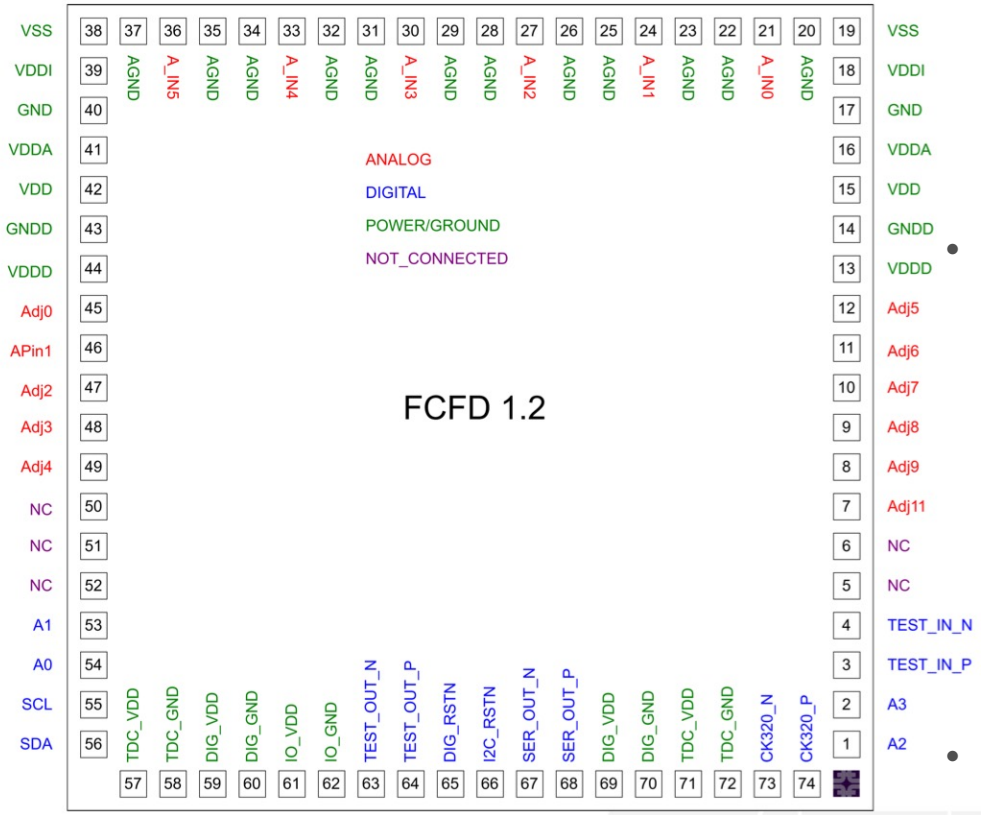
FCFD1.2 floorplan

- Chip size: 3300x3000 um
- 6 channels, 450 µm width per channel
- Analog integration for several large modules:
  - Frontend (ADC included), 6 TDCs, globalDigital and pad ring.



Current floorplan and pads

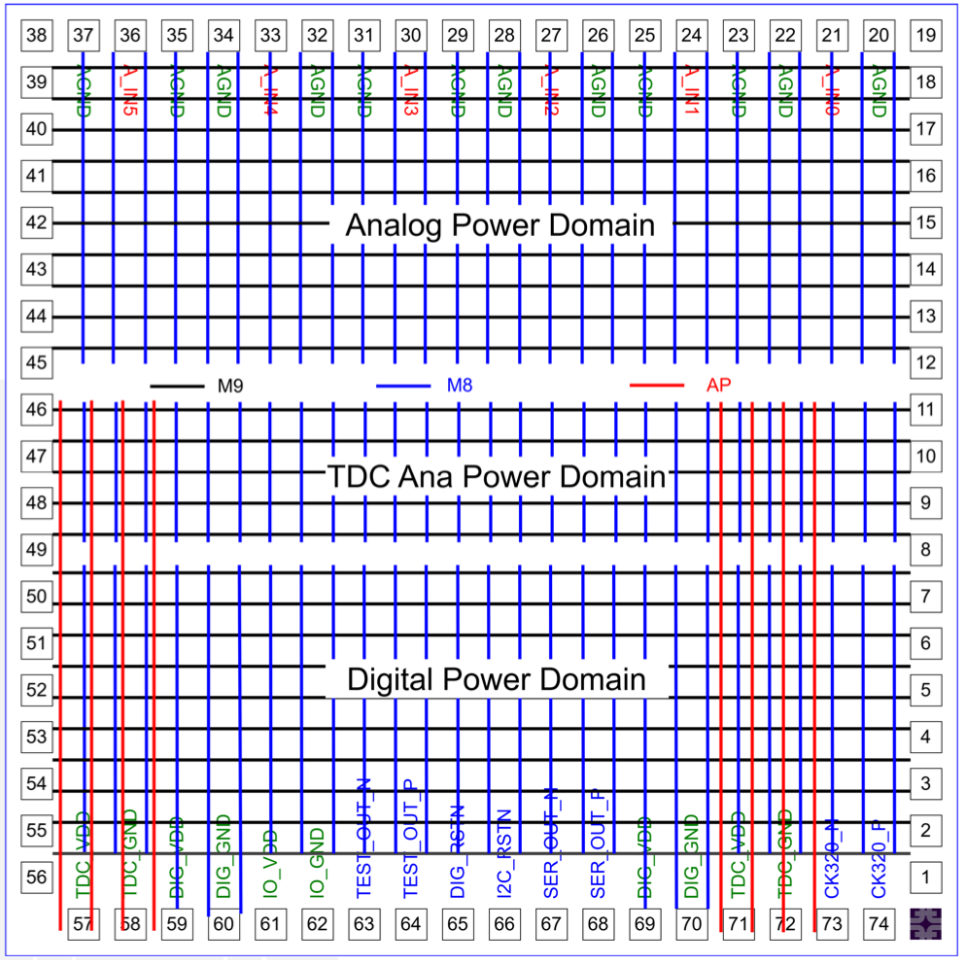
FCFD1.2 I/O



- Total 74 pads:
- 43 pads for analog frontend
  - Power supply/ground pads: 12
  - substrate pads: 2
  - Biasing adjustment:11
  - Input and shielding pads:18
- Essential function pins (16):
  - ser:2 (side)
  - clk320:2
  - reset:2
  - test_in:2
  - test_out:2
  - I2C(SCL/SDA, Addr):6
- Power supply pins at bottom(10):
  - Digital:4
  - ESD power/ground: 2
  - TDC:4
  - Not connected: 5

FCFD1.2 Power Grid

- Three main power domains:
  - Analog/TDC ana/Digital
- M8/M9 are used for local power grid.
- AP layer only used for TDC analog power domain from pads.
- The analog substrate is isolated with high resistant NT_N band.



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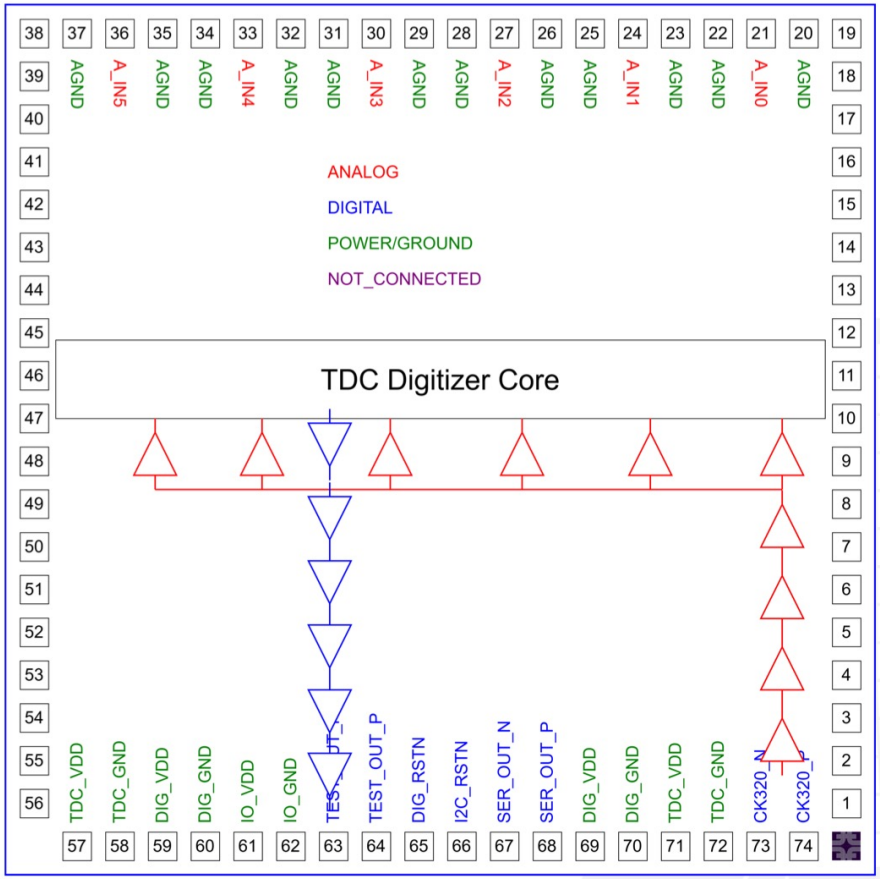
FCFD1.2 Clock Distribution

- Clk320 routed in digital power domain with clearance to other digital circuits.
- A return clock signal is output for test purpose.



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Schedule for FCFD for barrel TOF

- FCFD1.2: Jul 2026, available for system-tests
- FCFD2.0: Fall 2027, available for system-tests
- FCFD3.0: Dec 2028, Production