

OSU Light Collection

2/10/25

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List of available sample tiles

Polished+milled to correct size

- ~20 2.4x2.4x0.4 with dimple
- 1 2.4x2.4x0.4 painted with dimple
- 3 4.7x4.7x0.4 with dimple
- 1 4.7x4.7x0.4 painted with dimple
- 1 4.7x4.7x0.4 wrapped with dimple
- 2 5x5x0.4
- 1 5x5x1.6
- 1 10x10x1.6



Will show results from this one today

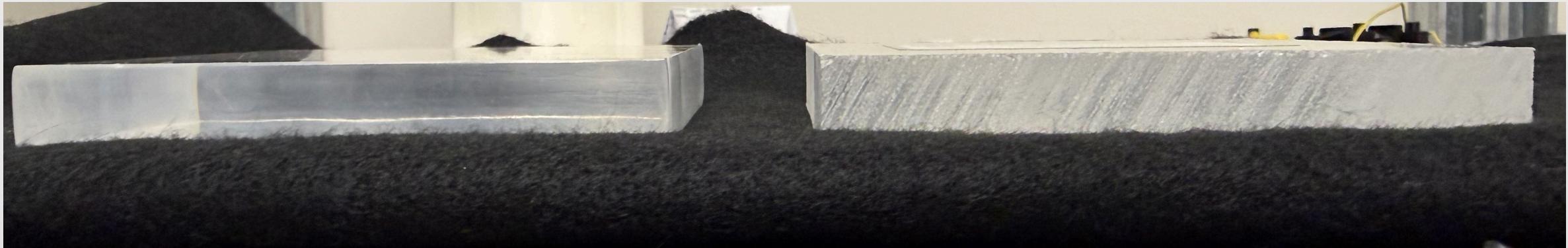
Unpolished+not milled to stated size.

- 3 5x5x0.4
- 2 5x5x0.8
- 1 5x5x0.8 with dimple
- 3 5x5x1.6
- 1 10x10x0.4
- 1 10x10x0.4 with dimple
- 3 10x10x0.8
- 3 10x10x1.6

About ~2cm
extra material
in x,y

Polishing the unpolished tiles

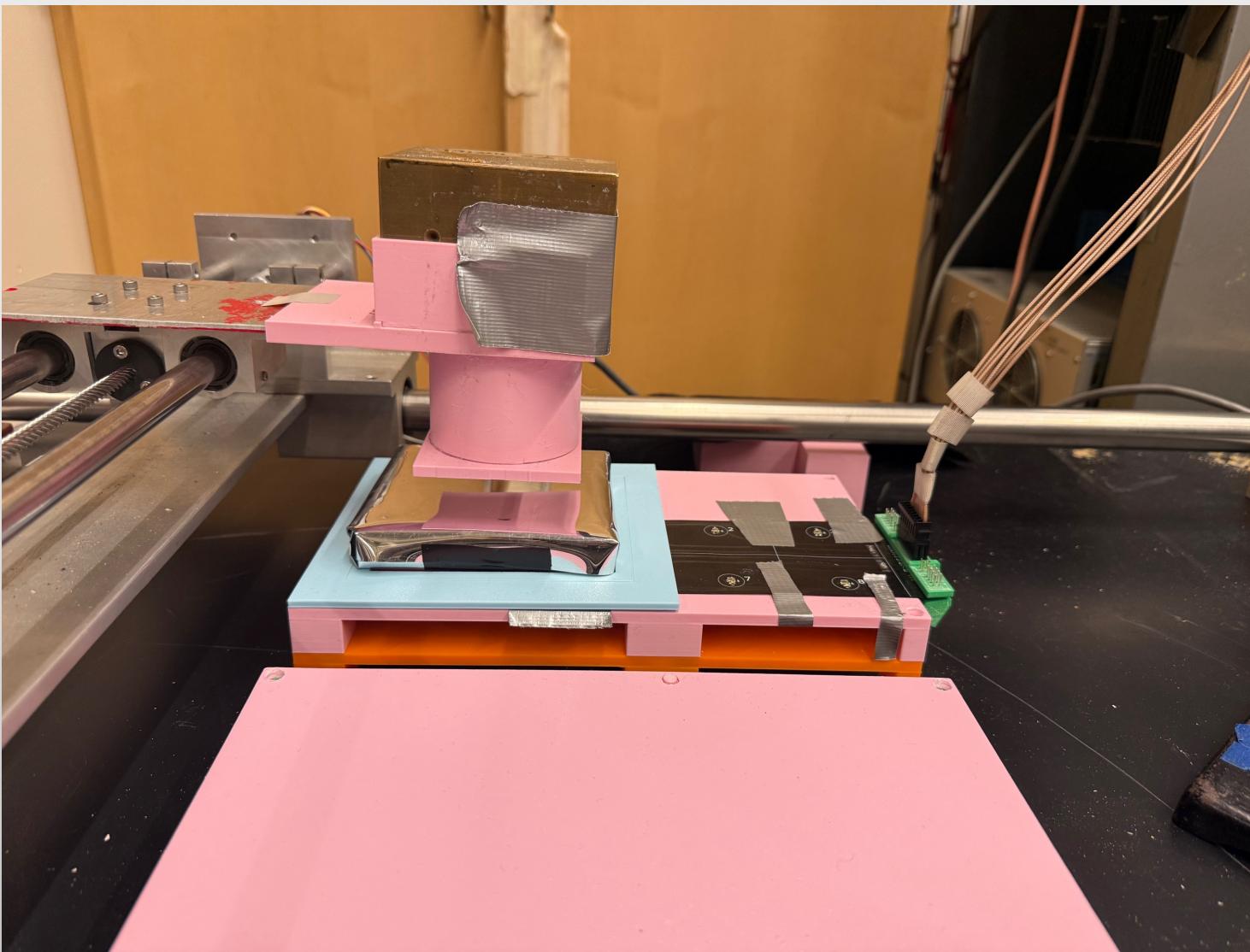
- Recently started polishing some of the un-milled tiles by hand.
- Here's an example



Polished

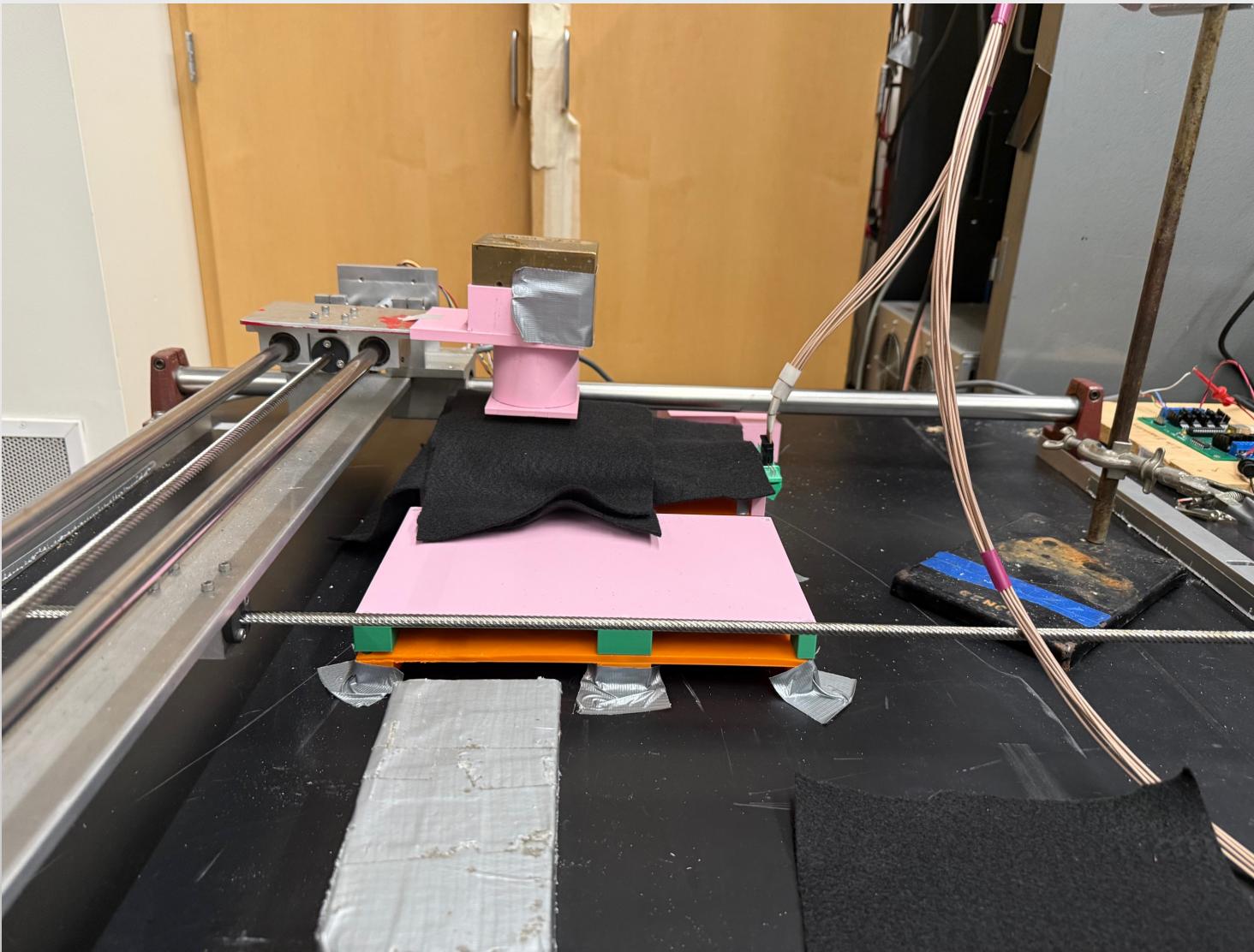
Original

Lab setup



- Sr90 beta source
- Source oved through a list of positions via x-y table
- Tile centered over SiPM
- Readout through CAEN module

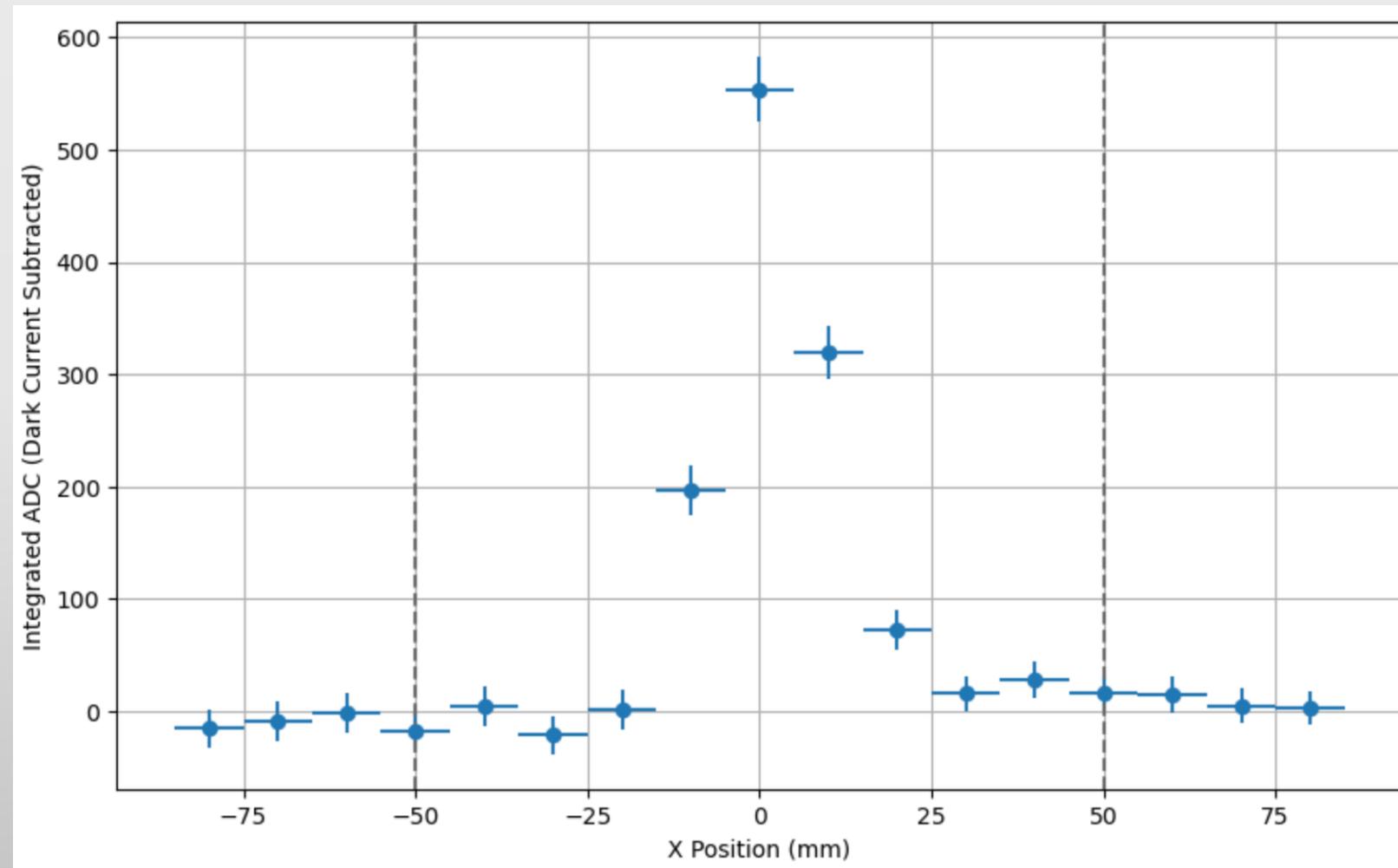
Lab setup (pt 2)



- For data taking, cover tile with felt and turn off the lights

Results from unwrapped, polished 10x10 tile

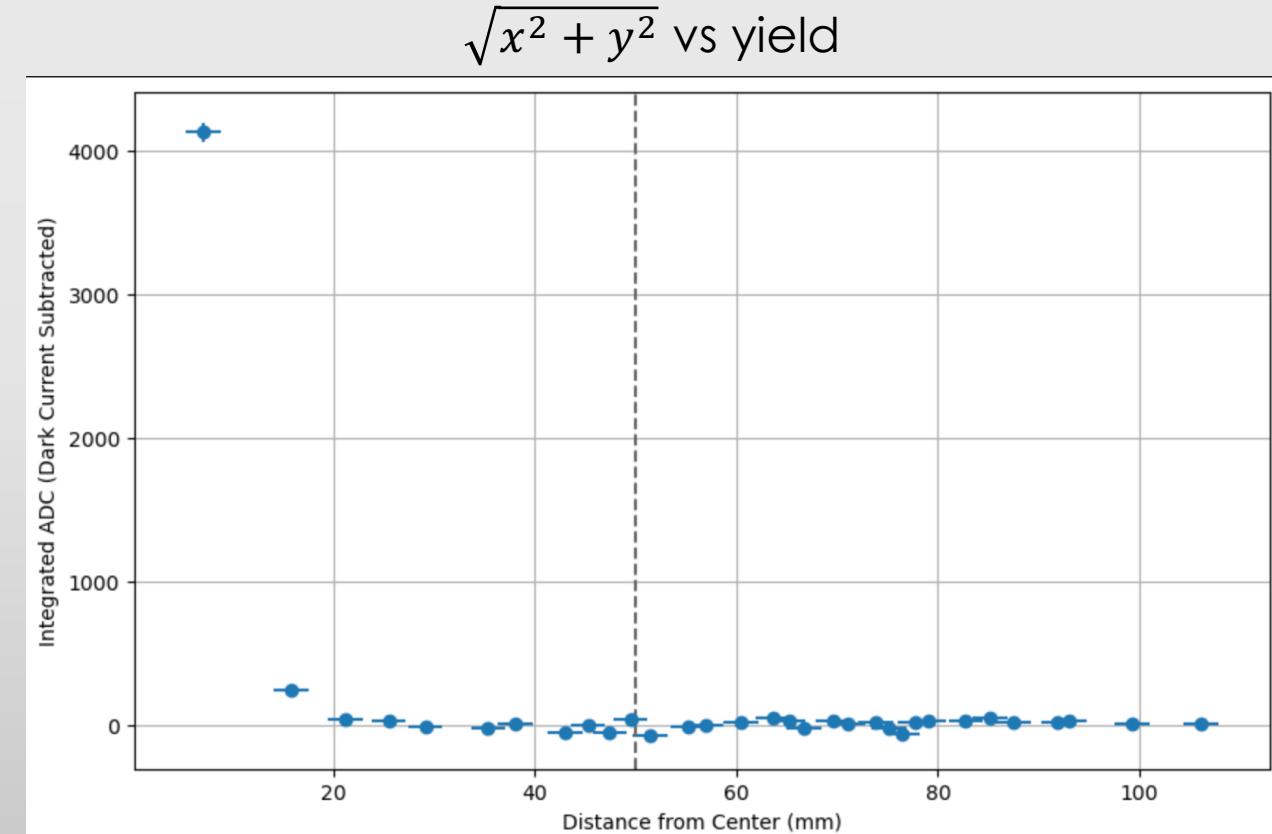
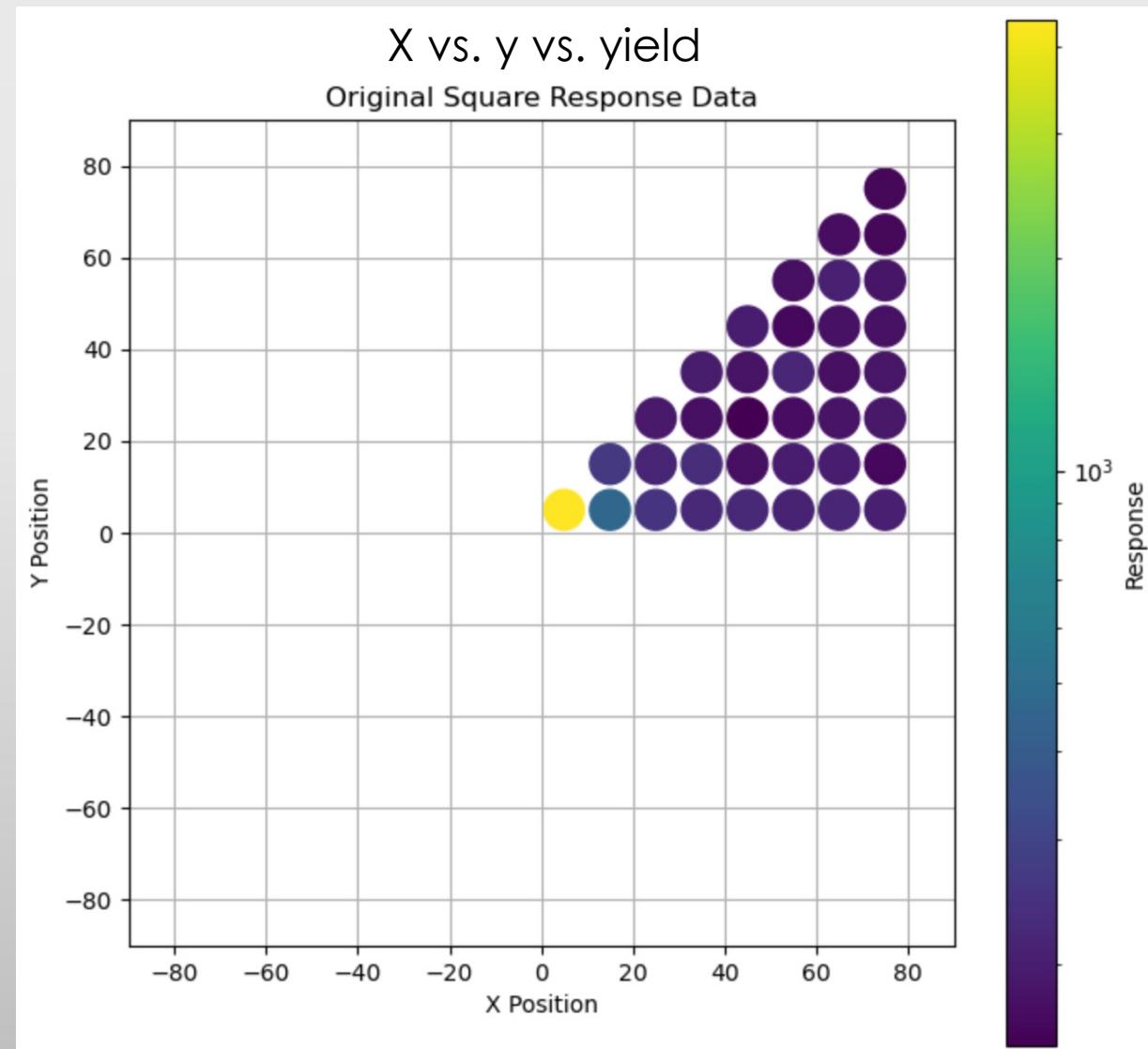
- Horizontal scan across the center of the tile:



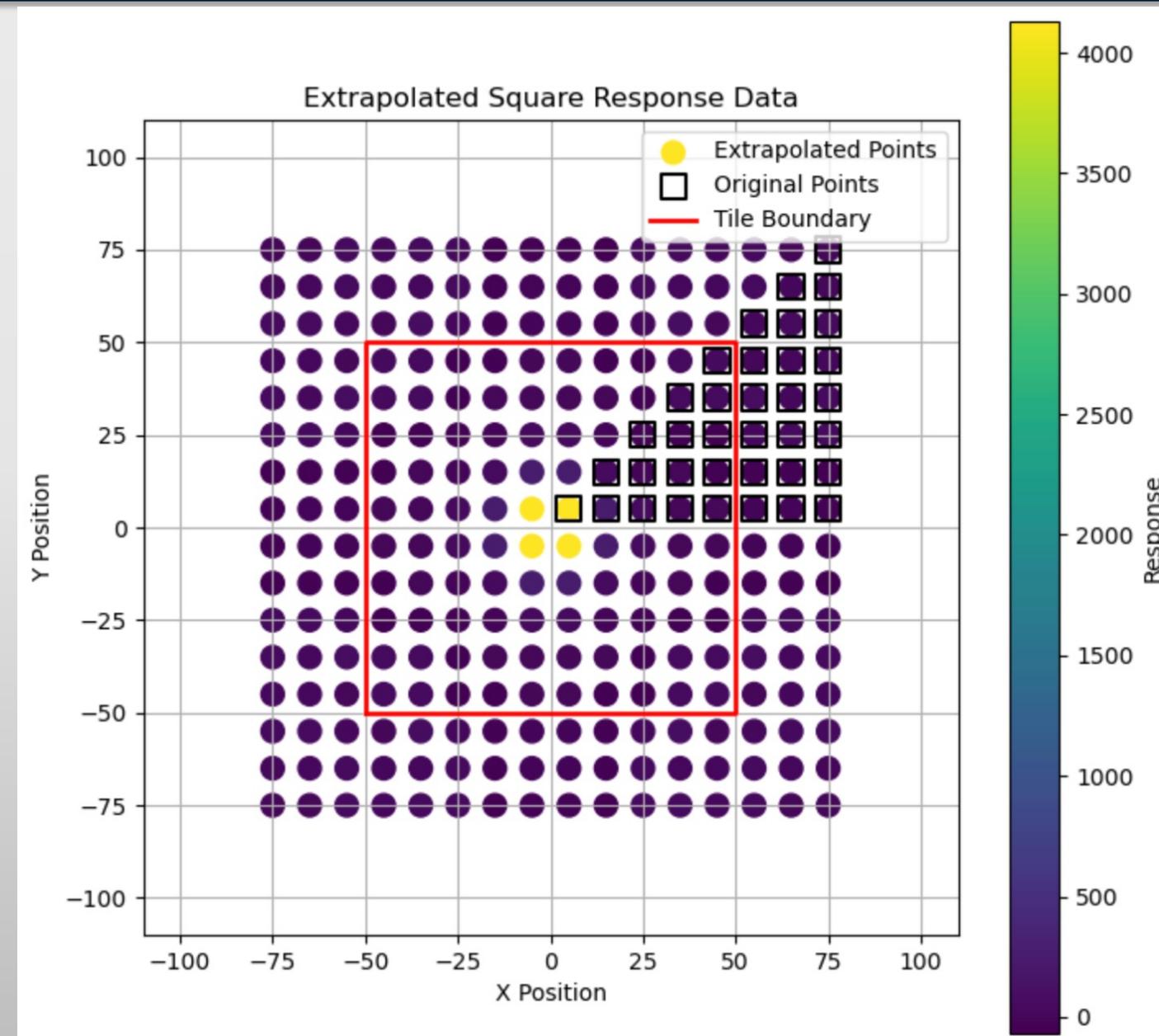
Vertical lines=edge of the tile

Results from unwrapped, polished 10x10 tile

- 1/8th grid scan

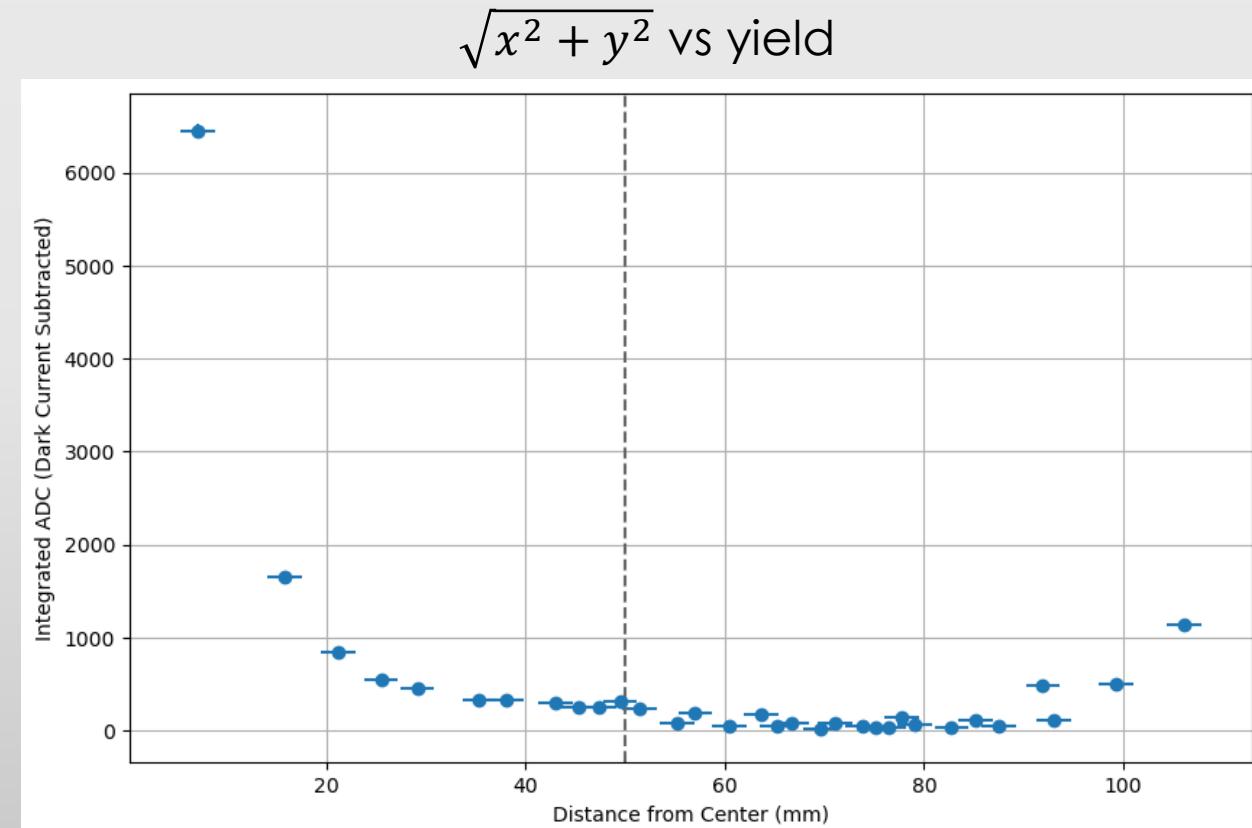
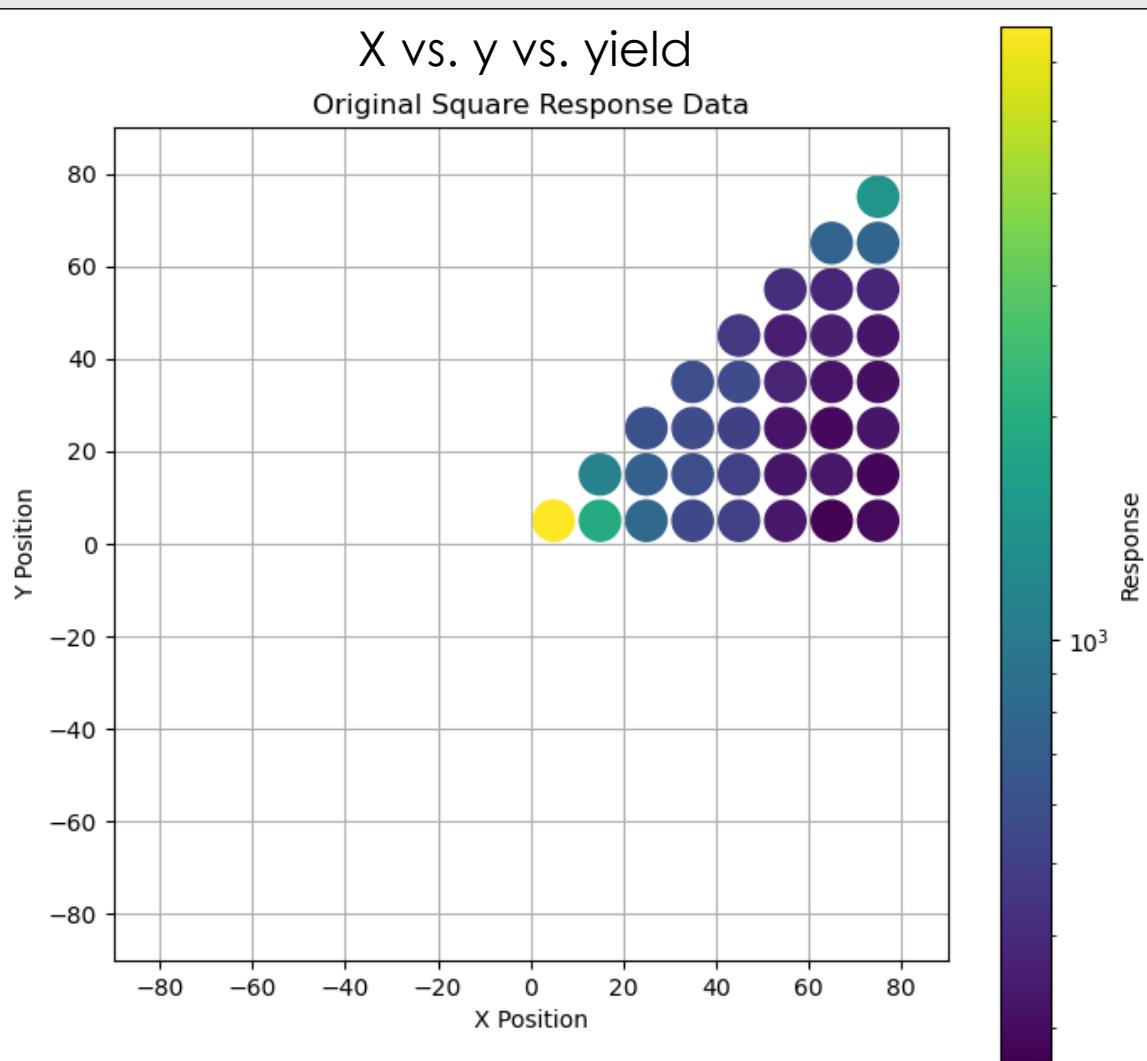


Heatmap from exploiting square symmetry



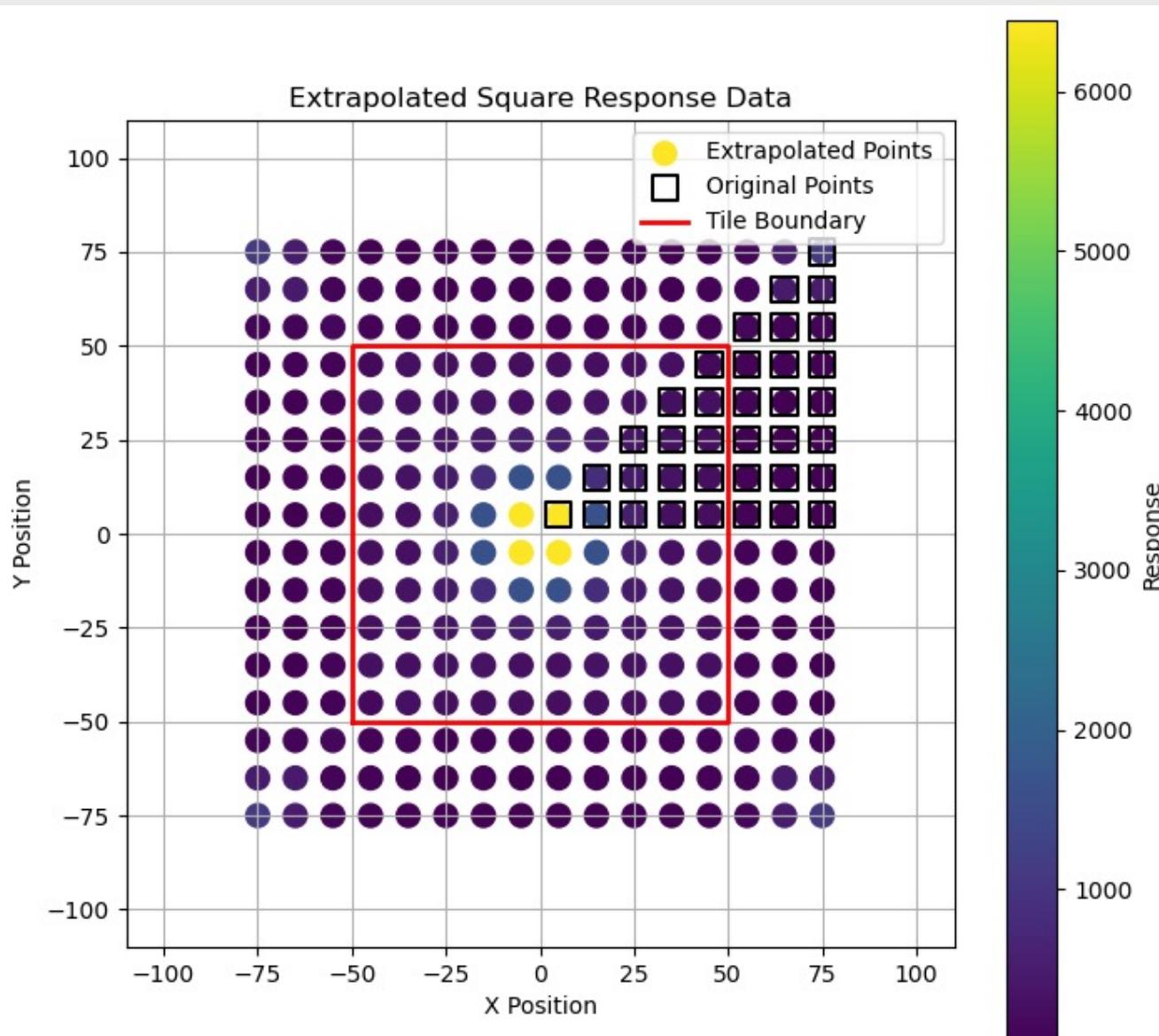
Results from wrapped, polished 10x10 tile

- 1/8th grid scan



Note: ignore these high yield points at 75, 75
I suspect due to my phone flashlight checking if it
was done

Heatmap from exploiting square symmetry



Clear improvement from unwrapped case, but very far from ideal.

Maybe wrapping can be improved (better technique/methodology)

Possible improvement by adding layer of reflective material over the PCB with only a very small hole for the SiPM. Could be that the whole cut into the tile's wrapping is too large.