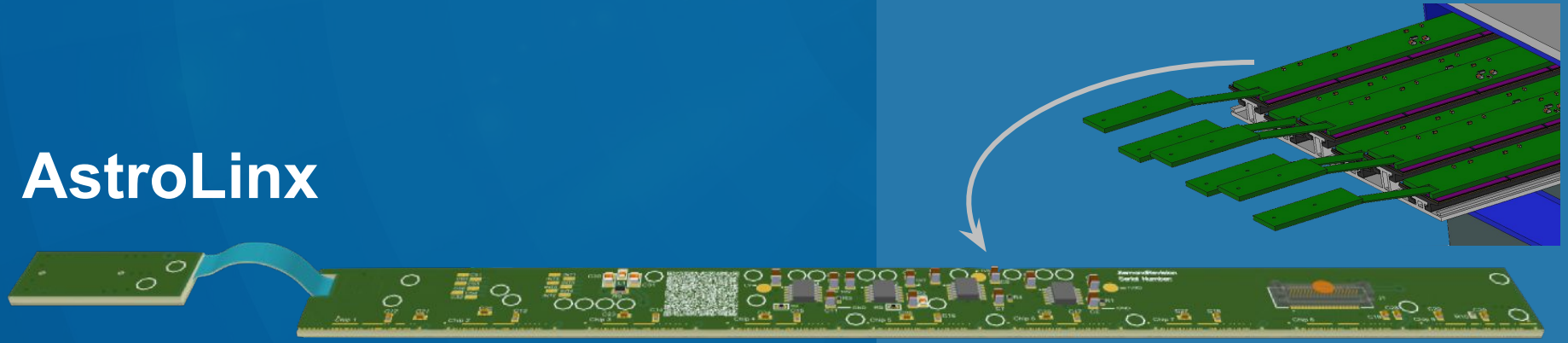
Barrel Imaging Calorimeter Preliminary Design Review

AstroLinx



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BIC PDR
September 17-18, 2025

Outline

- Overview
- Design
- Test articles
- Final design plans
- QA/QC plan
- Safety
- Plans for preproduction, production

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Charge Questions

Charge:

1. Is the progress and design maturity of the barrel electromagnetic calorimeter systems aligned with being baselined in June 2026 (>60% maturity is required)?

2. Are the technical performance requirements appropriately defined and complete for this stage of the project?

3. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?

4. Are the current designs and plans for detector and electronics readout likely to achieve the performance requirements with a low risk of cost increases, schedule delays, and technical problems?

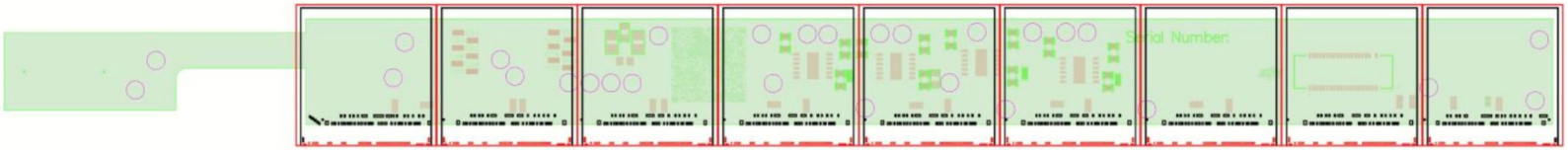
5. Are the calorimeter fabrication and assembly plans consistent with the overall project and detector schedule?

6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?

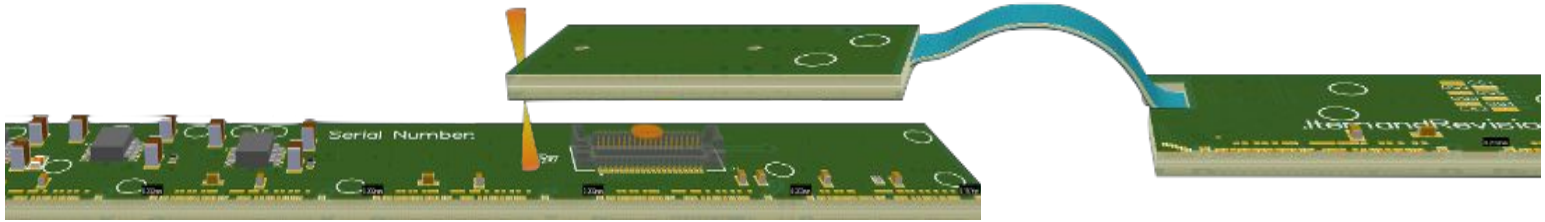
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?

8. Have the recommendations from previous reviews been adequately addressed?

Overview



- Supply power and data transmission to AstroPix chips
- Each AstroLinx supplies 9 AstroPix and adheres atop to form a module
- Wire-bonds connect AstroLinx to AstroPix
- Test article design is a rigid-flex PCB
- Connects 12 modules in daisy-chain to form 1 full stave
  - Each module reads out on the data bus to End of Tray Card Directly
- Connects to the End of Tray card with same connector



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Design - Impedance Structures

- Reduces reflections → lower loss and less noise
- Target: 50 Ohms +/- 2.5Ohms
  - Manufacturing capabilities
  - Useability
  - Dependant on stackup

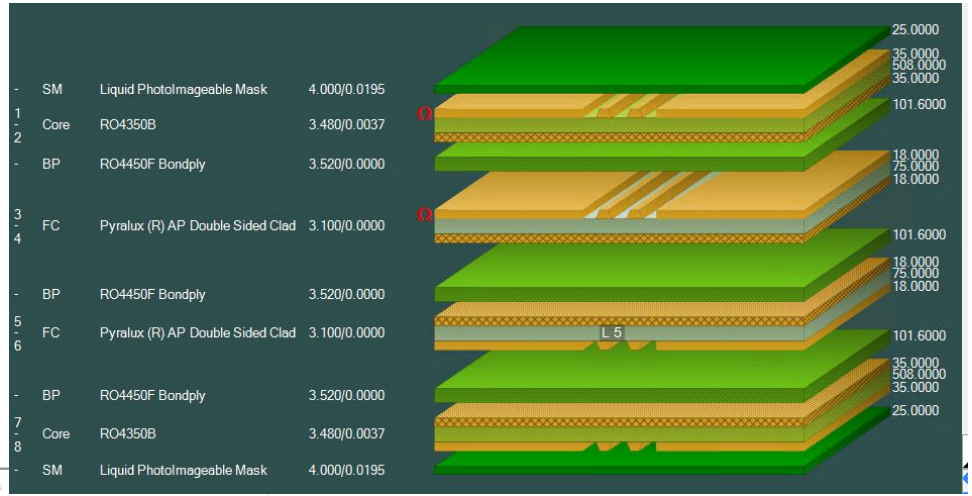
Structure	Layers	Track Width	Gap	Thickness of copper	Impedance (Ohms)
Co-planar Single Ended Stripline	Route 1, 8 GND Ref 2,7	350um	100um	1 oz (35um)	51.07
Co-planar Single Ended Mictrostrip	Route 3 Ref 4	110um	100um	½ oz (17.5um)	49.53
Coplanar Single Ended Stripline (Flex)	Route 3 Ref 4	110um	100um	½ oz (17.5um)	51.07

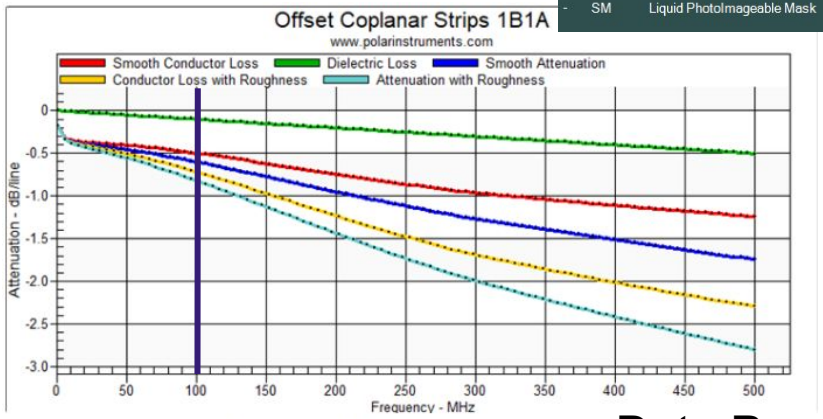
Design - Stack-up

Data signal integrity

- Limit reflections → less noise
- Limit power loss → better transmission lines and less power and signal loss
- Speedstack for stackup
- SI9000 for data simulation
- 3.5 dB loss over total board
  - Within 10 dB target

Physical stack-up





Loss of Layer 3 Routing in upstream region

Data Power Loss Plot

Recommendation: Stave Concept: Simulate power and data transmission along the full chain to the EOS board
Response: This is simulated using the module PCB (AstroLinx) for up to 12 modules.

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Design - Power

LV provides power to the Chips

- Need 3V minimum at the last module for regulators to maintain voltage
- 9V input
  - Allows for input voltage fluctuation
  - Reduces current for same power
    - Multiple power pins to reduce resistance
  - Vastly reduces power drop over each module
- Voltage drop per AstroLinx 5mV – actual LV voltage at last regulator ~8.25V
- Total power consumption per AstroLinx: 0.544mW, per stave: 6.52mW

Supply	Voltage per chip (V)	Current per chip (mA)	Power per Module (mW)	Power per stave (mW)
VDDA	1.8	1.47	23.85	286.2
VSSA	1.2	1.33	14.4	172.8
VDDD	1.8	6.88	110.16	1321.92

Given power consumption for AstroPix

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Design

Charge 4 and 8

Additional Items:

- HV filter
  - Remove noise for a cleaner HV transmission
- Chip select and interrupt chevrons
  - Allows selection of which module in order of stave
  - Data is sent to/from individual configurable module IDs
- Power circuits
  - Low voltage is converted to separate input voltages on AstroLinx
  - Lower power loss
  - Power nets to chips are closer to necessary voltage
- Power stability
  - Each chip layout has a power filter for each voltage level with 100nF capacitor
  - Improves voltage stability and removes any noise in voltage conversion
- SPI Ground
  - The final wirebond layout has a large GND pad to allow for ending the communication buses

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Plans for Test Articles

Charge 1

Fabrication and QC testing - Q2 FY26

- 6 AstroLinx PCBs for AstroPix V3

Additional Test Article fabrication

- Impedance coupon
  - Test item to verify our signal lines have correct structure at all layers
- Peel coupon
  - Verifies board fabrication for adhesion between layers
- Readout adapter board
  - Allows AStep board to communicate with the module for demonstration

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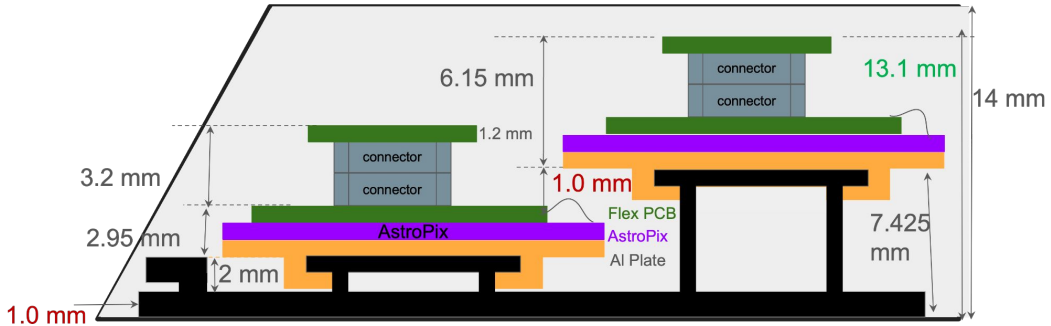
Future Design Changes

Limitations in mechanical envelope

- Current design PCB Thickness ~1.7mm
- Redesign to 1.2mm
- Investigate move to a rigid design with jumper
  - Helps with change in impedance with new stackup
- Value Engineering for production quantities



Sector cross-section

QA/QC Plans

Procedures

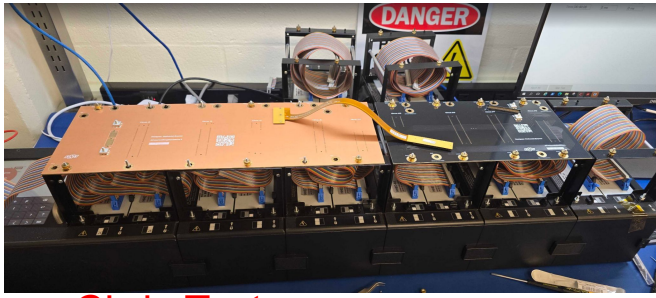
The AstroLinx will be fabricated and assembled by a vendor, so testing is vital. We plan to test every PCB in Preproduction.

QA Procedures:

- Time Domain Reflectometry - Verifies that all traces are uninterrupted

QC Procedures:

- Visual Inspection
- Connectivity and High Voltage with Cirris Tester
  - Outputs connection table and line resistance
- Verify signal loss with Vector Network Analyzer



Cirris Tester (ATLAS QC Stand)

Plan is to optimize QC procedures based on Preproduction experience

ES&H

Charge 7

Safety design considerations:

- HV moved away from board edges
- HV given clearance from other copper to avoid arcing

Points of concern:

- Chemicals while cleaning the PCBs
- High voltage while testing
- Soldering

All items have been planned and accounted in our training and testing procedures. No safety concerns after our QC testing.

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Plans for Preproduction/Production

- Test Articles
  - 30 AstroLinx
  - OSU testing
  - Optimize testing procedures for these articles
- Preproduction (FY26-FY27)
  - 450 AstroLinx
  - Test all
  - Deliver 24 PCBs/week
- Production
  - 41663 AstroLinx (including 87% cumulative yield)
  - Sample rate testing

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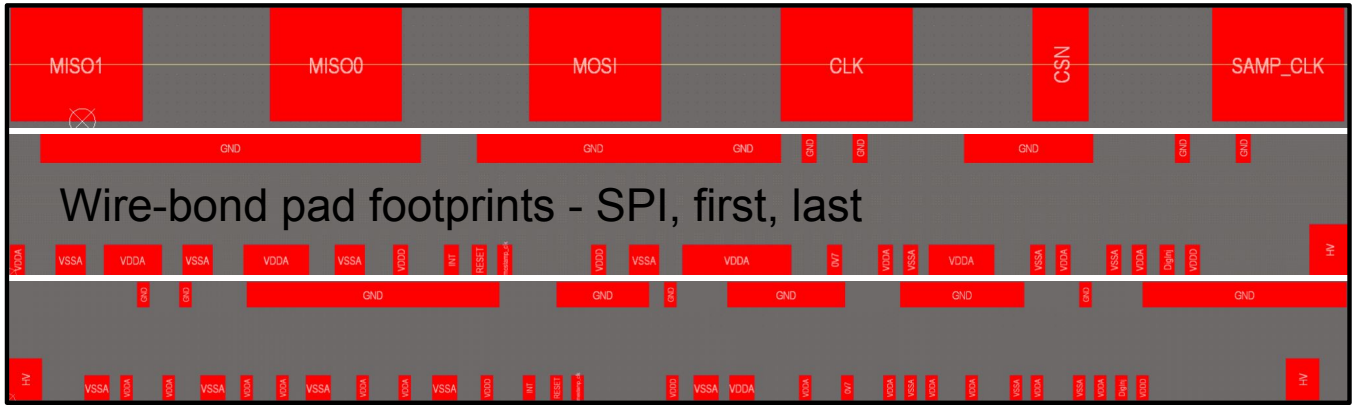
Questions?

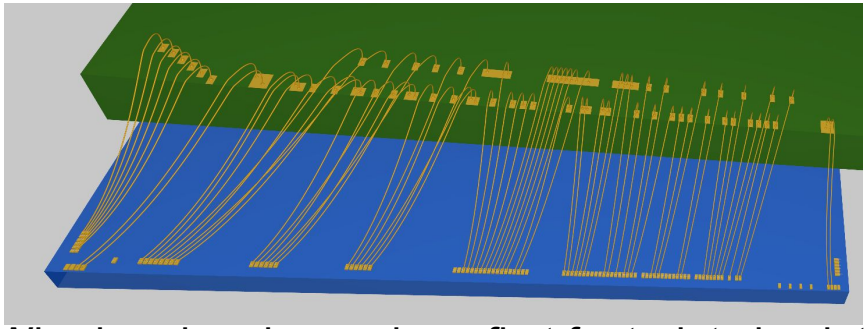
Backup Slides

Design - Interface

Charge 4

Used wire-bond simulation in Altium Designer to verify the wire-bonds can be placed with the pad placement on the AstroLinx. Prevents collision and creepage.





Wire-bond pad mapping - first footprint simulation

Pinout for test articles

Position	Row1	Row2
1	CS1	CS2
2	CS3	CS4
3	CS5	CS6
4	INT1	INT2
5	INT3	INT4
6	INT5	INT6
7	GND	GND
8	Reset	DigInj
9	GND	GND
10	GND	GND
11	GND	GND
12	timestamp_CLK	sample_clk
13	GND	GND
14	MISO1	MISO2
15	GND	GND
16	MOSI	CLK
17	GND	GND
18	GND	LV
19	LV	
20	LV	HV

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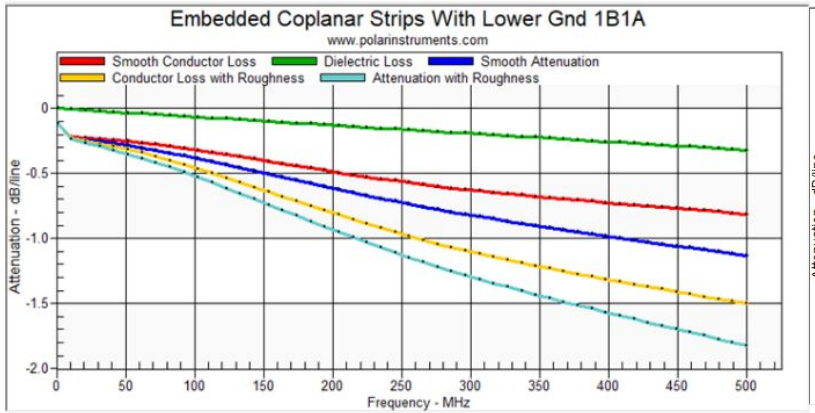
Design - Signal Integrity

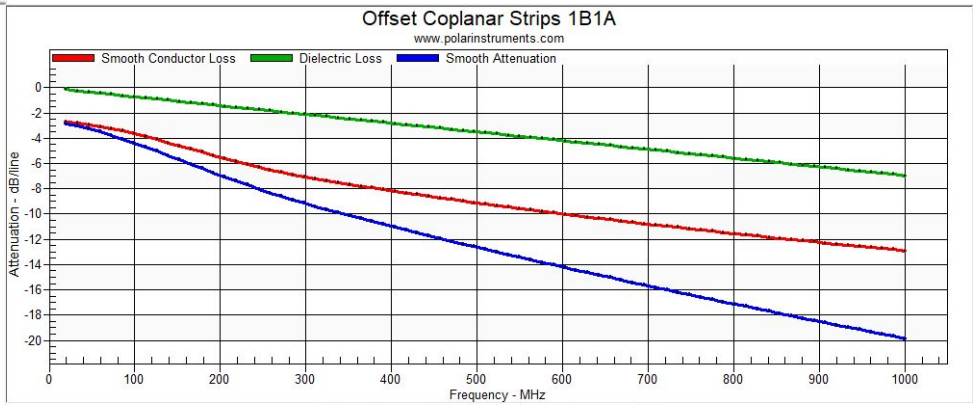
- 3.5 dB loss over full stave
  - Well below -10db standard

Data Power Loss Plot

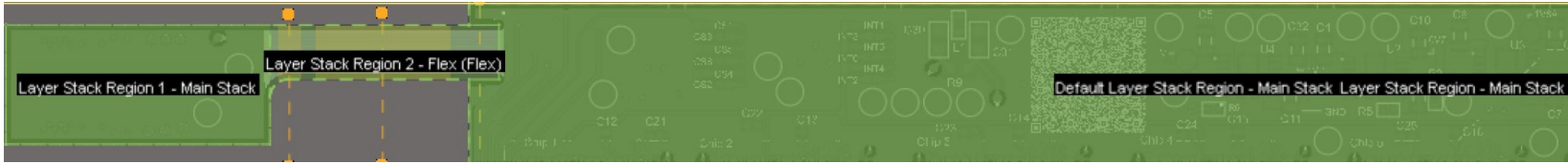


Loss of top Layer of Flex region

Data Power Loss Plot



Loss of Layer 3 Routing in downstream region



Board Region View

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