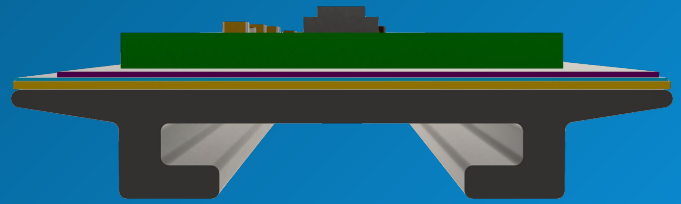
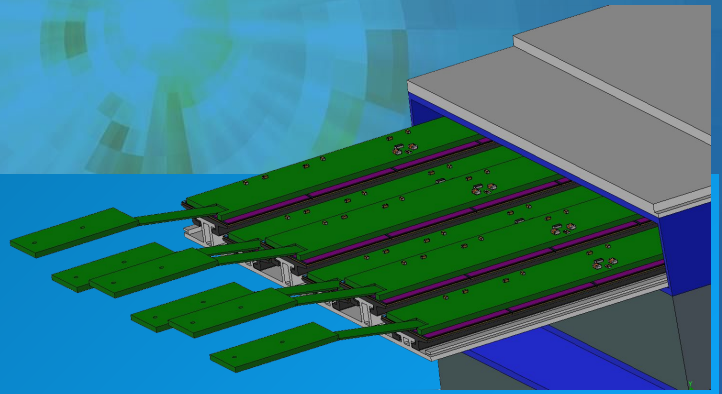
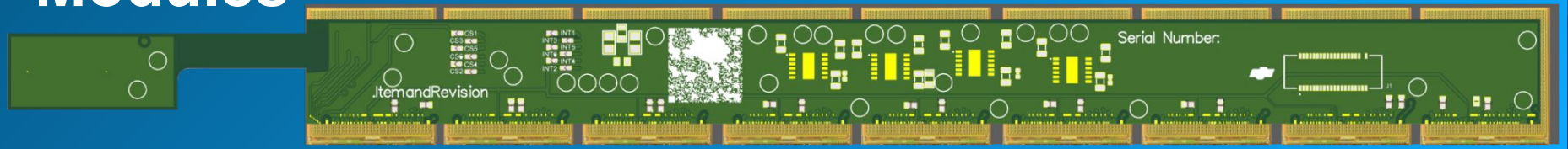
Barrel Imaging Calorimeter Preliminary Design Review





Modules



Manoj Jadhav
Argonne National Laboratory
on behalf of the BIC DSC

BIC PDR
September 17-18, 2025

Charge

1. **Is the progress and design maturity of the barrel electromagnetic calorimeter systems aligned with being baselined in June 2026 (>60% maturity is required)?**
2. **Are the technical performance requirements appropriately defined and complete for this stage of the project?**
3. **Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?**
4. **Are the current designs and plans for detector and electronics readout likely to achieve the performance requirements with a low risk of cost increases, schedule delays, and technical problems?**
5. **Are the calorimeter fabrication and assembly plans consistent with the overall project and detector schedule?**
6. **Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?**
7. **Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?**
8. **Have the recommendations from previous reviews been adequately addressed?**

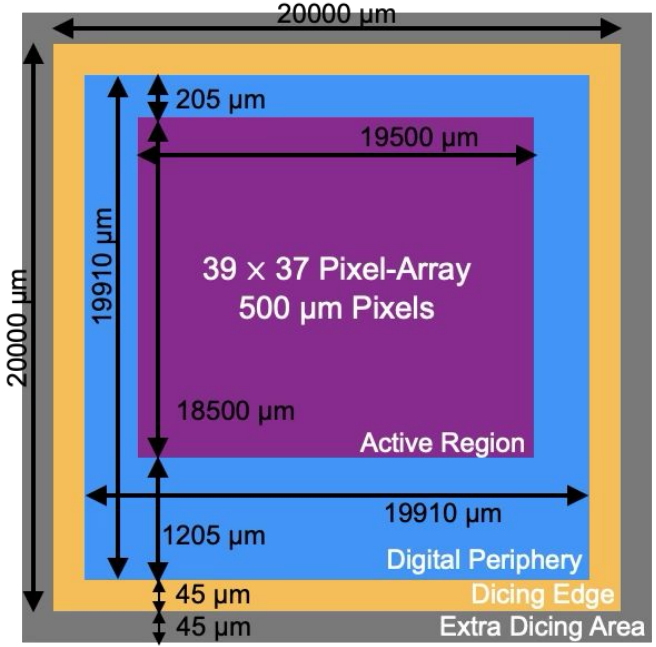
Outline

- Overview of AstroPix and active coverage
- Concept of imaging layers
- Production statistics
- AstroPix Modules and Staves
- Assembly toolings
- Module test articles
- Module QC procedures
- Pre-Production plan
- Production plans
- ES&H
- Summary

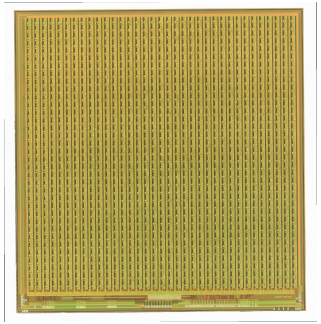
AstroPix

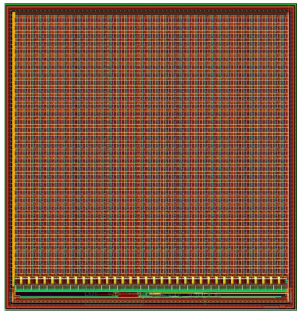
A low-power HV-CMOS monolithic active pixel sensor

- Current AstroPix version: 3 and 5 (1.87 cm × 1.96 cm)
- AstroPix v4 is MWP run with size of 1 cm × 1 cm
- Version 5 is designed and ready for submission (Regina's talk)
- ePIC-BIC Final AstroPix chip size: **2 cm × 2 cm**
- Pixel pitch: 500 µm
- Pixel matrix: 39 × 37
- Sensor thickness: 525 µm
- Pixel to chip edge distance: 250 µm (including dicing area)



AstroPix v3





AstroPix v5

AstroPix Coverage

Minimizing dead area in the imaging layers

- AstroPix chip size = 2 cm × 2 cm
- **Active area = 1.95 cm × 1.85 cm**
- Total Sector length = 435 cm
- Length to cover with single Stave = 217.5 cm
- AstroPix chip + gap = 2.01 cm
- Number of chips required = 217.5/2.01 = 108.21

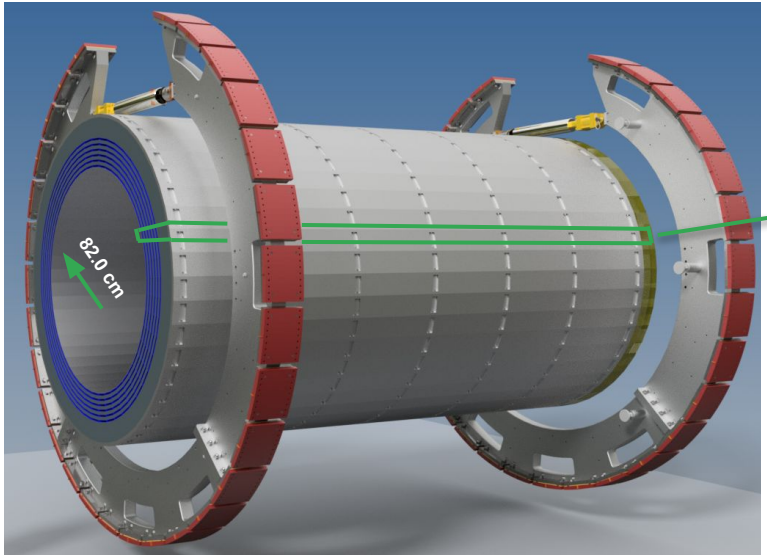
- 12 Module with 9 chips = **108 AstroPix Chips**
- Length of the Module = 9*2.01 = **18.09 cm**
- Length of the Stave = 9*2.01*12 = **217.08 cm**
- Length of Imaging Sector = **434.16 cm**

Inactive area percentage along Stave = **2.99%**

Transverse Coverage of imaging layers

Layer#	Length (mm)	# Staves	Overlap or Inactive (mm)	Overlap/Inactive per Stave (mm)	Overlap/Inactive per Gap (mm)	Inactive (%)
1	107.257	6	4.243	0.707	0.8486	0.47
3	117.411	7	12.589	1.7984	2.0982	0.43
4	122.488	7	7.512	1.073	1.252	0.41
6	132.642	8	15.858	1.982	2.2654	0.38

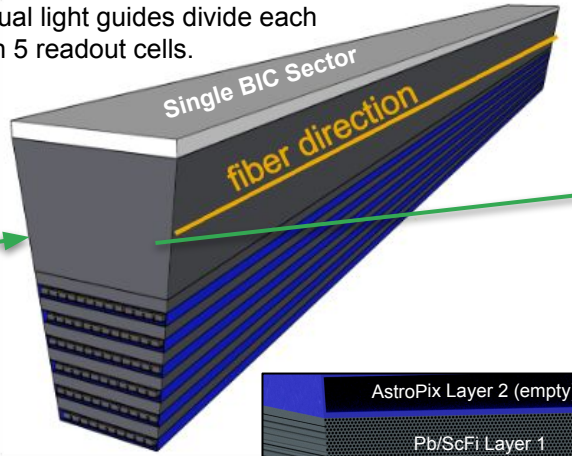
The BIC Design

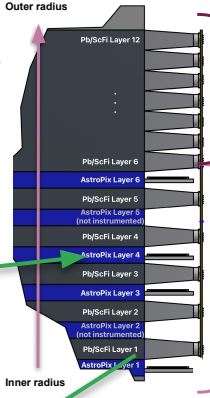


Pb/SciFi Layers - 17 rows of fiber between corrugated lead.

Each sector has 12 Pb/ScFi layers.

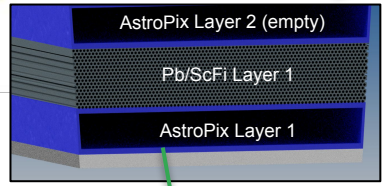
Individual light guides divide each layer in 5 readout cells.





Bulk back section of Pb/ScFi

6 slots for AstroPix sensors, 4 **instrumented** interleaved with **5 Pb/ScFi layers**



4(+2) layers of AstroPix interleaved with **5 Pb/ScFi layers**

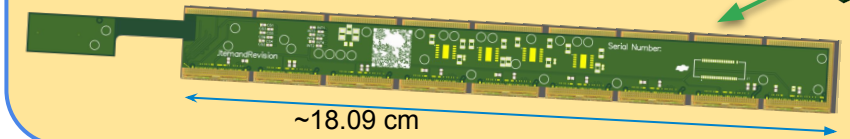
SiPMs - 5 per layer x 12 layers = 60 (Hamamatsu S14161-3050)
1 light guide per cell

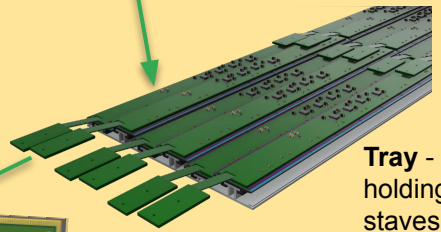
Length: ~435 cm
Inner Radius: ~81.5 cm
Structure: 48 sectors
η Range: -1.71 < η < 1.31
Depth: 17.1X0 at η = 0
Sampling fraction ~10%

AstroPix Module - Nine AstroPix sensors daisy-chained together on Flex PCB.

A stave consists of 12 modules.

A tray contains of 6-8 staves.

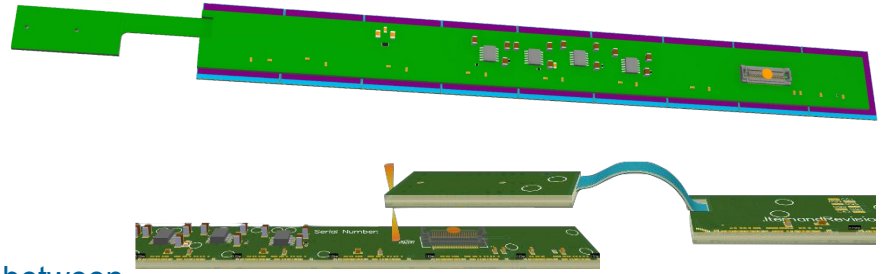


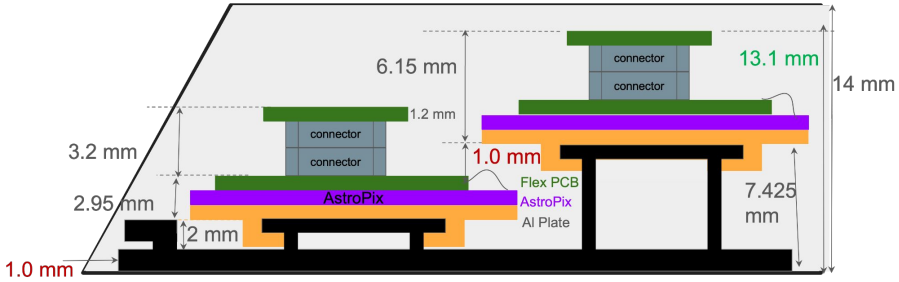


Tray - Structure holding the AstroPix staves for a single layer (217.5 cm long).

The BIC Imaging Layers

- **Module** is an electrically testable elementary unit for imaging layers
  - **9 AstroPix HV-CMOS chips** - 2 cm × 2 cm (Regina's talk)
  - Base Plate (Aluminum) slides on Stave rail
  - Rigid(-flex) PCB readout
- 12 modules forms a **Stave** and readout at the end of Sector using End of Tray Card (FPGA) (~217cm)
- The envelope drawer to fit the Staves is 14 mm in height
- Multiple iteration of designs to fit into the envelope
- Current Module and Tray design allows required overlap between Staves and fits well in the available envelope

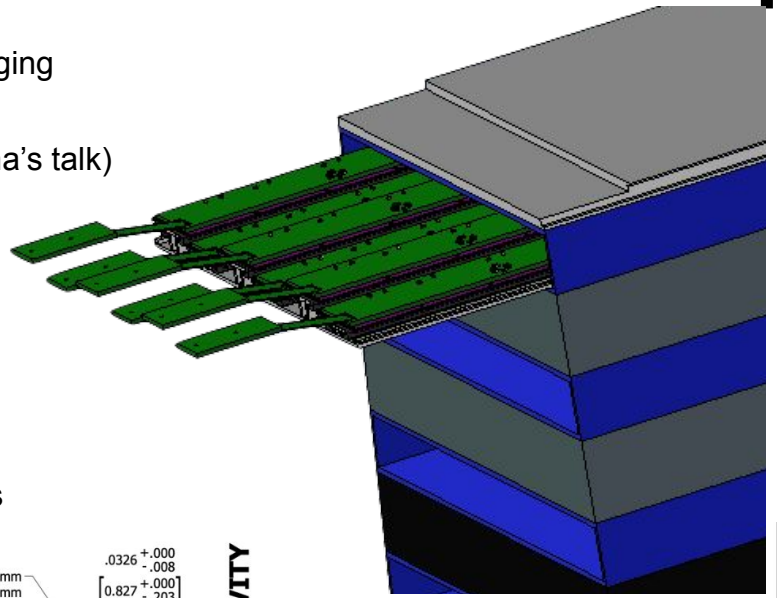


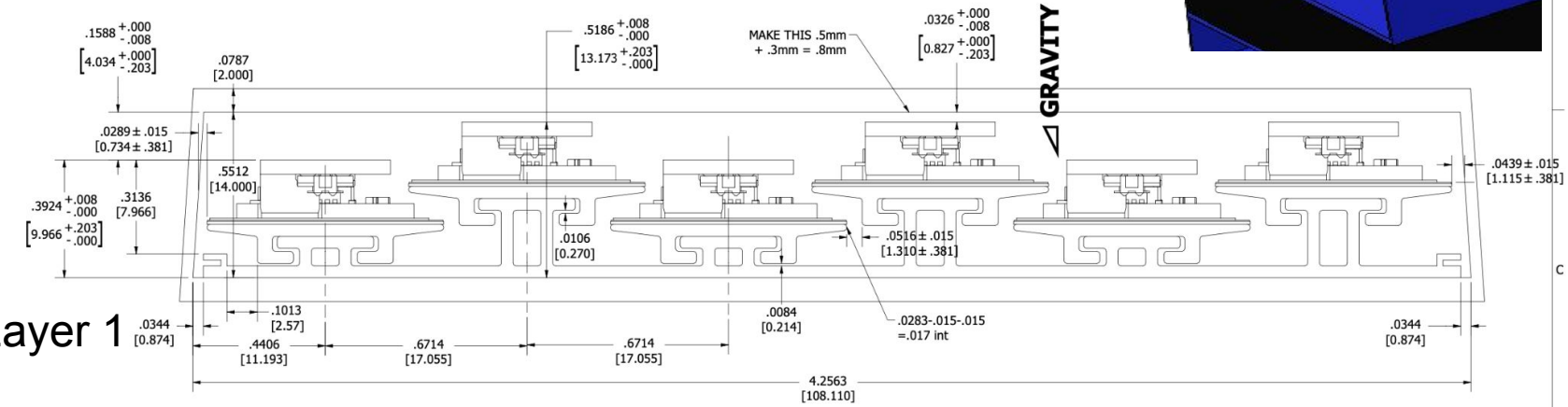


The BIC Imaging Layers

Charge 3

- **Module** is an electrically testable elementary unit for imaging layers
  - **9 AstroPix HV-CMOS chips** - 2 cm × 2 cm (Regina's talk)
  - Base Plate (Aluminum) slides on Stave rail
  - Rigid(-flex) PCB readout
- 12 modules forms a **Stave** and readout at the end of Sector using End of Tray Card (FPGA) (~217cm)
- **Tray** consists of (6, 7, 7, 8) Staves (56 Staves/Sector)
- There are total 48 sectors with length of ~435 cm
- The BIC is made up of 32256 Modules using ~291k chips





Layer 1

Imaging Layers

Production components

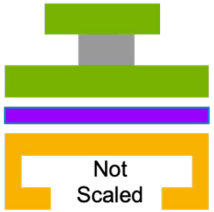
	Total on-detector	Yield at step	Cumulative Yield	Total # parts to produce
sectors	48			
trays	384	99%	99%	**388**
staves	2688	98%	97%	**2771**
modules	32256	95%	92%	**35061**
AstroPix chips	290304	85%	78%	**372185**
wafers				**6203**
end-of-tray cards	384	90%	90%	**427**
tray support rails	384	95%	95%	**405**
module PCBs	32256	90%	75%	**43008**
module base plate	32256	95%	87%	**37076**

AstroPix Module

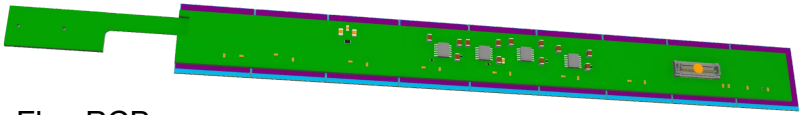
Charge 1

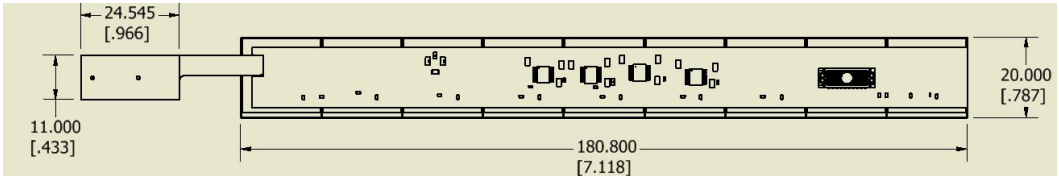
Mechanical design

- AstroPix Module comprises of 3 layers glued together;
  - **Base Plate, AstroPix Chips, and Flex PCB**
- Two adjacent modules will be locked using mechanical structure on base plate (yet to be done)
- AstroPix Chips will be glued to Aluminum plate using **thermally conductive adhesive** with good **electric insulation** (eg. DOW SE4445-CV, Stycast)
- **100 µm gap** between two AstroPix chips
- Flex PCB will be glued on top of chips (eg. Araldite 2011)
- Electrical connection through wire bonds from AstroPix chip to Flex PCB - encapsulated using insulating epoxy/adhesive (eg. Dow Sylgard 186)
- The Aluminum base plate will be slided onto the Stave railing on the Tray



AstroLinx Flex 1.2 mm
Mated Connector 2 mm
AstroLinx 1.2 mm
Glue 0.1 mm
AstroPix 0.525 mm
Glue 0.2 mm
Module Baseplate 1 mm





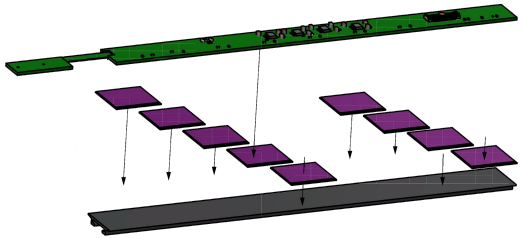
The design dimensions for module is nearly complete and the module stackup fit very well in the available envelope

AstroPix Module

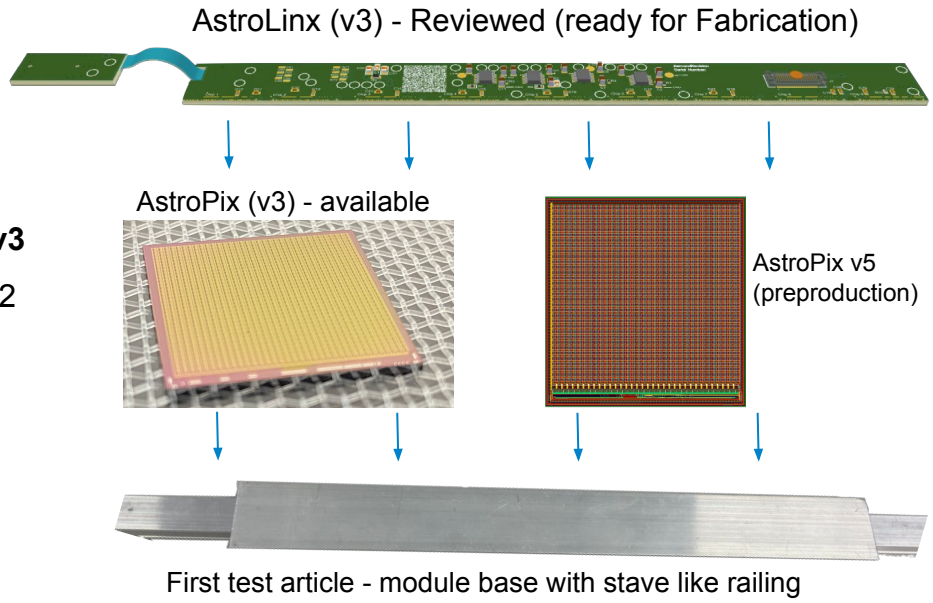
Charge 1, 8

Module design

- AstroPix Module comprises of 3 layers/components glued together
  - **Flex PCB**
  - **9 AstroPix Chips**
  - **Base Plate (Aluminum)**
- **Failsafe design** - easy to rework on Stave
- **Test Articles** - **Building 6 modules using AstroPix v3**
  - Development of AstroLinx readout PCB FY26Q2
  - Development of toolings for alignment
  - Setting up QC procedure by FY26Q3



First module test Article FY26Q2



Recommendation PDR2 2024: Stave Concept: Prepare mock ups of the full stave for data integrity studies
Response: We will be building 6 astropix v3 modules as a half Stave test article, perform QC testing and deliver for system testing - FY26Q3

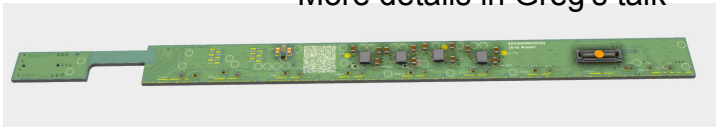
AstroPix Module

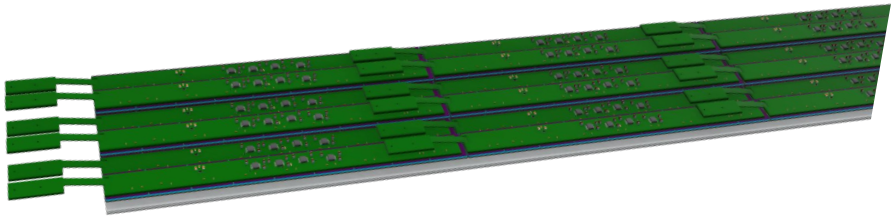
Charge 2

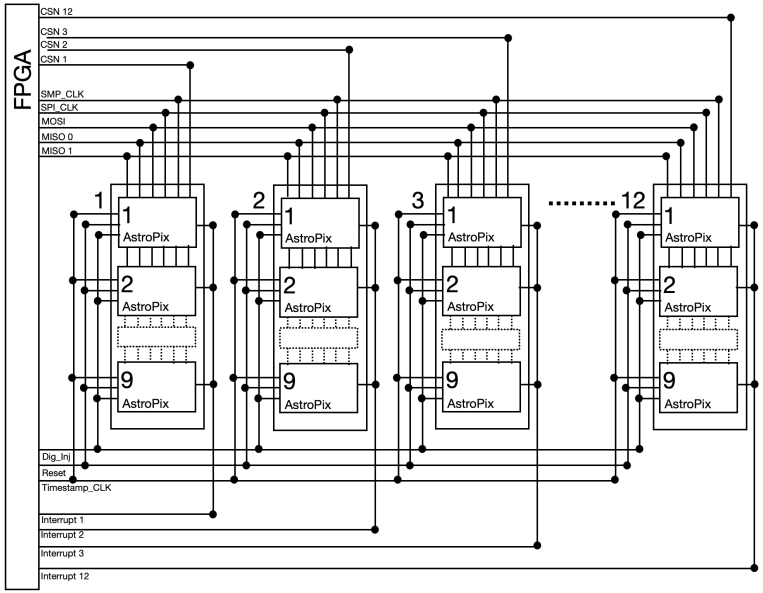
Electrical design of Stave

- 9 AstroPix Chips will be **Daisy-chained on the Module**
- Each Module plugs into its adjacent Module - 12 modules on Stave
- All Modules will be individually **controlled by End-of-Tray Card**
- Voltage Regulators (LDO) to regulate power on each Module
  - Analog and digital power of 1.8V at the Modules
- The broadcast commands/data readout through **SPI protocol**
- 4 **differential data SPI (Clk, MOSI, 2MISO)** common on a stave
- One **single-ended Chip-select SPI and interrupt** per Module
- First test article designed and reviewed (July 21st, 2025)

More details in Greg's talk







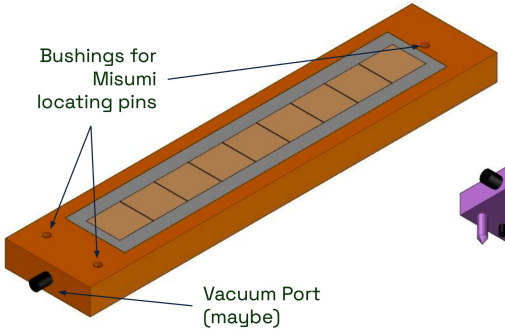
Electrical design of module is finalized with pinouts. 6 Module test articles will be build for Stave testing.

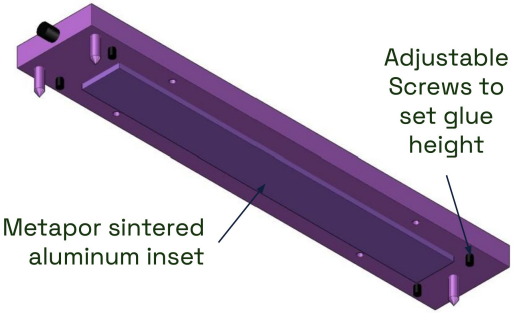
Assembly Toolings

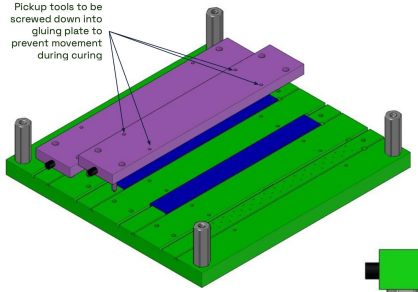
Charge 1, 3

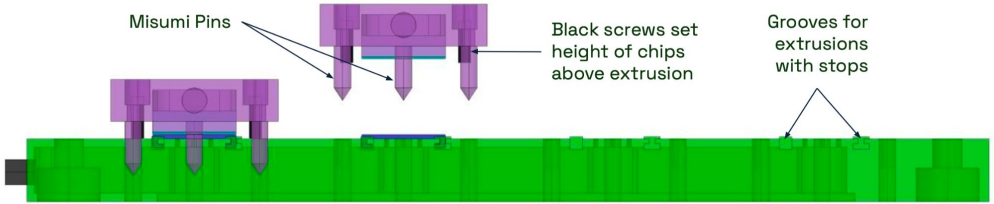
Toolings for assembly

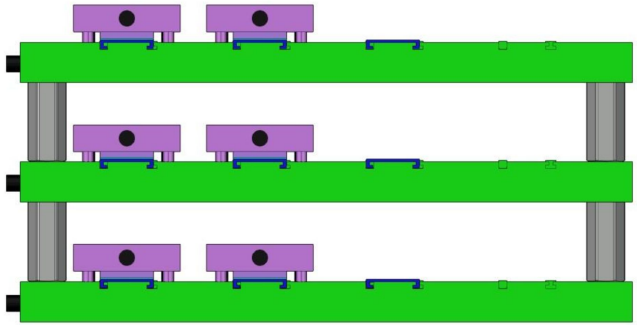
- Align the chips on Al base plate with chip-to-chip gap of 100 um (under optimization)
- Aligns AstroLinx with chips (fiducials on PCB)
- Allow glue amount control and fixes glue height during cure time
- Four modules can be assembled at a time with single tooling set (update to 6 modules in production)
- Multiple parallel sets (6) during Production phase
- Glass dummies are available for mock ups
- Chip dummies with pad layer under fabrication











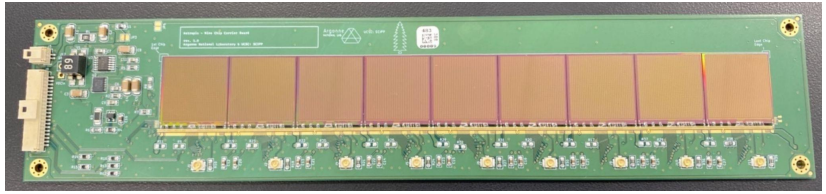
We're working on tooling design and fine-tuning the chip-to-chip gap tolerance for the stencils.

AstroPix Module Test Article

Charge 2,3

Test article 9-chip PCB board

- **Benchmarking** electric design of **AstroPix Module - proof of concept with PCB test article**
  - Mockup the AstroLinx electronics
  - Power distribution stability
  - Testing DAQ development
- Readout board **Daisy-chained 9 AstroPix chips**
  - Readout through SPI as well as Shift Registers (not on Module)
  - 2 LDOs (LT3041, LT3045 - radiation hard)
  - 20 Pin Samtec connector plugs to AStep FPGA board
  - One analog o/p available for each chip
- Testing with AStep card with CMOD FPGA
  - FW/SW available to test
  - Can test up to 3 modules with single card



ASTEP-HW

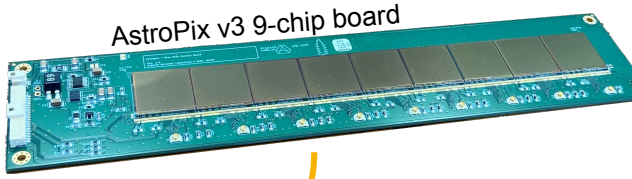
FPGA

PC

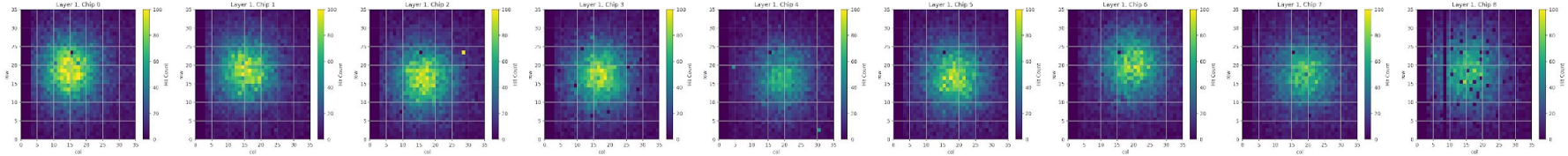
HV Bias board

AStep FPGA board

AstroPix v3 9-chip board



More in Bobae's talk tomorrow

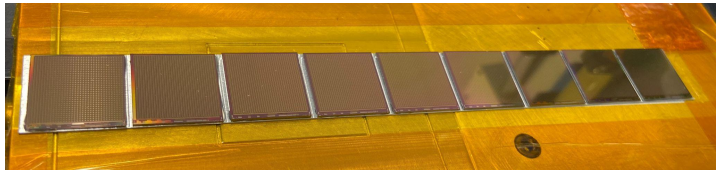


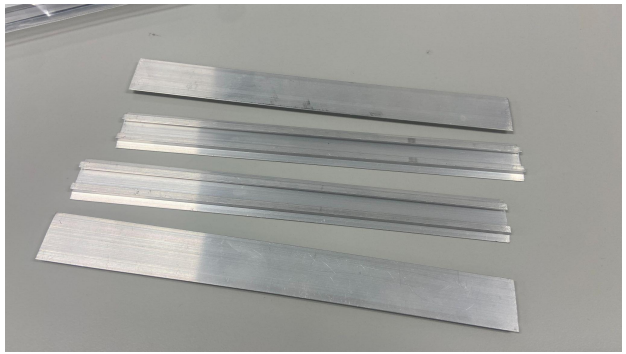
AstroPix Module Test Article

Charge 1

Test Article- Aluminum base plate

- **Benchmarking** Mechanical support for **AstroPix Module**
- 1 mm thick Al plate to slide on the Stave railing
  - Develop assembly procedure
  - first test article for fabrication of base plate
  - locking mechanism still missing (discussion ongoing)
- Trial runs with AstroPix v3 sensors (smaller than final version)
- Glue dispenser robot for glue pattern and controlling glue amount
- Dummy silicon and glass chips will be used
- The dimensions and design are made to work for Production phase
  - 180.9 mm long (fits exactly for 9 chips)
  - no additional dead space
  -



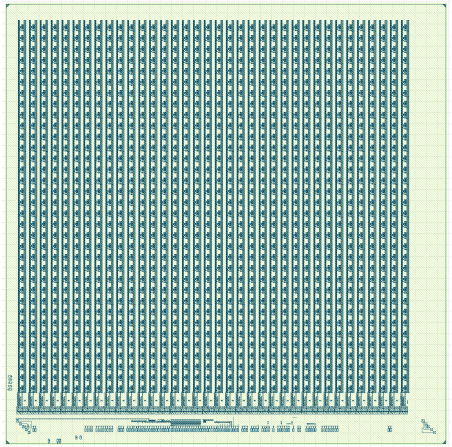


AstroPix Module Test Article

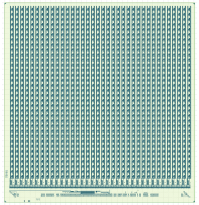
Dummy assembly

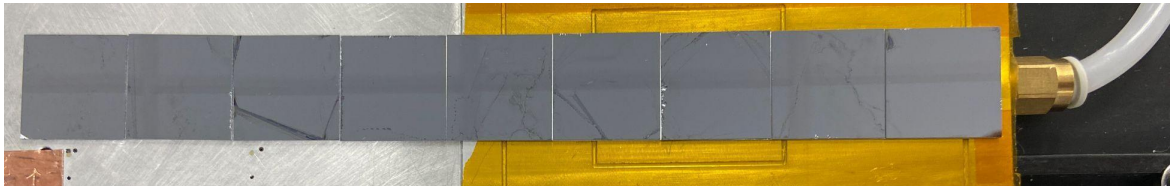
- Module first article base plate received
- Dummy glass chips delivered
- AstroPix design has been updated to final size to create dummy silicon chip with metal layer
    - Fabrication of 10 wafers undergoing
- **First assembly of Dummy chips on Al base plate**
- Study of encapsulations
- Testing toolings tolerances for test article run
- Wire bonding mockup and procedures
- Module assembly mockup and procedures

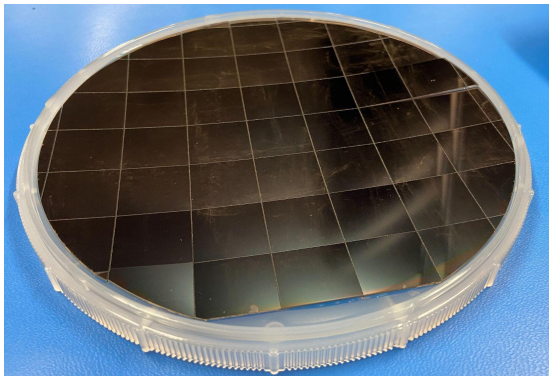
AstroPix v5 scaled to 2 cm x 2 cm footprint



AstroPix v5





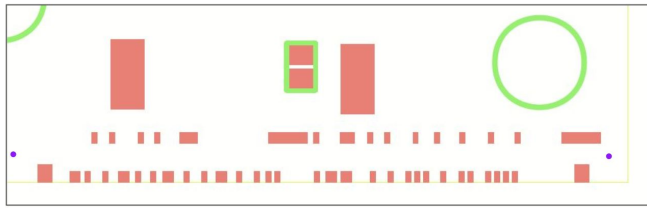


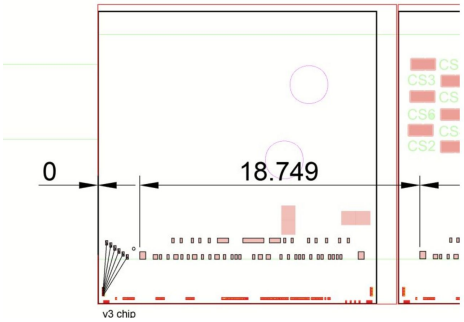
AstroPix Module Test Article

Wirebonding

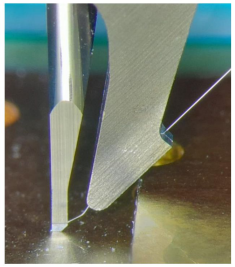
- **Benchmarking** Mechanical support for **AstroPix Module**
- Finalize the wire bonding requirements for test article
  - Tight clearance on vertical SPI pads at first chip
  - Keeping HV line aways from data lines
  - Alignment of pads for all 9 chips

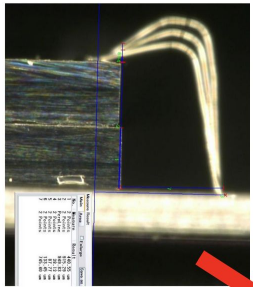
Fiducials for alignments

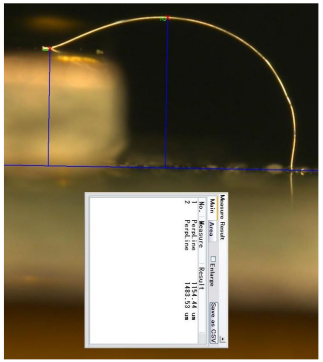


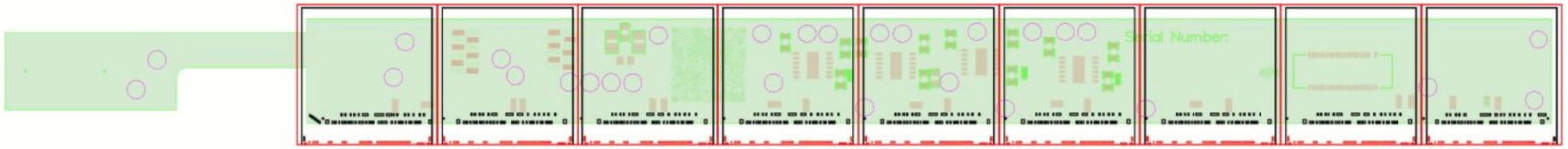


2mm out for 1.1mm height









AstroPix Module QC Procedure

AstroPix Module and Staves

- Initial QC at AstroPix chip level (**chip probing**) - More details in Sanghoon talk
  - IV measurements
  - ASIC functionality testing
- Visual Inspection and Metrology of diced chips
- Visual Inspection and Metrology of base plate and AstroLinx module PCB
- **Module QC**
  - Visual Inspection (physical damages, alignments, etc.)
  - Wire bond pull test - Strength of wire-bonds (batch level)
  - Go/No-go gauge for module tolerances
  - Electrical QC
- **Stave QC**
  - Visual Inspection
  - Electrical QC
- Integration testing **with ETC on Tray**

Preproduction plan

AstroPix Module and Staves preproduction design

Charge 3-5

- **Module Test Article**
  - Test articles (6) using v3 astropix chip will be built and tested FY26Q2
    - Load it on stave railing (half stave), connectivity tests, QC FY26Q3
- **Modules preproduction**
  - Preproduction modules will be built with AstroPix v5
  - Design and develop QC test stand and procedure (v3 and v5) FY26Q2
  - Finalize QC test procedure FY26Q3
  - AstroLinx will be updated for v5 AstroPix (FY26Q4)
  - Start of preproduction assembly FY26Q4
    - 450 modules using v5 chips (~8 modules per sites per week (3 sites))
    - assembly using 2 tooling sets per site (One for glueing chips and one for PCB)
  - Also covers 50 modules using **v6 engineering run AstroPix chips** (FY27Q2)
  - Design update of AstroLinx for AstroPix v6

Preproduction plan

AstroPix Module and Staves preproduction design

Charge 3-5

- **Assembly Tooling**
  - Design toolings for v3 assembly is ongoing (FY25Q4-FY26Q1)
  - Update the version of tooling design for v5 chip (FY26Q2)
    - One set hold 4 modules for assembly
    - two toolings per site
  - Wirebond procedure and protection
- **Stave loading and QC procedures**
  - Final loading on the stave
    - Total 35 Stave will be built (FY27Q3)
  - Finalize QC tasks, Setup a testing systems
  - Develope a FW/SW for QC procedure

Production plan

AstroPix Module and Staves production design

Charge 3

- **AstroPix wafers**
  - Fabrication of AstroPix wafers FY27Q3
  - Total 6203 wafers (60 chips/wafer)
    - 372185 chips to be QC'ed (~75 wafers/week)
    - PNU will take a lead in QC testing AstroPix chips (6 lines of test setup)
    - Argonne will be a backup site (3 lines)
- **Module assembly**
  - Total 35061 module will be built (180/week per site)
  - 3 sites will be building modules and QC testing
    - Argonne 1/3
    - UCSC 1/3
    - PNU ⅓
  - AstroLinx Module PCB
    - Total of 43008 needed, design and QC testing at OSU (QC testing per batch)
- **Stave loading and QC procedures**
  - Total 2672 Stave loading
  - Test box and loading box will be same
  - Assembly sites will be loading modules to Stave/Tray and QC test

ES&H

AstroPix Module and Staves final design

Charge 7

- Safety in place for module assembly and QC
- Each Module talks to ETC directly to avoid replacement of whole stave
- Wirebond potting to safeguard wirebonds
  - safety and reliability of detector
- Temperature and humidity controls
  - protection of module from sparking, corrosion, etc.
- Test setup interlocks (for HV, LV)
  - avoid accidents during testings
- Electrostatic safety - AstroPix chip and assembled modules
- Radioactive source dosimeters and training
- Ergonomic evaluations
- Some of the other hazards
  - Chillers, cold plates hazards
  - Mechanical handling (pinch hazards) toolings, probing, etc
  - Chemical hazards (glue)
- Work control and planning documentation for all assembly sites (in pre-brief)
- Work will be done in cleanroom environment (ISO 7)

Summary

Modules and Staves

- **Mechanical Design**
  - **Mechanical final design is done for Modules**
  - Initial test article fabrication is done and first trial performed
  - Yet to decide for locking mechanism
- **AstroPix Chip**
  - **Final design is v5 completed** and about to be fabricated
  - Next run will have the **final chip size v6, 2 cm × 2 cm in FY26Q04**
  - Production of dummy silicon chips for assembly procedure (glass and Silicon)
- **Electrical Design and Flex PCB**
  - First AstroLinx for AstroPix v3 is design and reviewed
  - Tested first test article with 9-chip PCB board
  - Still need to thin down the AstroLinx to fit in the given envelope (current 1.76 mm, target 1.2 mm)
  - Final Design v5 AstroLinx in **FY26Q03**
- **Mechanical loading procedure**
  - Design work on assembly tooling for preproduction phase - FY26Q01
  - Ongoing discussion on adhesive selection and glueing procedure
  - Wirebond potting needed to be addressed

Thank you!

AstroPix/Wafers and Modules/Staves Institutes

AstroPix chips and Wafers: Chip Design, Fabrication, chip QC

Modules/Staves: Module assembly, Stave loading/QC

Modules/Staves: AstroLinx rigid-flex pcb design, fabrication, and QC