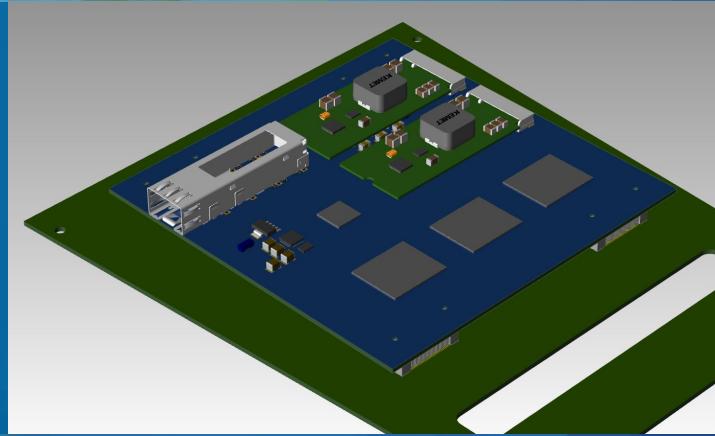


# Readout DAQ

**Norbert Novitzky**  
Oak Ridge National Lab  
on behalf of the BIC DSC



**BIC PDR**  
September 17-18, 2025

# Charge



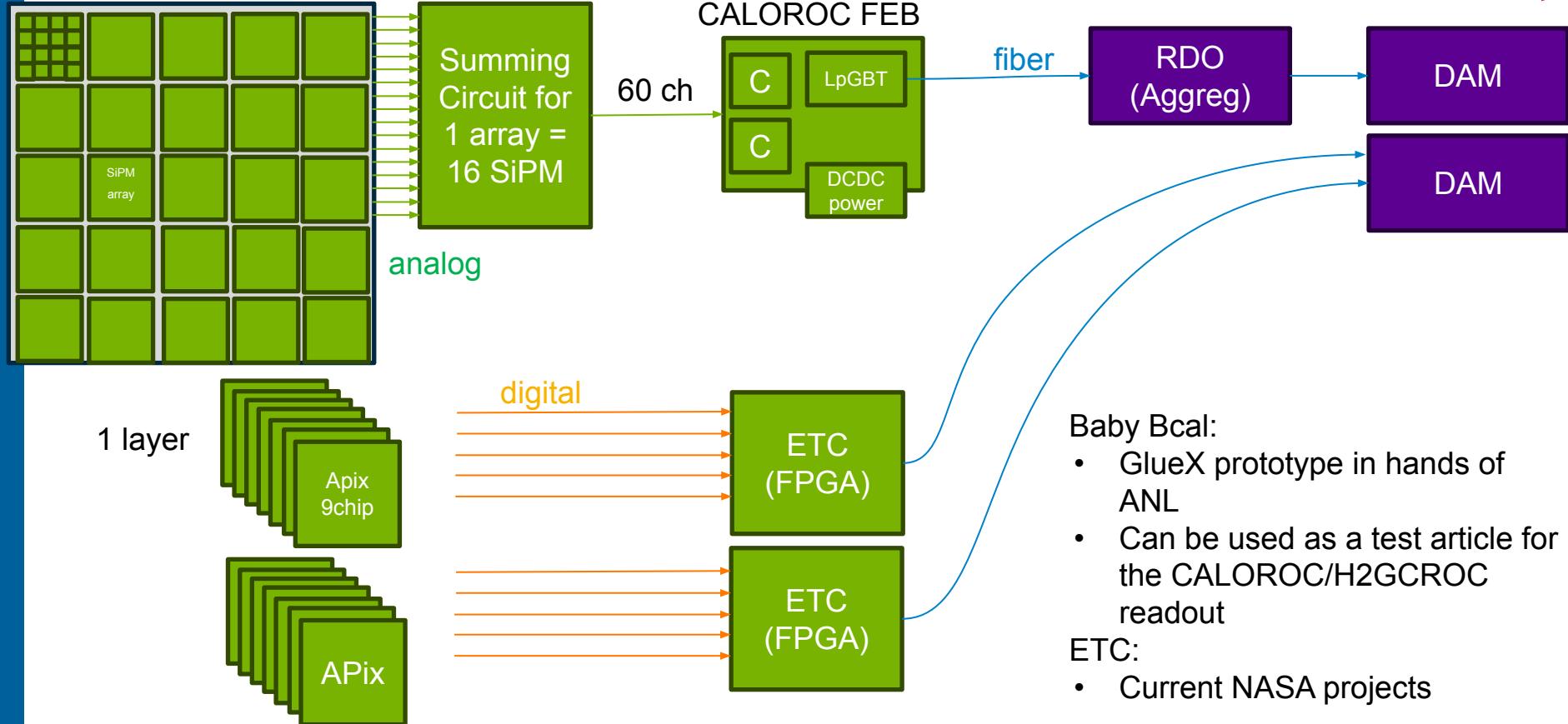
1. Is the progress and design maturity of the barrel electromagnetic calorimeter systems aligned with being baselined in June 2026 (>60% maturity is required)?
2. Are the technical performance requirements appropriately defined and complete for this stage of the project?
3. Are the plans for achieving detector performance and construction sufficiently developed and documented for the present phase of the project?
4. Are the current designs and plans for detector and electronics readout likely to achieve the performance requirements with a low risk of cost increases, schedule delays, and technical problems?
5. Are the calorimeter fabrication and assembly plans consistent with the overall project and detector schedule?
6. Are the plans for detector integration in the EIC detector appropriately developed for the present phase of the project?
7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?
8. Have the recommendations from previous reviews been adequately addressed?

# Outline



- Overview
- Design
- Test articles
- Final design plans
- QA/QC plan
- Safety
- Plans for preproduction, production

# Readout chain - Overview



# Atropix ETC iteration



## A-STEP:

- An Astropix-v3 device for NASA
- Has to be very compact and very small heat generation for payload requirements

## ComPair-2:

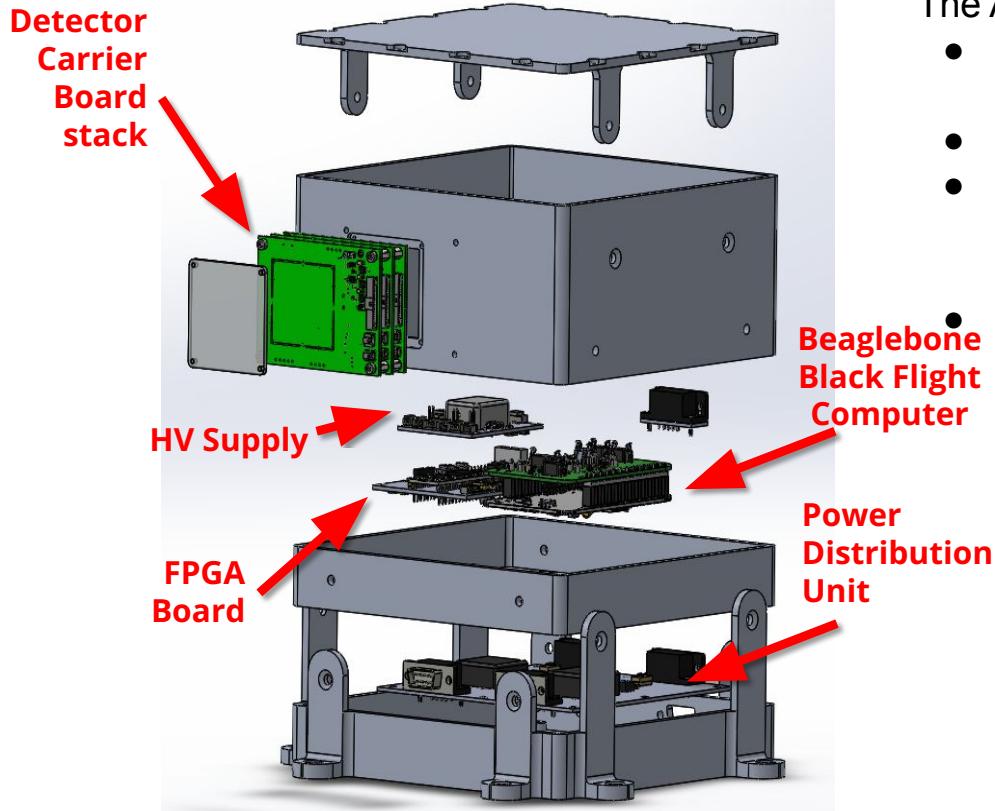
- Using also Astropix-v3, upgrade from double sided silicon sensors from ComPair-1
- Large area sensor
- Readout with similar FPGA module

## BIC:

- Same team of people working @ NASA (all the experience from previous project)
- First step to readout a module
- Construct a stave of Astropix and adopt the firmware

# Sounding rocket gamma-ray telescope

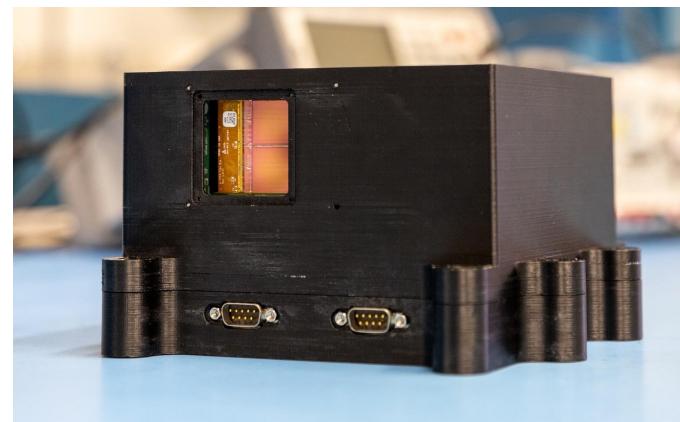
## A-STEP: 3 layer stack of 4 AstroPix chips



The A-STEP payload:

- Digilent CMOD-A7 board with a Xilinx Artix 7 35T FPGA
- On-board DAC for controlling HV supply
- On-board buffering + 8-channel ADC for detector and subsystem voltage, current, and temperature status housekeeping.

DIP pins used for both power and SPI interface with data recorder/transmitter on flight computer

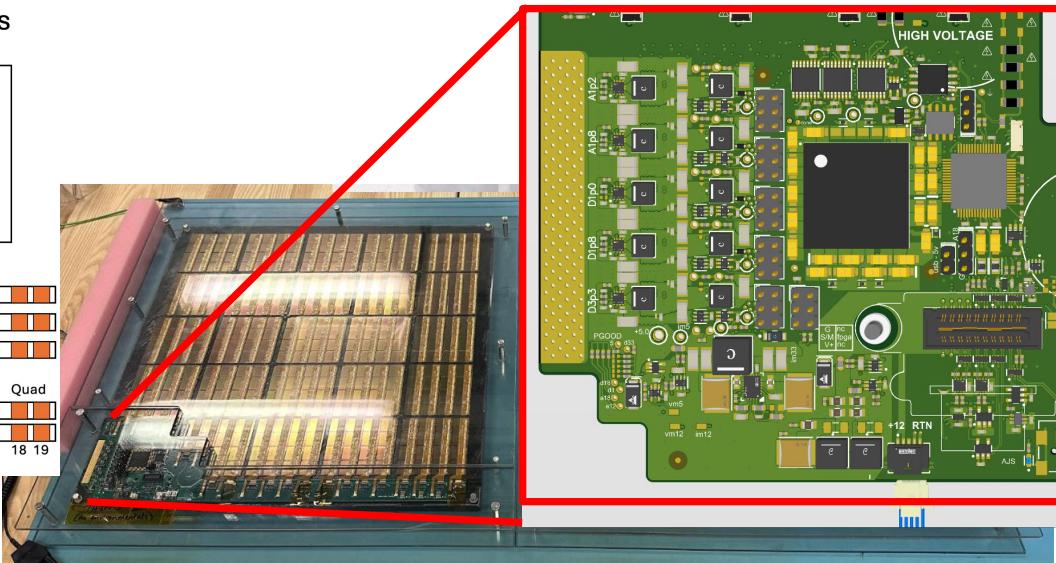
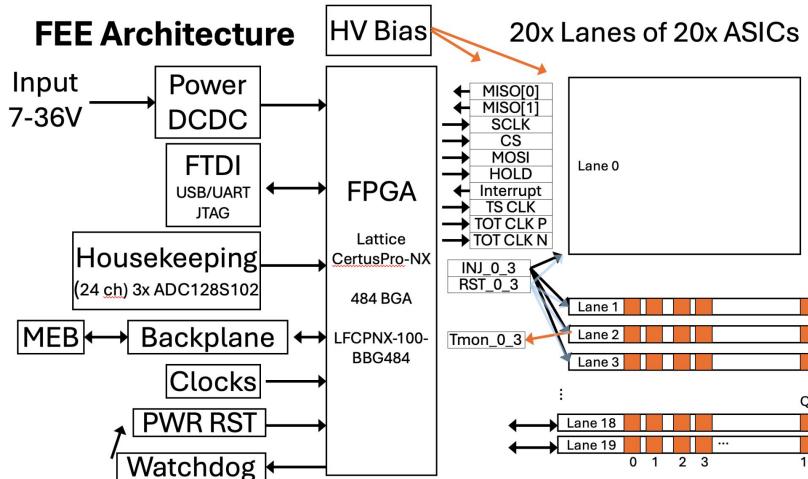


# Balloon-borne gamma-ray telescope

## ComPair-2: 380 AstroPix chip readout per layer



The first version ComPair-2 Front End Electronics (FEE) has been designed, fabricated, currently being tested



# Balloon-borne gamma-ray telescope

## ComPair-2: 380 AstroPix chip readout per layer

- Strong heritage for ETC
  - 108 chips/stave
  - ComPair-2 will provide a baseline design for the ETC on BIC
- Mechanical validation (July 2025)
  - Thermal/Vacuum + Vibration testing
- Early stages of electronics validation
- Collected design changes for v2 of the ComPair-2 layer and will implement them in the next iteration



# Astropix ETC iteration



## A-STEP (done):

- An Astropix-v3 device for NASA
- Has to be very compact and very small heat generation for payload requirements

## ComPair-2 (done):

- Using also Astropix-v3, upgrade from double sided silicon sensors from ComPair-1
- Large area sensor
- Readout with similar FPGA module

## BIC (in-progress):

- Same team of people working @ NASA (all the experience from previous project)
- First step to readout a module
- Construct a stave of Astropix and adopt the firmware

**Recommendation:** Define clear schedule until test article and test early with real AstroPix modules

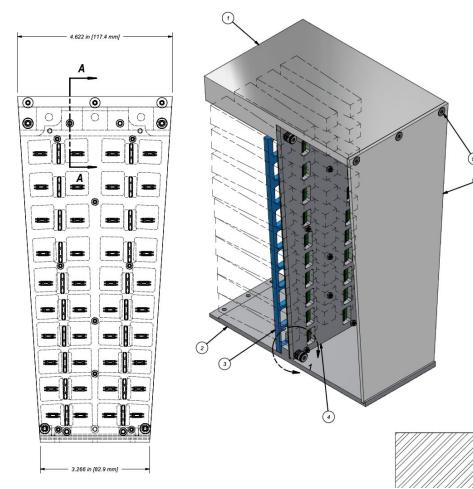
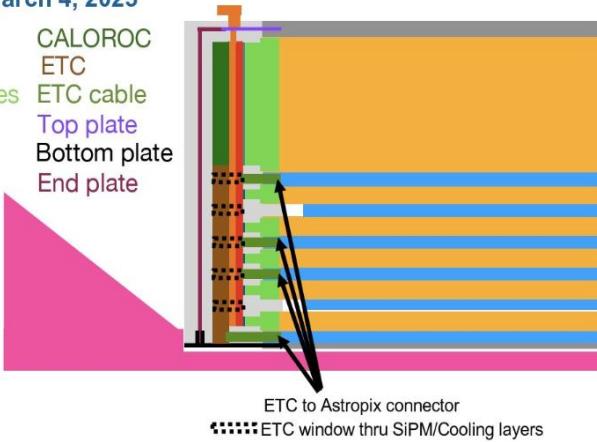
**Response:** Funding is available ~now for ETC and the test article will be available in summer 2026; In the mean-time we use A-STEP fpga for 9-chip pcb testing

# Overview of the Sci/Fi readout

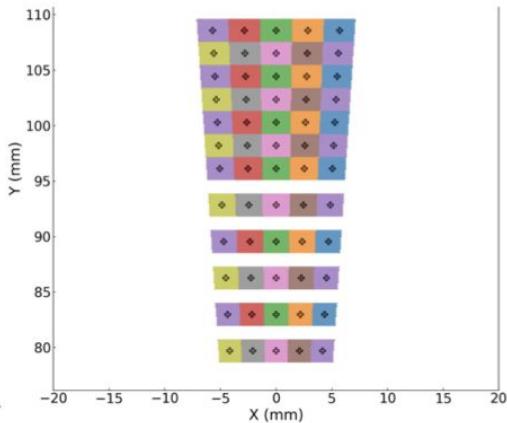
Sylvester & Zisis, March 4, 2025

Legend:

PbScFi	CALOROC
Astropix	ETC
Light Guides	ETC cable
Cookies	Top plate
SiPMs	Bottom plate
Cooling	End plate



For  
Baby  
BCAL



The Sci/Fi layers are ending in a lightguide with a SiPM 4x4 array at the end. In one sector there are:

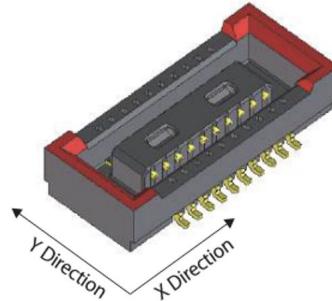
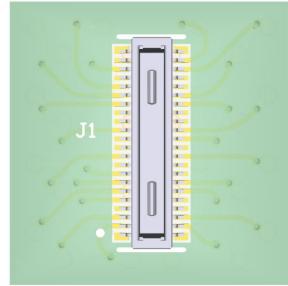
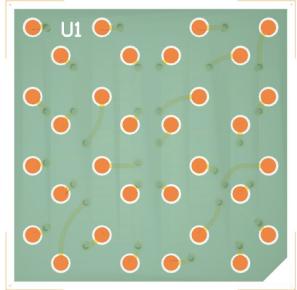
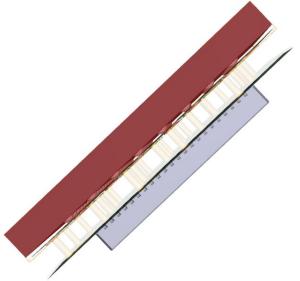
- 12 layers of SciFi
- 5 columns

In total  $60 \times (4 \times 4 \text{ } 3 \times 3 \text{mm}^2 \text{ array})$

- Signals from individual SiPM's are summed up to one channel

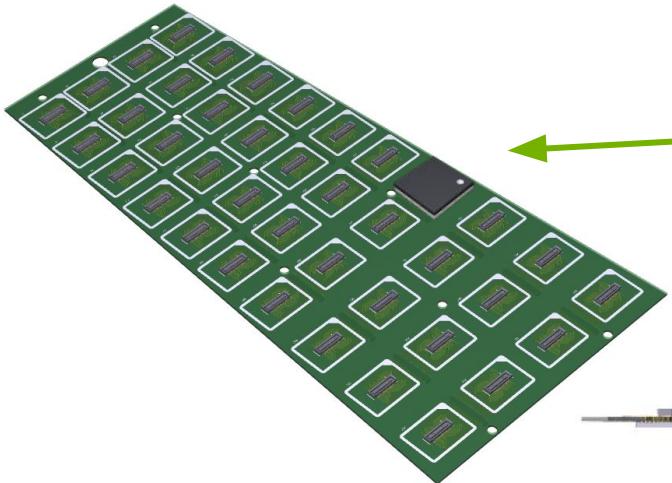
Design for Baby BCAL now, BIC design will follow

# SiPM Boards



SiPM array will be on small removable board

SiPM mini-boards with connectors;  
Modularity for re-purposing and ease of maintenance



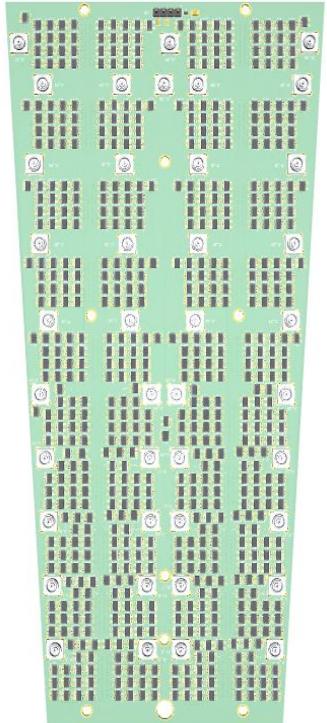
SiPM window PCB for Baby BCAL interface to 16:1  
multiplexing/summing board for “conventional” or CALROC  
readout

Compact design; thickness ~7mm with SiPMs attached

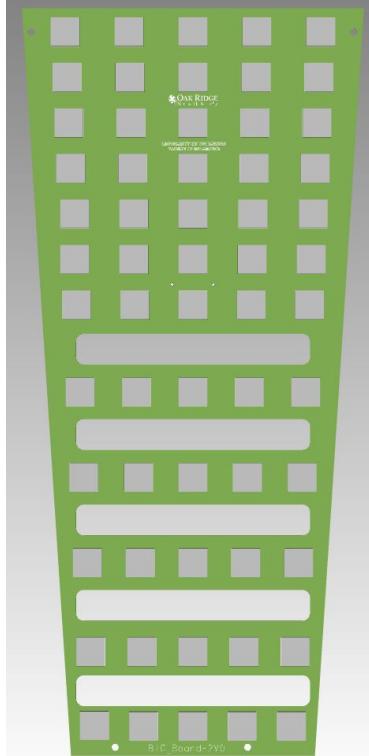
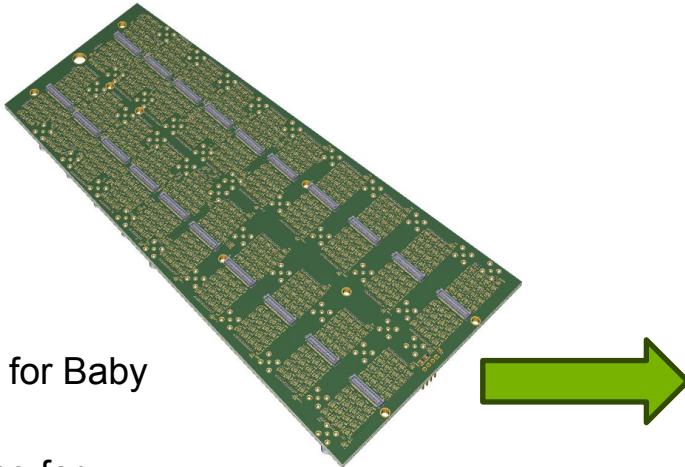
# Summing stage

SiPM summing board for Baby BCAL

- Validate the summing scheme for the final design



SiPM amplifier PCB for Baby BCAL with 16:1 multiplexing/summing for “conventional” readout



Sample signals from 16:1 multiplexing of a S14161-3050HS-04 4x4 array with a LYSO scintillator

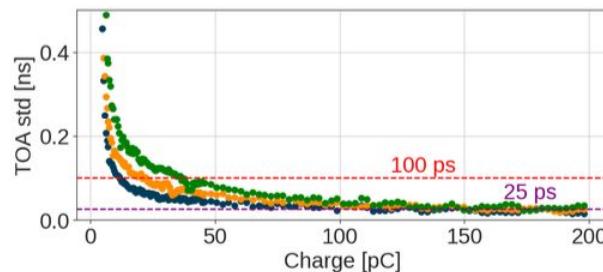
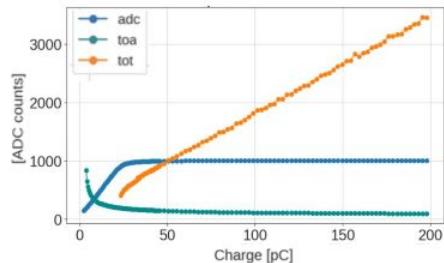
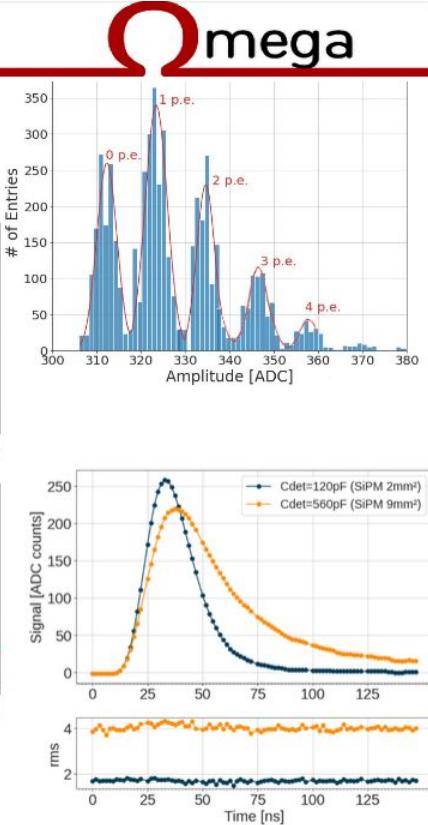
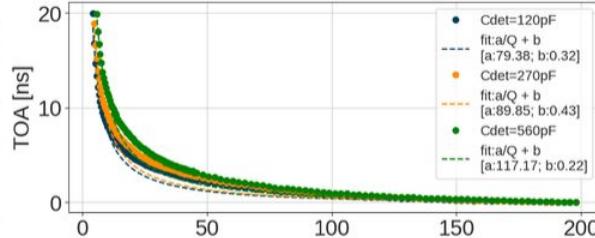
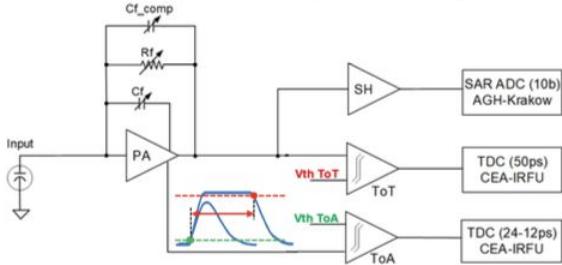
BIC design:

- SiPM+summing board

# CALOROC pre-brief material

## CALOROC1A (based on H2GCROC)

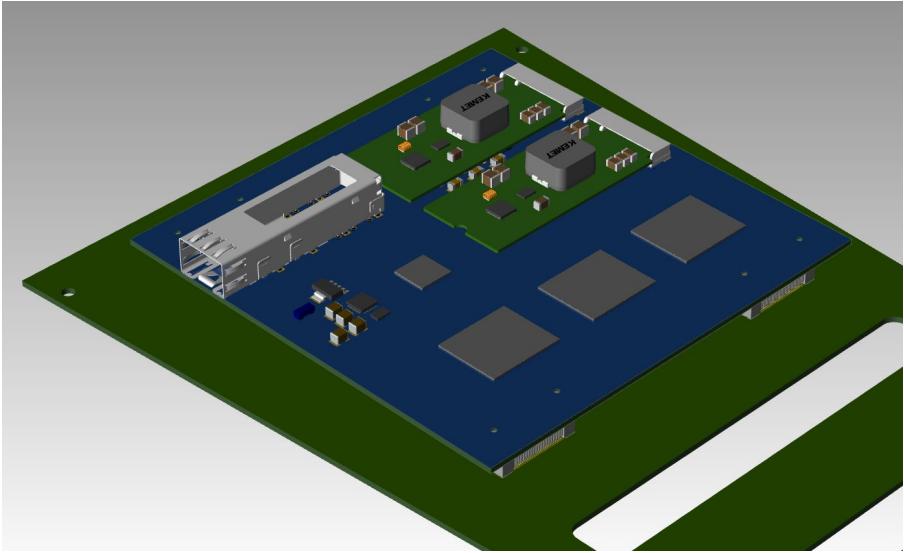
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized \*
- 15 mW per channel / Radiation performance / SiPM range 100-600 pF



- CALOROC1A will only update its back-end to be EIC compatible

\* TWEPP 2023 → <https://doi.org/10.1088/1748-0221/19/04/C04005>

# Front-End Board - CALOROC



CALOROC number of channels 36, minimum 2 is required:

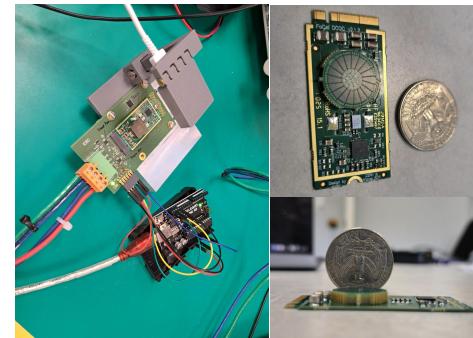
- 3 CALOROC is an option to increase the channel count (simulation studies are ongoing)
- Enough space for all the components
- There is more information in the pre-brief material about CALOROC

Will include also LV power distribution for the ETC and Astropix sensors

The front-end board (FEB) for the SciFi layers:

- Low voltage power via DC/DC bPOL48 converters, input ~30V, 3.3V output, 1.5V output
- LDO's near the ASICs: 2.5V, 1.2V needed
- SFP+ for communication
- LpGBT
- 1-3x CALOROC ASIC

Except the SFP+, all components are radiation tolerant. SFP+ has to be tested or find alternative



# Test article – SiPM board readout



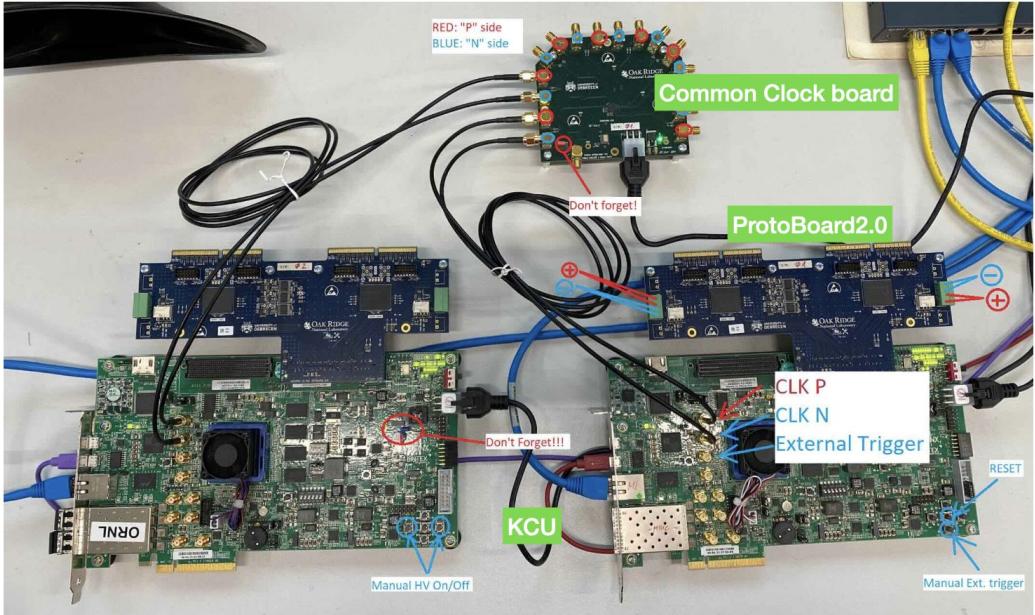
## U Regina

- Baby BCAL:
  - Mini boards reflowed week of Sept 8
  - Electrical testing and scintillator plus  $^{90}\text{Sr}$
  - Window and summing boards to arrive in ~3 weeks
  - Electrical tests and full assembly at U Regina (by mid Oct)
  - Integration tests with H2GCROC at ANL (late Oct)
- PED BIC
  - Mini boards + window board OR + cables
  - Cooling
  - By early 2026
- FDR Test Article spring 2026; Preprod Jun 2026; Prod-Ready Oct 2026

# Test article – H2GCROC protoboard



From ORNL



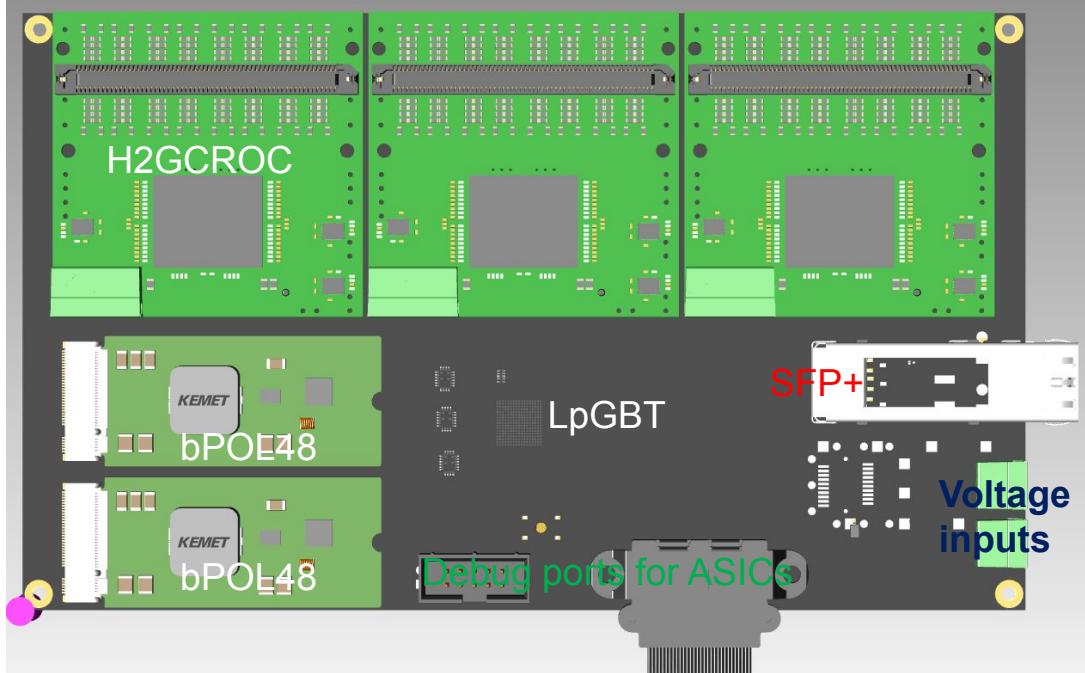
Currently available H2GCROC protoboard:

- Same analog design as in the CALOROC1A.
- Readout via a KCU105 evaluation board, multiple readout boards can be synchronized for large scale tests
- In total there are 20 protoboards available within ePIC

Purpose:

- First CALOROC will be available in early 2026
- H2GCROC is very similar, except self-triggering and zero-suppression
  - This can be simulated in the FPGA

# Moving towards CALOROC



First test article for the H2GCROC/CALOROC board:

- The purpose is to construct a test article for ASIC testing
- H2GCROC ASIC is available, same 2x1.26Gbps data lines
- CALOROC will be available in early 2026, mezzanines can be replaced
- SFP+ fiber □ towards RDO/DAM readout board

***Test the full-chain readout from SiPM to DAM board***

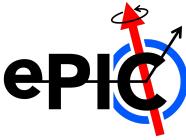
# Test articles – ETC

NASA/GSFC



- AstroPix ETC-specific design was delayed due to extensive delays in processing the contract
- GSFC has designed 3 systems for AstroPix readout
- test bench readout
- A-STEP sounding rocket
- COMPAIR-2
- Work will begin on the ETC design very soon, now that contracts have been signed between GSFC and DOE.
- No show-stoppers expected; design is at 60% (and likely more)

# Plans to work towards final design



## HGCROC

2025 July-December:

- Test SiPM signals with H2GCROC protoboard
- Feedback to the CALOROC analog part requirements

2026:

- First test with CALOROC ASIC
- Progress on the CALOROC FEB with the ETC/Astropix requirements
- Finalize the number of channels, preamplifier settings, etc for the ASIC production

2027:

- Finalize the FEB design and test

## SiPMs

- 2025 October – window and summing boards
- 2025 November – integration with HGCROC at ANL
- 2026 April – Preproduction

## ETCs

- Update from NASA coming soon

# QC/QA, Safety

We have three labs to lead the testing sites: ANL, NASA, ORNL

Universities (students/postdocs) will be trained to perform testing either locally or at the laboratory centers

## SiPMs:

- QC/QA procedures based on GlueX (see pre-prief material)
- Common procedure will be developed

**CALOROC** testing: Using in multiple calorimeters, we will develop a common platform for accepting them

- ❖ Together 3-4k ASICs to test, about 3-4 weeks with the robotic arm in LLR France

## LpGBT, bPOL48 modules:

- ❖ Used widely in ePIC, common testing phase
- ❖ LpGBT and bPOL48 are usually tested at CERN
- ❖ LpGBT will be validated in ORNL

## FEB production and testing:

- ❖ Together 2x48 end of sector FEBs
- ❖ X-ray image on the BGA
- ❖ This will be swift, allocate 1 week at most

## ETC:

- ❖ ~ 400-500 boards to produce and test

## Safety:

We will follow the standards from ANL, BNL, ORNL and NASA

# Plans for pre-production and production



- SiPM board and summing stage:
  - Test article on the Baby BCAL is currently constructed (FY26 Q1)
  - Test article for final design will be produced in FY27
- Following the ASIC schedules:
  - Astropix v5
  - ETC first test article FY26 Q3
  - CALOROC expected FY26 Q2, production in FY27
  - CALOROC readout board FY26 Q1 (compatibility with H2GCROC)
  - Combine ETC - CALOROC to ESB - FY27 preproduction - Integration
    - Production in early FY28

# Summary



- HGCROC tests continuing at ANL and ORNL
- ETC progress hoped for soon
- SiPM: Achieve BIC PED goals in two stages:
  - test operation of compact/miniatuerized electronics without cooling on Baby ECal ESB
  - implement lessons in electronics for BIC ESB and incorporate ESB cooling

# Transition Title

# Instructions–deadlines (to remove later)



Thank you for your participation in the PDR Review!!

## Internal deadlines (to be discussed):

- Outline drafts of presentations: next Thursday 8/21
  - enable us to ensure all parts are covered and not duplicated
  - bullet points on slides of what you plan to discuss
  - upload to FY25 BIC PDR folder
- Presentation draft (decent) shared with GTL 8/26
- Pre-brief materials/documents draft: 8/28

## From the EIC project:

- Page Turner: August 28th →FINAL slides walk-through
  - **Date and Time:** Thursday, August 28, 2025 @8am-4pm EDT
  - **Indico:** [Page Turn/ Dry Run - Review of the ePIC Barrel Imaging EMCal \(28 August 2025\) · Indico](https://indico.cern.ch/event/1054544/) password: PDR2054BIC
- Pre-brief Material Posted for reviewers: September 5th
- Final presentations posted: September 9th
- PDR Review: September 17-18
  - start at 8:30 am EDT

# Pre-Brief Materials



From the charge: You will be supplied with the detailed schedule and manpower assumptions, drawing packages, copies of presentations relevant to this subject material, and the project milestones extracted from the most current EIC resource loaded P6 schedule as part of the pre-brief material.

- schedule and personpower assumptions (by EIC project)
- drawing packages (by BIC)
- presentations (by BIC)
- project milestones (by EIC project)
  
- BIC Interface document
- BIC Merlin schedule

# Instructions–to remove later



Charge:

- 1. Is the progress and design maturity of the barrel electromagnetic calorimeter systems aligned with being baselined in June 2026 (>60% maturity is required)?**
2. Are the technical performance requirements appropriately defined and complete for this stage of the project?
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- 4. Are the current designs and plans for detector and electronics readout likely to achieve the performance requirements with a low risk of cost increases, schedule delays, and technical problems?**
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7. Have ES&H and QA considerations been adequately incorporated into the designs at their present stage?
8. Have the recommendations from previous reviews been adequately addressed?

# Outline–Instructions (to be removed later)



**Presentations should be no more than 20 slides of content, 20 minute presentation (shorter ok)**

- Overview (2 slides)
  - introduce parts, scope (some intro in general talk)
- Design (5 slides)
  - component design or designs for setups for building/testing (show drawings)
  - do they meet technical specifications or performance requirements? what are the specifications?
  - what are the interface criteria?
  - what are any open points to be done before the FDR?
- Test Articles (4 slides)
  - demonstrate major technical challenges are understood
  - how does the performance compare with expected/required?
- Plans for work until the Final Design (review, June 2026) (1 slide, if applicable)
- QA/QC Plan (1-2 slides)
  - for production: QA done at a batch level or fraction of parts, QC done on 100% of parts
- Safety (1 slide)
  - what safety features are part of the BIC design
  - identify how sites deal with safety (ANL: Work Control Documents), what are the highest hazard tasks, who are the contact people
- Plans for Preproduction, Production (1-4 slides)
  - what are the biggest challenges? schedule, cost, technical performance? How are you dealing with it (mitigating risk)? What is the actual plan?