FCFD Variant for RICH Detectors

July 2026 Joint ePIC/EICUG Meeting

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U.S. DEPARTMENT of ENERGY

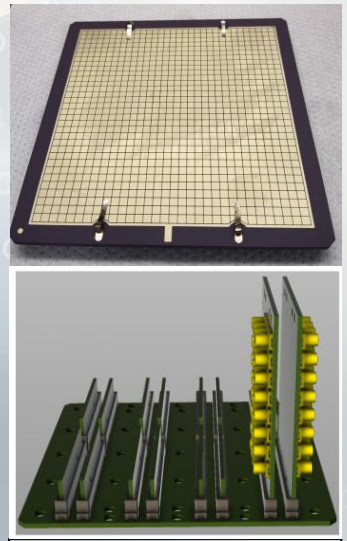
Background

- Raymond Dawson – Electronics Engineer at Jefferson Lab
- Responsible for electrical design of HRPPD sensor, and front-end electronics and ASIC integration into pfRICH and hpDIRC
- Goal for meeting: Converge on each detector's requirements for FCFD design

- Agenda
  - Current status
  - Preliminary testing results of the HRPPD with the FCFD
  - Timing analysis with FCFD
  - Mechanical concept
  - Power consumption
  - Data readout
  - Next steps
  - Detector specifications for FCFD
  - Discussion

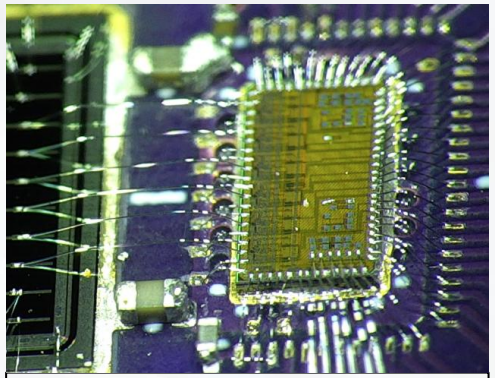
Current Status

- Next revisions of HRPPDs ordered in June
  - Updates for assembly and improvements to signal integrity
- Preliminary testing and analysis performed with FCFDv1.1 (analog front-end)
  - Testing resumes after HRPPDs return from CERN
- FNAL group starting design of FCFD Variant v1.2
- Preliminary mechanical envelope and cooling design started

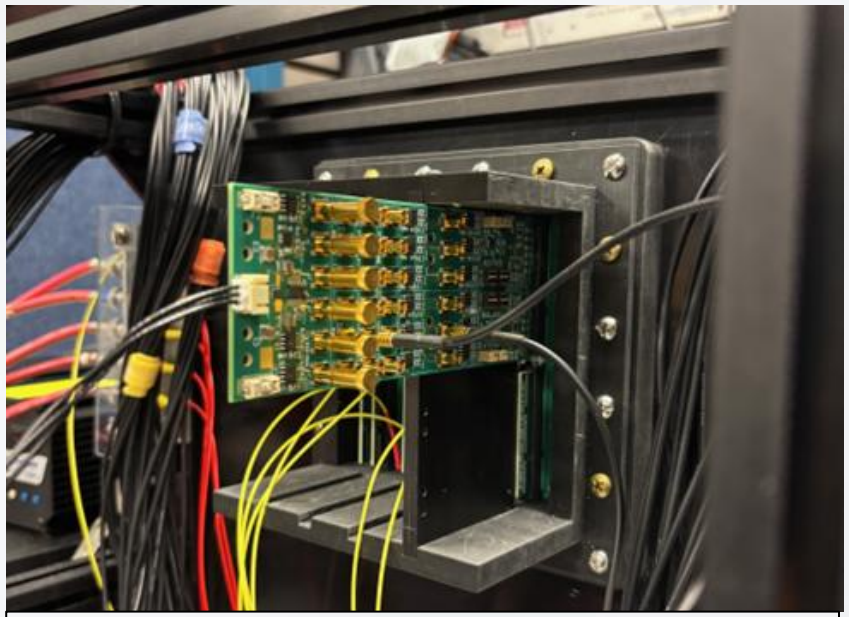


HRPPD and Front-End Electronics

FCFDv1.1 Variant Front-End Board

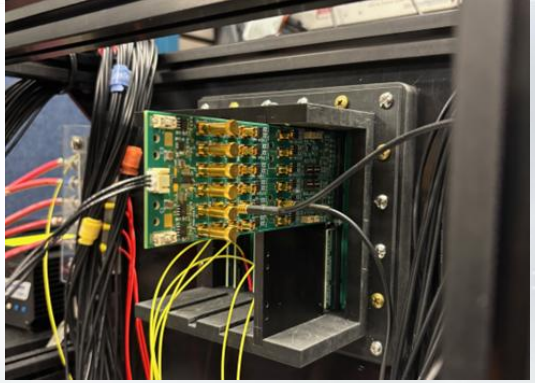


FCFDv1.1

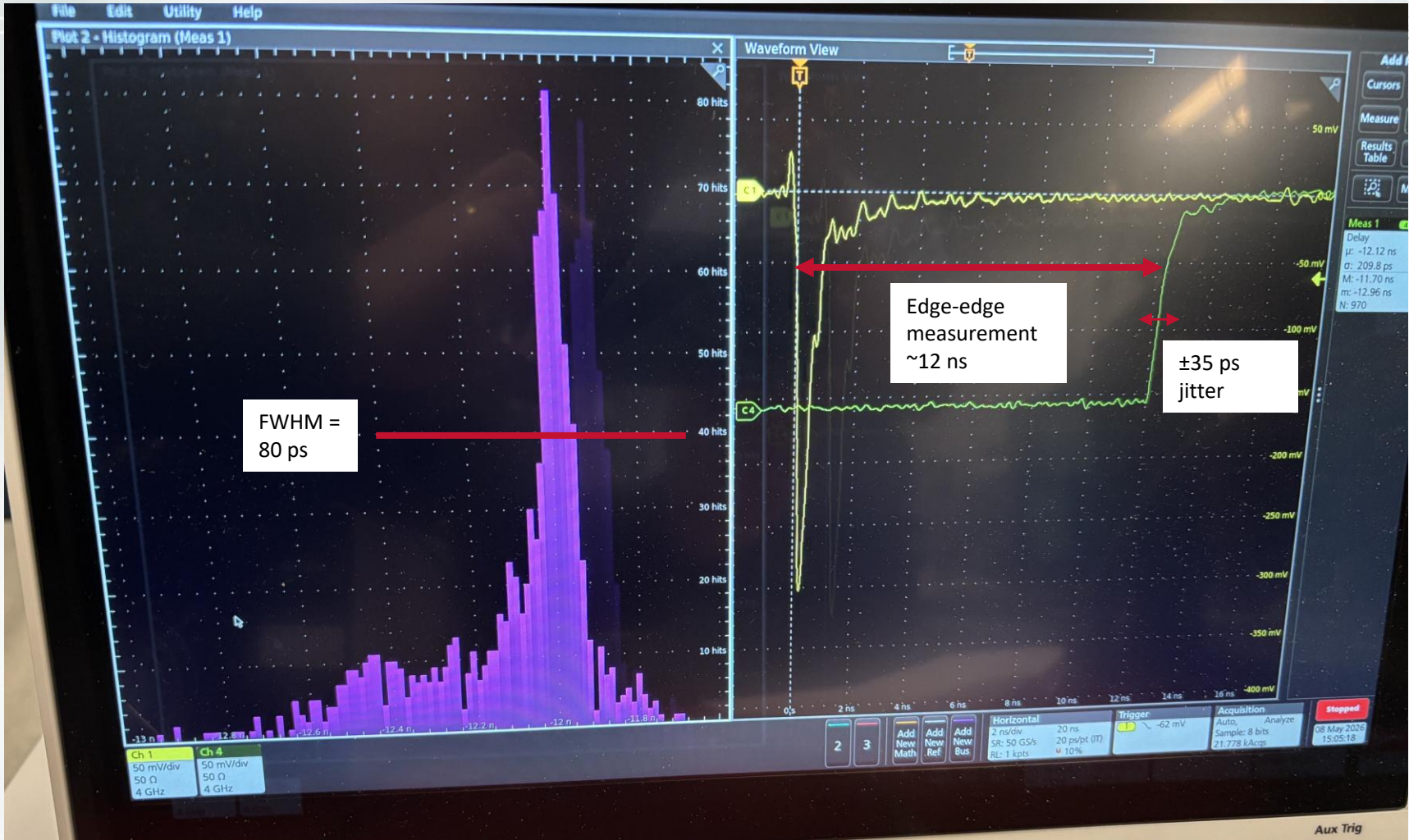


Test setup with FCFD FEB installed on HRPPD

Initial Laser Testing with HRPPD



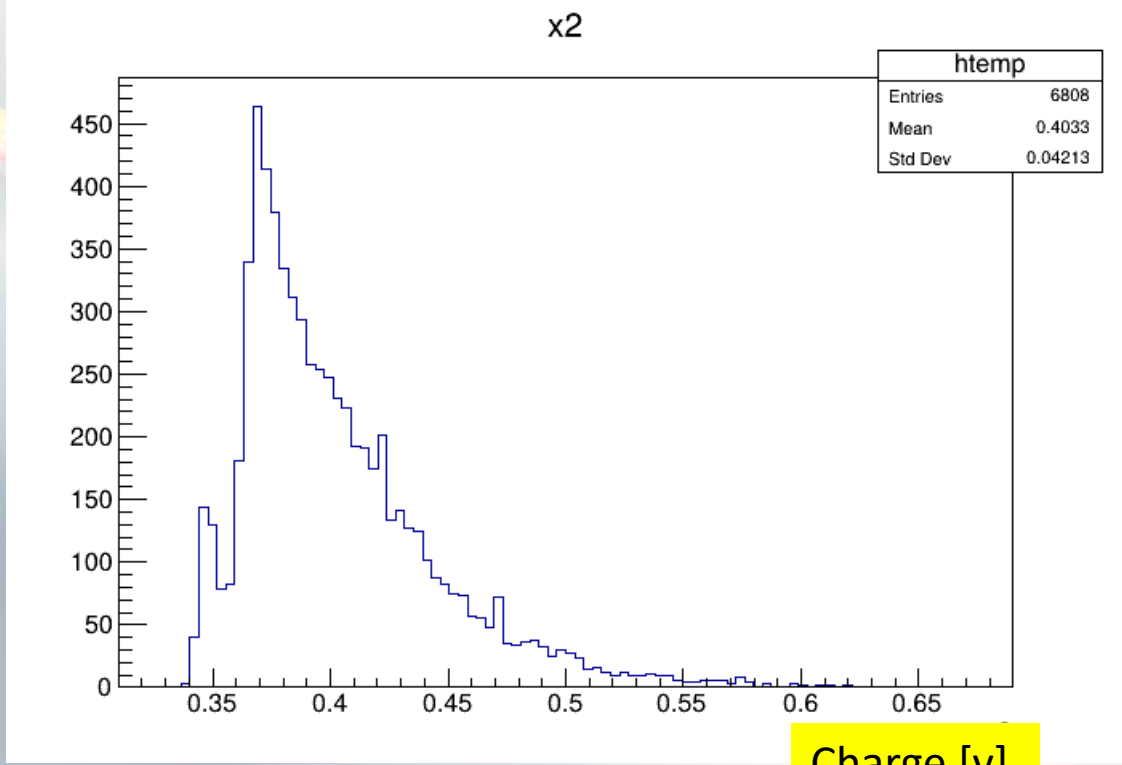
- Test setup:
  - True timing response of laser measured with fast photodiode and HRPPD
  - Laser was diffused over area, not exactly centered on pixel
    - Gain was low 10^5, low 1-2mV signals
  - Yellow is photodiode response
  - Green is CFD output of ASIC
  - Histogram records response time difference of photodiode from CFD
    - ~1k samples
  - Lead and tail ends could be charge sharing, small signals, noise, dark pulses, reflections
- Results
  - FWHM = 80 ps
    - 6 bins above FWHM line
    - Each bin is 13.3 ps, 3 bins per division
    - Each division is 40 ps
  - Std dev = ± 35 ps
- Seems promising as a first run but obviously much **more testing is required**
  - Data is essentially filtered for good pulses because trigger is photodiode and not CFD
  - Need to assess gain and noise impacts



Timing Analysis

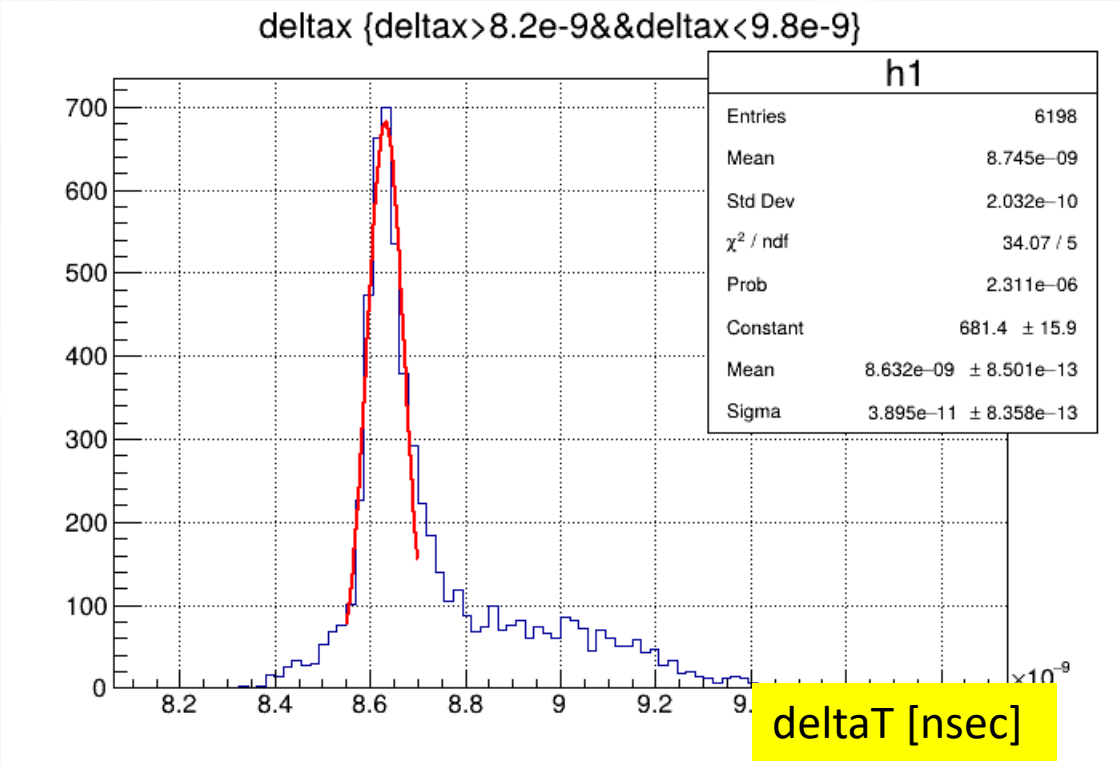
Charge distribution of data (in volts)

- Peak voltage amplitude from FCFD
- Voltage equates to charge
- Testing was run at few ~10^5 gain (1-2mV signals)



Timing resolution distribution of CFD output

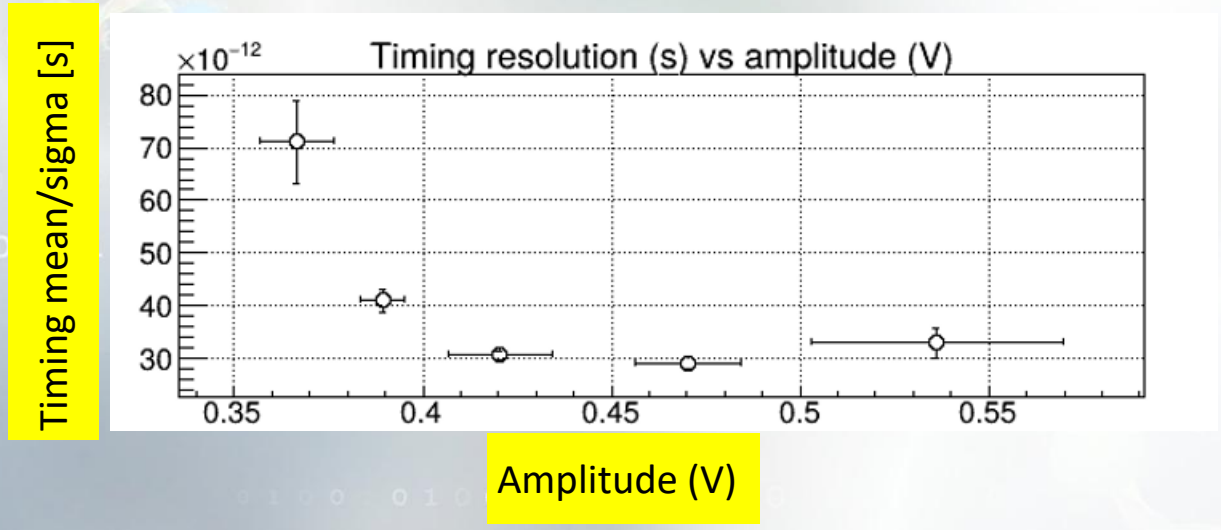
- Showing time difference CFD and photodiode
- Setup modified: 12ns -> 8.65ns
- Sigma = 38.95 ps
- Target = 40 ps



Timing Analysis

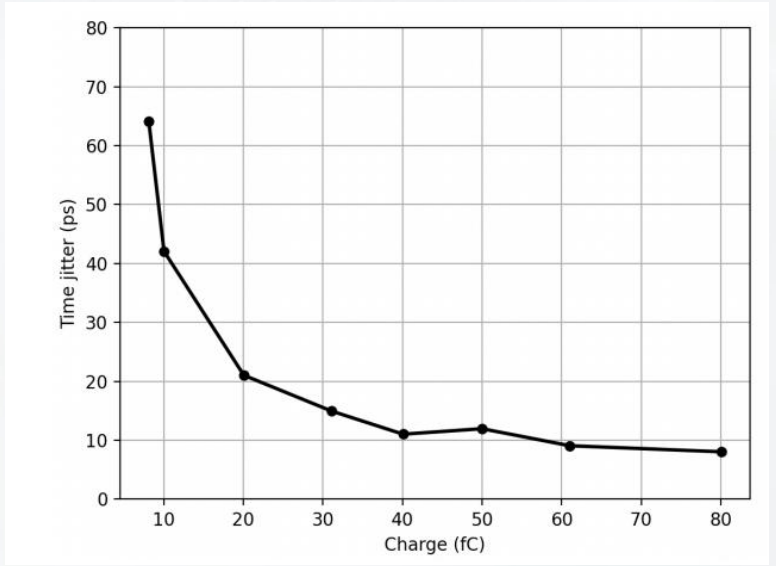
Time resolution of the FCFD with the HRPPD

- Time resolution @ different charge amplitudes
- Timing behavior follows that of FNAL testing with AC-LGAD

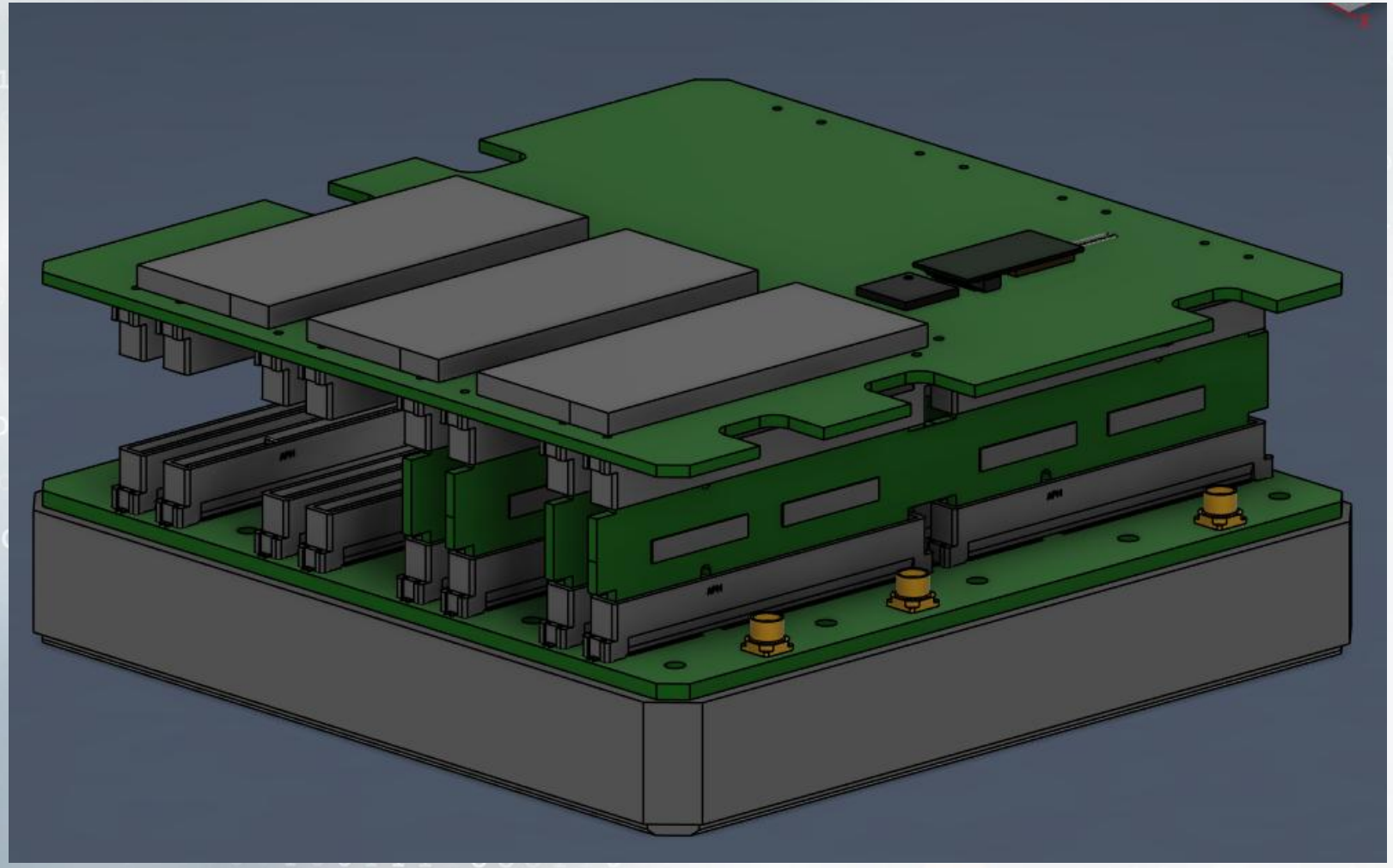


Time resolution of the FCFD with the AC-LGAD

- This is the plot directly from the FCFDv1.1 paper
  - "Optimization and Performance Characterization of the Second Generation Fermilab Constant Fraction Discriminator Readout ASIC"



Mechanical Concept



Parts per HRPPD

- 16x interposers + 1x spacer
- 1x backplane
- 8x FEBs + 32x FCFD 32-ch
- 1x bridge/father card
- 3x bPOLs (LV connector not shown)
- 1x lpGBT + VTRX+

- 68 HRPPDs in pfRICH
- 72 HRPPDs in hpDIRC

- Dimensions:
  - LxW: 121.8 x 121.8 mm @ enclosure
  - H: 51.5 mm

Power Consumption per Detector

- Power per HRPPD: 10.5 W
  - 8x FEBs (32x FCFD) + lpGBT/VTRX+ = 9W + 1.5W = 10.5W
- 716 W for whole pfRICH
  - 68 units
- 756W for whole hpDIRC
  - 72 units
  - 6 HRPPDs per crate = 63W

Parts	Per unit	QTY
FCFD (32-ch)	~200mW	4
bPOL48	~70% eff	1 per line
Per FEB	~1.13W	8
Total	~9W	Per HRPPD

Parts	Per unit	QTY
lpGBT	750mW	1
VTRX+	300mW	1
bPOL48	~70% eff	1 per line
Total	~1.5W	Per HRPPD

Data Format and Rate for pfRICH

- Data format
  - Semi-official number: 160 bits/hit (max)
    - 5-bit ADC + 8bit TDC + other info = 64 bits/ch
    - Header(H) + trailer(T) + filler (F) = 96 bits/ch
  - H+T+F may be merged for channels hit at same time
- Data rate
  - lpGBT + VTRX+ bandwidth vs average hit rate
    - 200Mbps per HRPPD with ~6kHz average hit rate
      - Requires 13.6Gbps from pfRICH as whole
    - Bandwidth of lpGBT + VTRX+ with FEC10 encoding is 7.68Gbps (10.24Gbps mode)
      - Two sets of lpGBT + VTRX+ cover ENTIRE pfRICH
      - Will have 1x lpGBT + VTRX+ per HRPPD
  - FCFD bandwidth vs maximum hit rate
    - Max rate from a pad is 20kHz → 3.2Mbps/pad → 102Mbps/32ch
    - Fits 32-ch FCFD data bandwidth of 320Mbps/chip

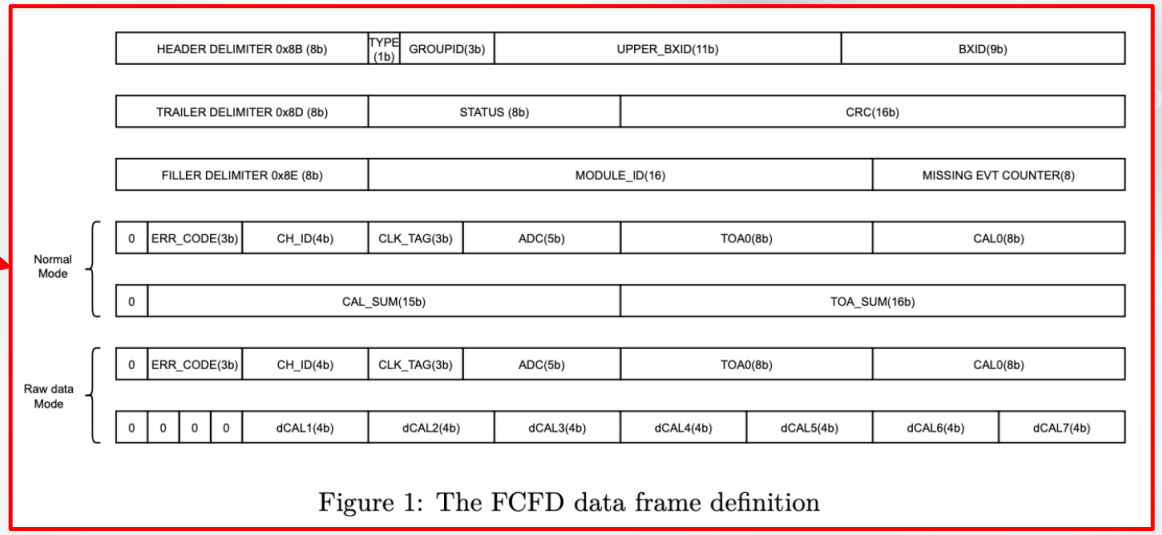


Figure 1: The FCFD data frame definition

Next Steps

- Outstanding issues
  - Impedance matching solution
- Sign off on Variant v1.1 specifications for pfRICH and hpDIRC
  - As soon as possible, Variant fab is ~4 months
- HRPPD with FCFDs
  - Testing will resume in August to characterize gain and noise
- Electronics
  - Design new backplanes with updated high voltage design
  - Create new FEB with FCFDv1.2 to test digital backend since Variants won't be ready until early next year
- FNAL
  - Started front-end design based on preliminary specs
  - Development cycle: Variant 1.2 (6-ch front-end + digital backend) -> 2.0 (32-channel) -> 3.0 (production)
  - Requested an HRPPD to characterize sensor for ASIC development

FCFD Specifications (Tentative)

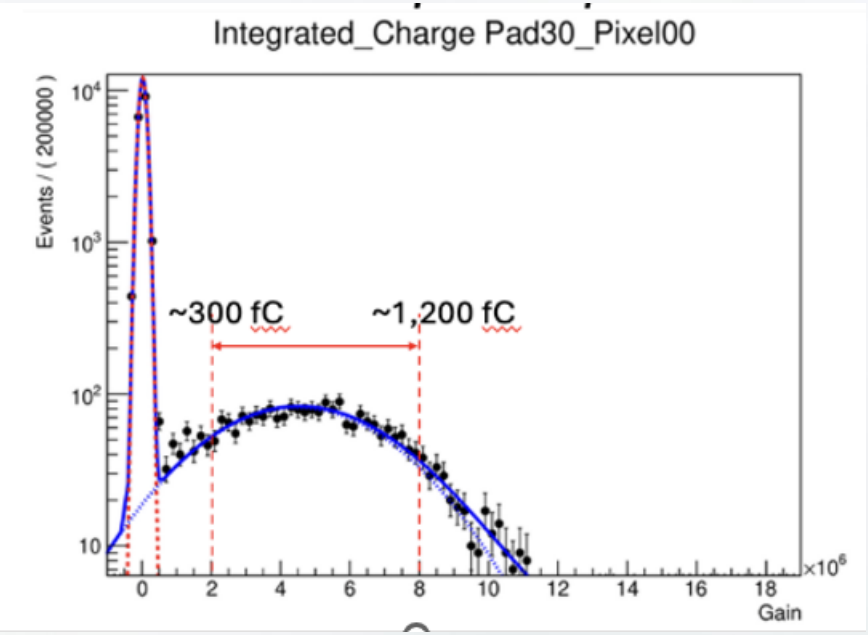
Detector	Channel Capacitance	Channel Rate	Time resolution	SPE Time and Charge Measurement Dynamic Range	Multi-photon Threshold	Charge Measurement Resolution
pfRICH	~10-15 pF	20 kHz max	~40 ps minimum	100 - 1,200 fC [10^6] (10 - 120 fC [10^5])	5-10 SPE	TBD
hpDIRC		~10 kHz		TBD	Not needed	TBD

Assumptions:

- Time resolution for hpDIRC same as pfRICH
- pfRICH region of operation defined within pictured area at 10^6 gain
- Low end of 100/10 fC to account for x3 pixel-pixel gain variations

Notes:

- Dynamic range dependent on final selected gain (TBD)
- hpDIRC is SPE only
- For multi-photon events in pfRICH:
  - Event will hit multiple pads in a cluster with majority clustered on the center pad
  - Center pad will have large charge (10+ SPE) – need to protect FCFD
  - Timing given by pads adjacent to center hit
  - Precise measurement of center hit not needed at high values
    - No timing needed
    - If charge available, then readout, but overflow bit is OK



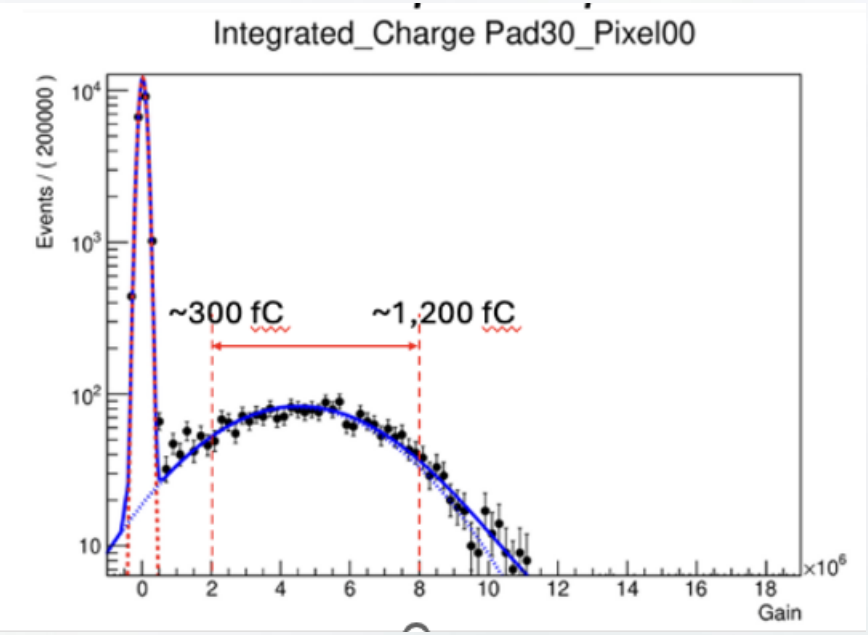
pfRICH Region of Operation @ 10^6 gain

Questions / Discussion

- How (or when) to settle specifications?

Detector	Channel Capacitance	Channel Rate	Time resolution	SPE Time and Charge Measurement Dynamic Range	Multi-photon Threshold	Charge Measurement Resolution
pfRICH	~10-15 pF	20 kHz max	~40 ps minimum	TBD 100 - 1,200 fC [10^6] (10 - 120 fC [10^5])	5-10 SPE	TBD
hpDIRC		~10 kHz		TBD	Not needed	TBD

- Hightlighted in red = need to confirm or plan to answer
- pfRICH
  - To settle SPE range, need to test FCFDs to characterize gain and noise
  - What is charge measurement resolution?
    - Defined by physics or electronics?
- hpDIRC
  - Is hpDIRC expecting a different SPE dynamic range than pfRICH?
    - Dynamic range needs to cover 95% of SPE charge range or data
    - Need to analyze test data at final gain to determine charge range?
  - What is maximum channel rate?
  - Will time resolution mimic pfRICH?
  - What is charge measurement resolution?
    - Detect 20% changes in charge
- General
  - How to incorporate 3x pad-pad gain variation into high end of dynamic range?



pfRICH Region of Operation @ 10^6 gain

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QUESTIONS?

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Appendix

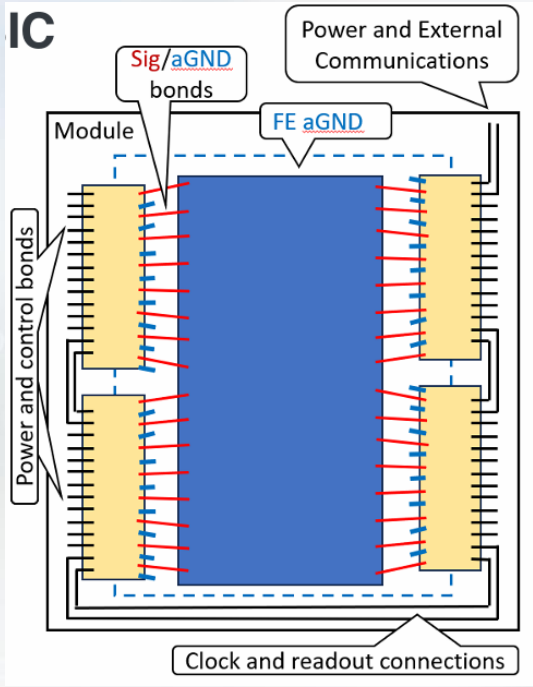
Mechanical Envelope

Notes

- Link to model
- Maximum height is 50 mm
  - Measured from window or lip?
- ASIC cards
  - FCFD estimated size 15x3 mm for 32 channels
    - Will need to be mindful of thickness of final board and connector, will require 10-12 layers
  - Used card edge connector on top side for expediency, probably a better solution
  - Connector height is estimated from FNAL estimate
  - ASICs may be wirebonded so no room for cooling pipes on ASIC side
    - Wirebonds will need protection
- Bridge card
  - bPOL model based off OTS CERN module, not sure if we will use custom
  - 2x VTRX+ modules included in model
    - Brian suggested more modules for redundancy and limit data loss on part failure
- How to reduce height?
  - Ballpark target height = 45 mm ± 10%?
  - ASIC card height could be reduced by ~2 mm
  - Shorten top side ASIC card connector

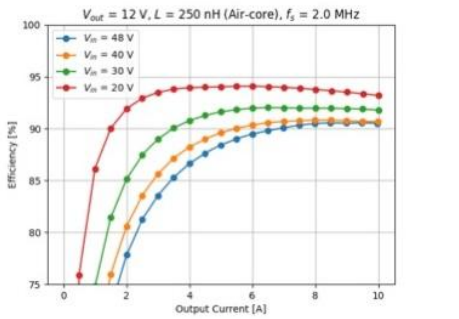
Chip	3mm
Sensor-ASIC gap	2-3mm
Back-side bonds	1mm
Extra routing area	2mm
pcb edge clearance	0.5mm
Total	**8.5-9.5mm**

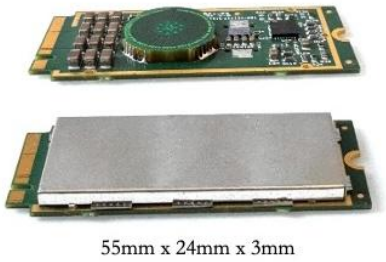
FNAL Estimate



bPOL48V module

Module optimised in volume, available in large numbers
Hosting:
- CERN GaN_controller ASIC
- CERN custom PCB air core inductor
- Commercial Gallium Nitride power stage

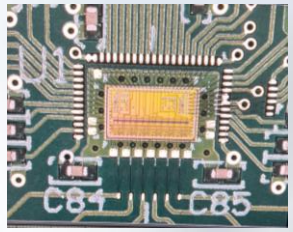




55mm x 24mm x 3mm

CERN Module

Power consumption of a 32ch-FCFD



- FCFD now goes for 32ch/chip.
- Previous number:
  - *Estimated from the table for 128ch.*
  - Analog 32ch: 3.8mW * 32 = 120mW
  - TDC+ADC 32ch: 0.2mW *32 = 6.4mW
  - Supporting Circuitry 32ch: 6.4mW
  - Global circuitry: 1per chip = 200mW
  - Total power per chip will be: 330mW
- New number:
  - *As presented at the TIC meeting*
  - Analog 32ch: 3.6mW * 32= 116.2mW
  - TDC+ADC 32ch: 0.2mW*32= 6.4mW
  - Supporting Circuitry 32ch: ?
  - Global circuitry: 1 per chip = 78mW
  - Total power per chip: 200mW.

Table presented by Artur at ePIC coll meeting on Jul 16, 2025

Circuit Component	Power per Channel [mW]	Power per ASIC[mW]
Preamp + Discr (low-*high power*)	2.1 - 3.8	269 - 486
TDC+ADC	0.2	26
Supporting Circuitry	0.2	26
Global Circuitry		*200**
Total (*high power*)		521 - 738

Table presented by Artur at TIC meeting on May 11, 2026

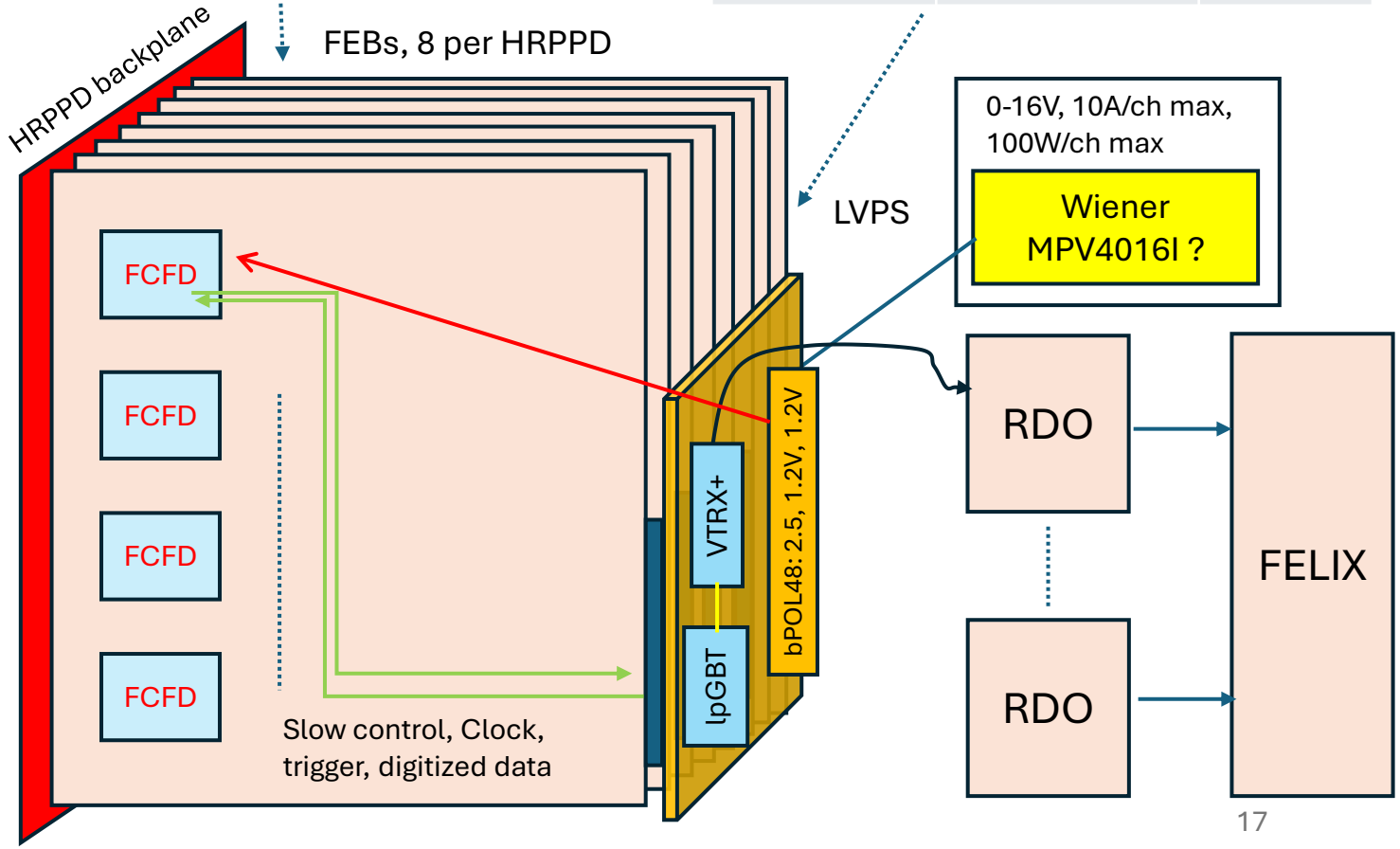
	Unit power(mW) (32-ch)	Unit power(mW) (128-ch)	Units in FCFD32	Units in FCFD128	FCFD32_Power(mW)	FCFD128_Power (mW)
analog_front (2.5V)	2	2.2	32	128	64	281.6
analog_front (1.2V)	1.6	1.8	32	128	51.2	230.4
TDC	0.2	0.22	32	128	6.4	28.16
eRx	1	1	2	1	2	1
eTx	2	2	1	1	2	2
Readout16	30	30	2	8	60	240
Serializer	3	3	1	1	3	3
fc_decoder	5	5	1	1	5	5
data_aligner	2	2	1	0	2	0
I2C	2	2	1	1	2	2
Total (mW)					197.6	793.16
Total (mW) for 2.5V					64	281.6
Total (mW) for 1.2V					133.6	511.56

Readout scheme and LV power consumption

- Average data rate (incl background):
  - Based on hit rate provided by Brian
  - 5bit ADC/TDC + ~20% hdr =12 bit/hit/pad.
  - 15Mbps per HRPPD
  - 1Gbps from pfRICH as whole
- Bandwidth of lpGBT + VTRX+
  - Max bandwidth for lpGBT with FEC10 encoding is 7.68Gbps. (10.24Gbps mode)
  - Whole pfRICH data could fit to this.
- Conceptual readout scheme.
  - Four (tentative) FCFDs per FEB.
  - FCFD output bandwidth: 320Mbps/chip
  - A Father board (FB) (a set of lpGBT and VTRX+) handles eight FEBs.
  - FB can handle multiple HRPPDs, but we should carefully design conn. diagram.
- Power: 1.1*8+1.6 = 10.4 W/HRPPD.
  - 707W for whole pfRICH. If we collect all data to one lpGBT+VTRX, we save 100W.
  - bPOL48 (DC-DC) eff. is assumed to be 70% in average (can be better).

Parts	Per unit	QTY
FCFD	200mW	4
bPOL48	~70% eff	1 per line
Total	~1.1W	per FEB

Parts	Per unit	QTY
lpGBT	750mW	1
VTRX+	300mW	1
bPOL48	~70% eff	1 per line
Total	~1.6W	Per FB



Data format and rate from 32ch-FCFD

- My previous estimate: 12bit/hit
  - 5 bit ADC + 5 bit TDC + 20% header
- (semi-)official number: 160 bits/hit (max)
  - 5 bit ADC + 8bit TDC + other info = 64 bits/ch
  - Header(H) + trailer(T) + filler (F) = 96 bits/ch
  - H+T+F may be merged for channels hit at same time.
- Number is consistent with statement also presented.
  - 130kbps / (30[Hz] * 32 [ch]) = ~135 bits
- Using Brian's average hit rate, it means:
  - 200Mbps per HRPPD, 13.3Gbps from pfRICH as whole.
  - Will need at least two sets of lpGBT+VTRX+.
  - Max rate from a pad is 20kHz → 3.2Mbps/pad → 102Mbps/32ch.
  - It still fits to FCFD data bandwidth of 320Mbps/chip
- Power estimate won't change.
- To be checked: Can the FCFD analog part handle 20KHz pulse rate? They assume 100Hz per channel...

Data format was presented for the first time.

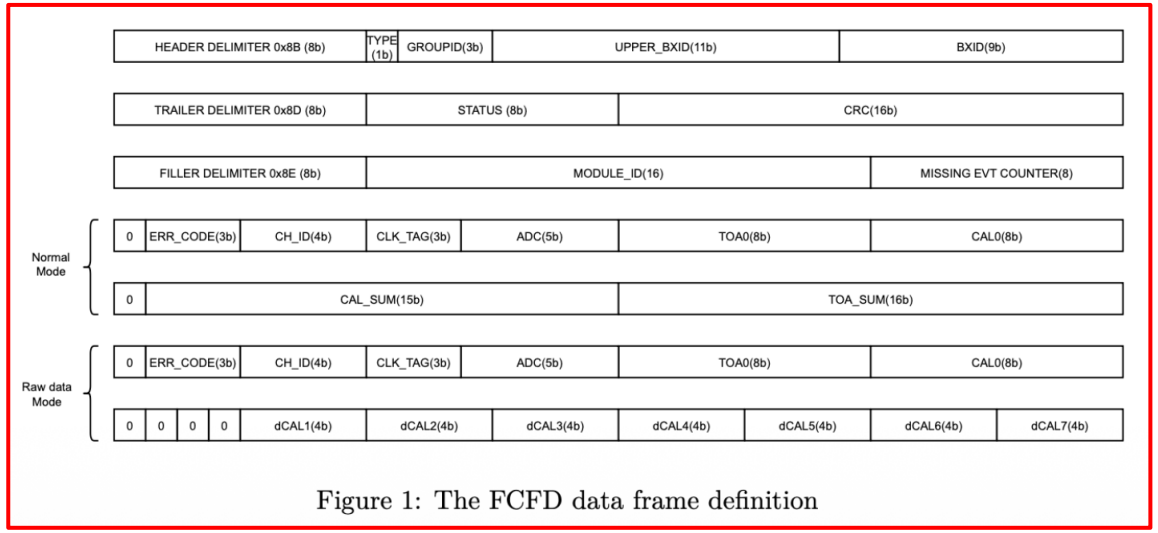


Figure 1: The FCFD data frame definition

- Assuming a hit rate of 30 Hz, the raw data rate per chip is approximately 130 kbps, which is far below the 320 Mbps bandwidth of a single ELink.

Bandwidth of lpGBT + VTRX+ with FEC10 encoding is 7.68Gbps. (10.24Gbps mode)

Data Rates

- Hit rate [/cm^2/s]
  - Hottest region: 200000
  - MPV: 6000
  - Peak region (75% of total): 5000 – 15000

- Convert Hit rate from /cm^2 to /pad: 9 pads occupy (0.325*3)^2 = 0.95 cm^2 -> Rate/pad = Rate/cm^2 * 0.95/9

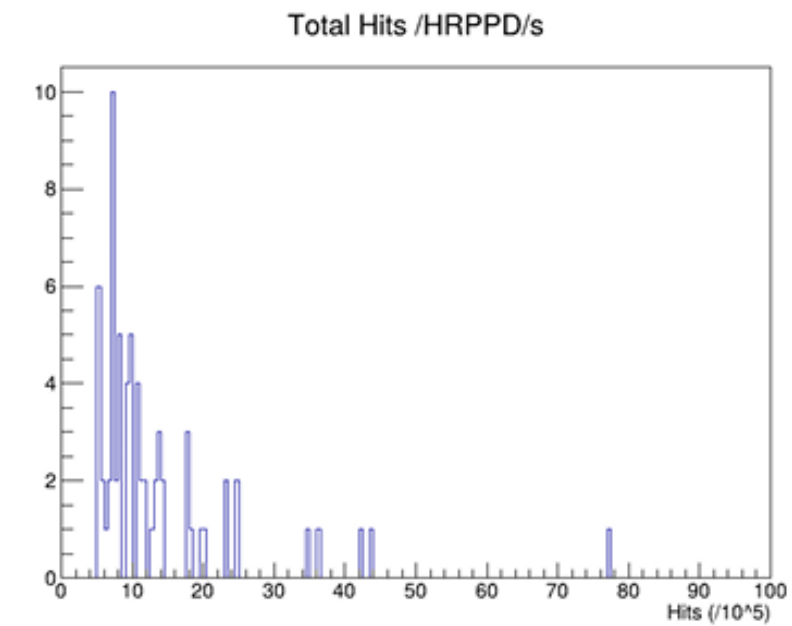
- FCFD data assumption: 10 bit (5 ADC and 5 TDC) + 20% (guesstimate)

- Data rate [Mbps/pad]
  - Hottest region: 0.25
  - MPV: 0.01
  - Peak region: 0.01 – 0.02

- For the hottest HRPPD: hit rate = 7.7M/s -> data rate = 93 Mbps

- Total pfRICH sees ~90M hits/s or ~1.1 Gbps
  - 80M Backgrounds hits/s
  - 10M Signal hits/s

- lpGBT+VTRX+ bandwidth of 7.7 Gbps -> lots of room



Questions / Discussion

- How to settle specifications?

Detector	Channel Capacitance	Channel Rate	Time resolution	SPE Time and Charge Measurement Dynamic Range	Multi-photon Threshold	Charge Measurement Resolution
pfRICH	~10-15 pF *	~20 kHz	~40 ps @ 100 fC	100 - 1,200 fC [10^6] (50 - 600 fC [10^5])	> TBD (2000 – 3000 fC?)	TBD
hpDIRC		~10 kHz		TBD	Not needed	TBD

  - Hightlighted in red = need to confirm or plan to answer
  - pFRICH
    - To settle SPE range, need to test FCFDs to characterize gain and noise
    - Why is time resolution only defined @ 100 fC?
    - For multi-photon events, is time and charge information needed or just a yes/no?
    - What is charge measurement resolution?
  - hpDIRC
    - Need to analyze test data at final gain to determine charge range?
    - What is expected channel rate?
    - Will time resolution mimic pfRICH?
    - Is hpDIRC expecting a different SPE dynamic range than pfRICH?
    - What is charge measurement resolution?
  - General
    - How to incorporate 3x pad-pad gain variation into dynamic range?