NUCLÉAIRE & PARTICULES

Omega

ÉCOLE POLYTECHNIQUE

IP PARIS

CALOROC status

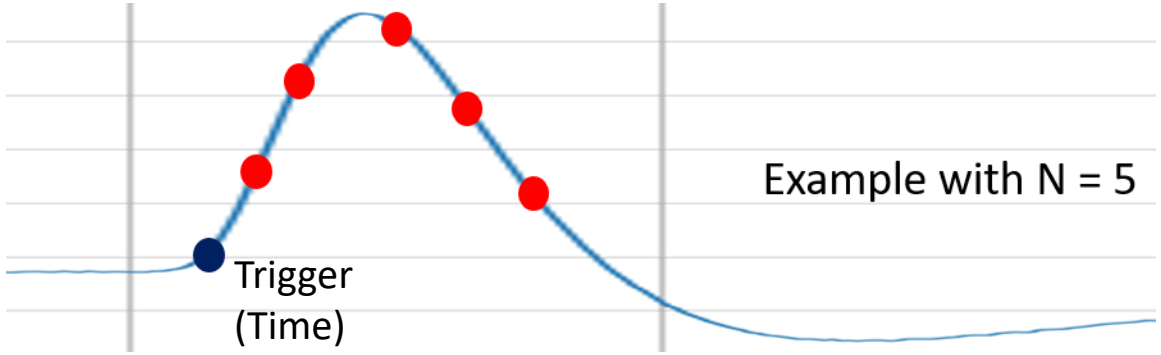
July 2026

Pedro Pablo Dumas Ziehlmann – pedro.dumas-ziehlmann@omega.in2p3.fr
Ecole Polytechnique – CNRS

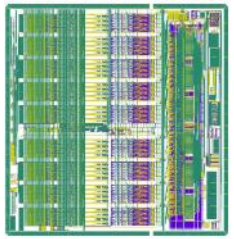
Organization for Micro-Electronics desiGn and Applications

CALOROC: Waveform Digitizer for SiPM Readout

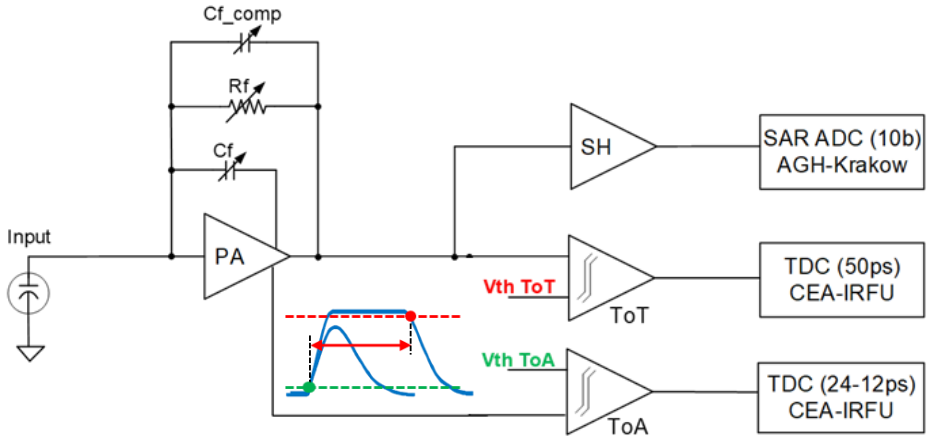
- CALOROC main changes:
  - Released in 2 versions: CALOROC-A and CALOROC-B
  - New 6-layer substrate – BGA (common)
  - New digital processing (common)
  - New testboards (common)



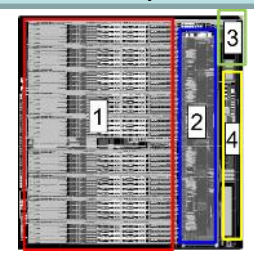
CALOROC 1A
CMS front-end
Low SiPM capacitance



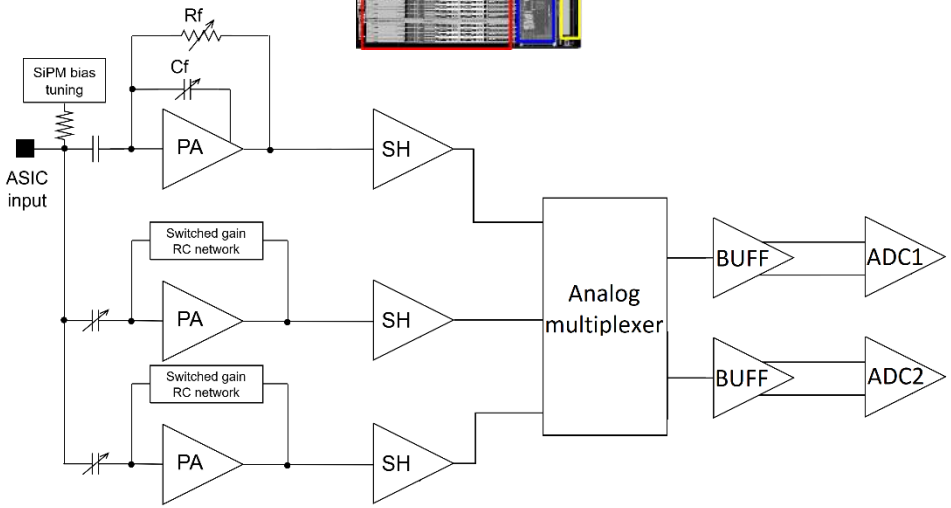
Measurements in progress



CALOROC 1B
New switched-gain front-end
High SiPM capacitance

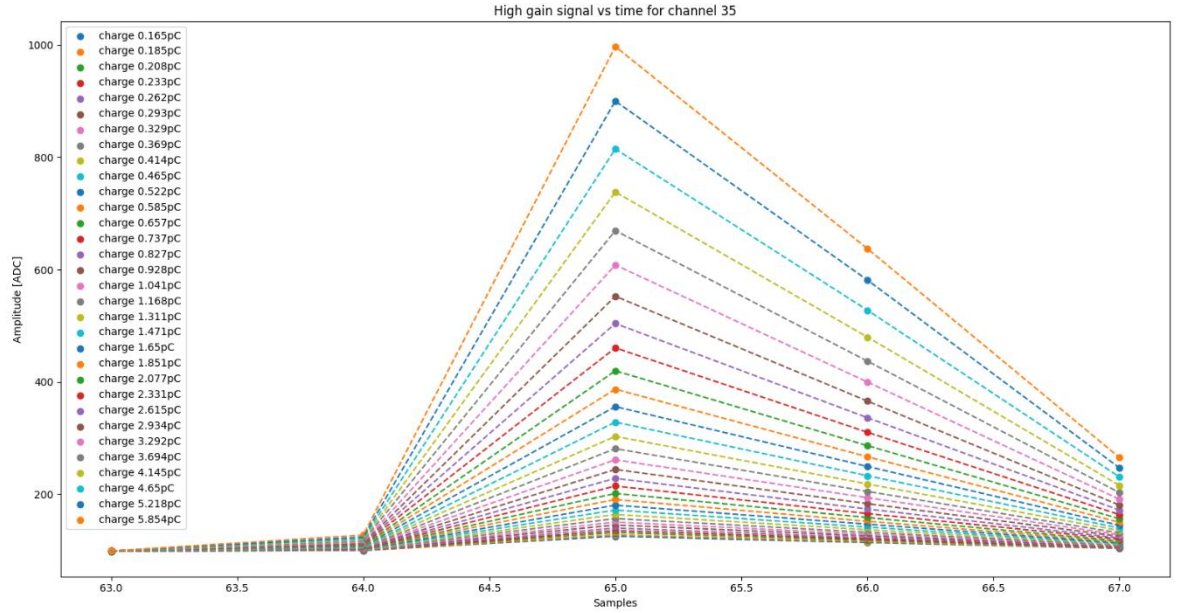


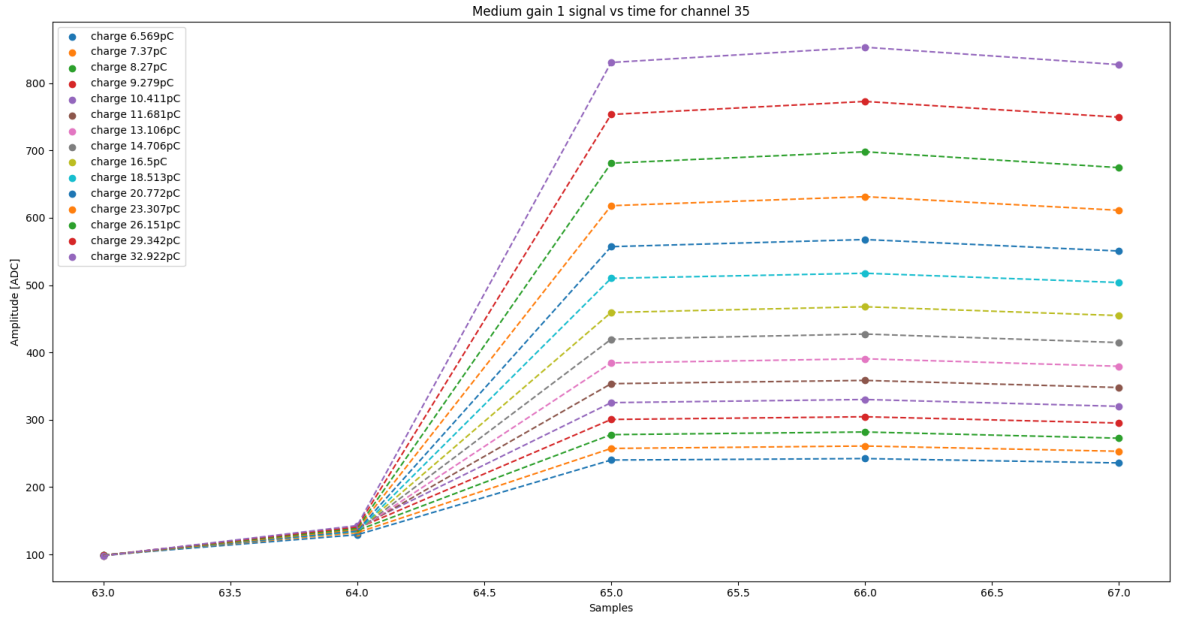
Measurements in progress



High Gain and gain switching Waveform Measurements

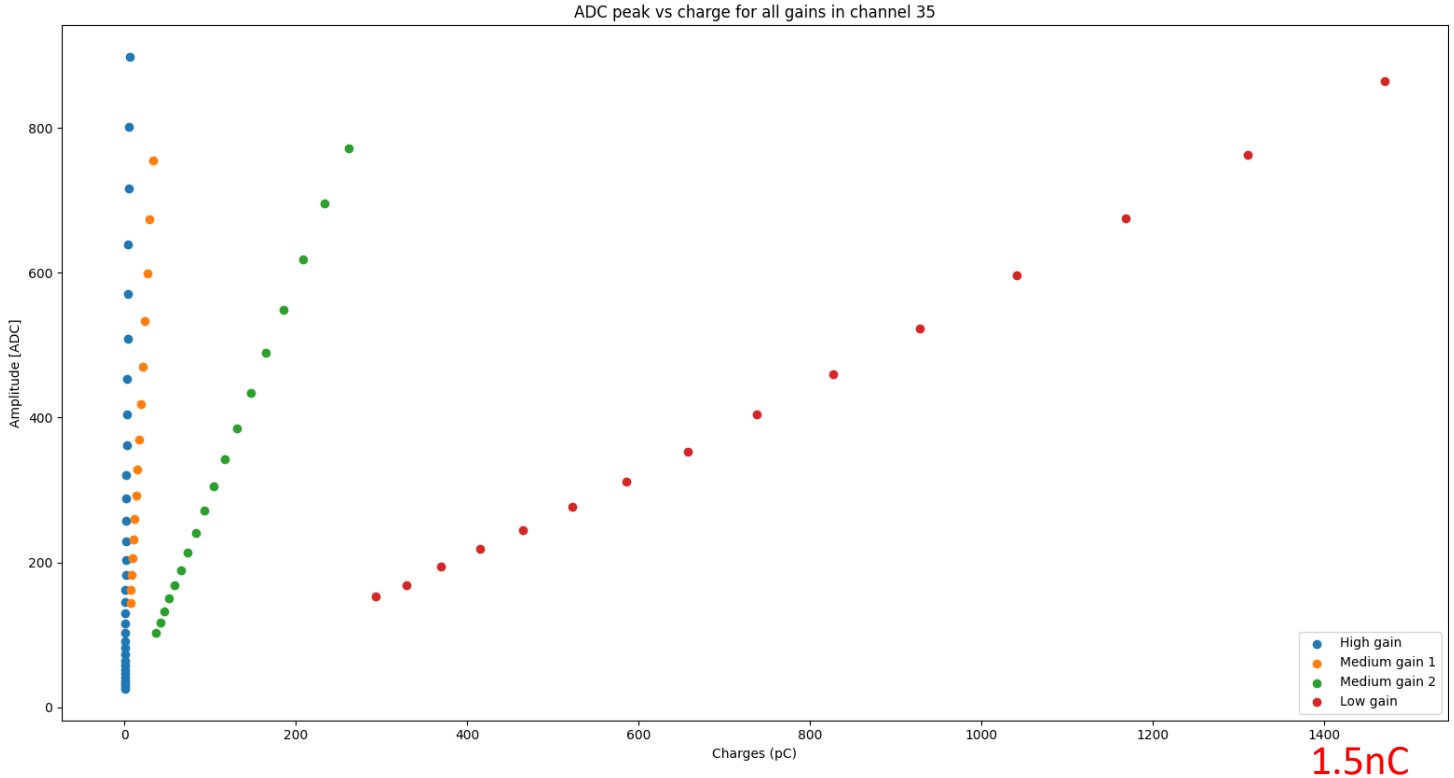
- Using internal injection of the ASIC:
  - Without autotrigger
  - Using fast commands to force autotrigger
- Using 5 samples (1 baseline + 4 signals)
- Time to peak of 25ns for the high gain signal
- When using the gain switching, the signal becomes wider as expected .
- Full waveforms available in the backup



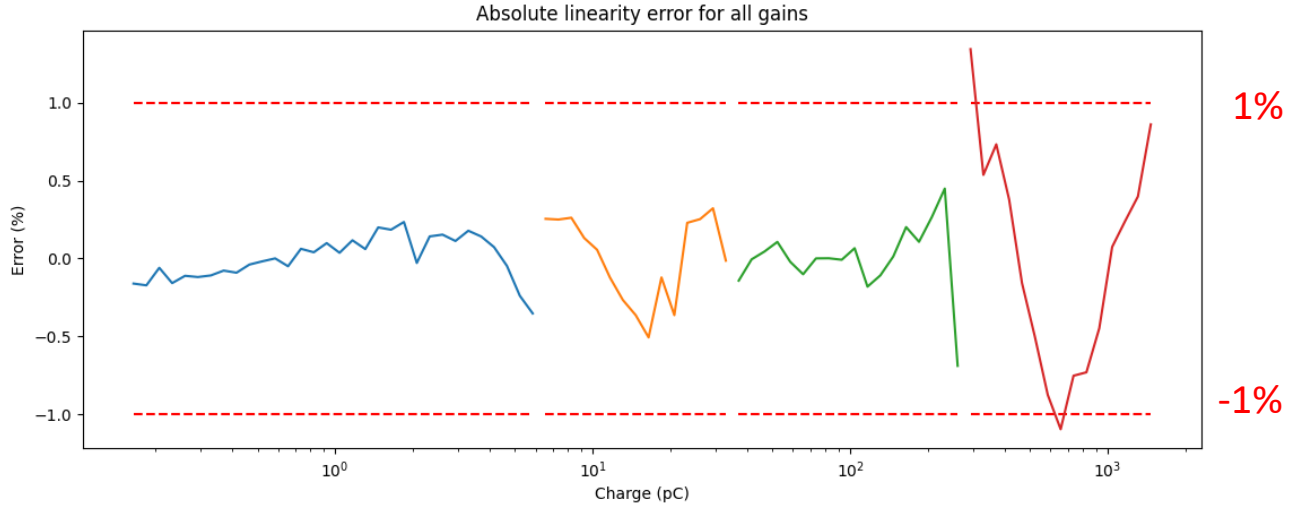


Linearity and full dynamic range

- External charge injection setup:
  - 2.2nF detector capacitance
  - 330pF injection capacitance
- Results:
  - Dynamic range of up to 1.5nC
  - Linearity error of less than 1% for all gains except the low gain
  - Linearity error close to 1% for the low gain
- Results are well within the requirements



1.5nC

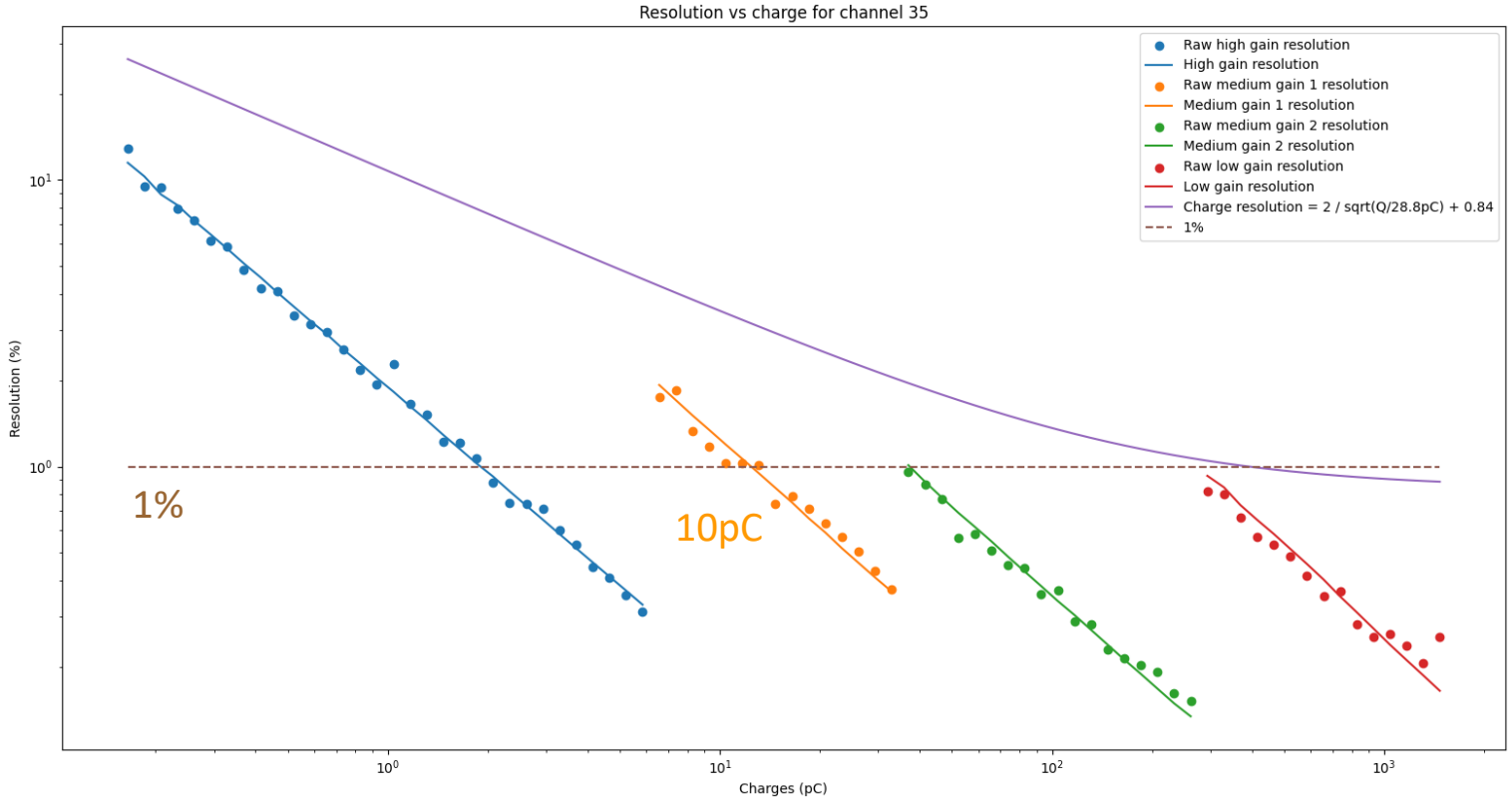


1%

-1%

Charge resolution as a function of the charge (Cd = 2.2nF)

- Resolution results:
  - Medium gain 1 higher noise than expected (50% more than on the previous PCB).
  - High gain has a lower gain than usual due to the slower injection signal.
  - RMS noise under 1% of the signal for the medium gain 2 and low gain.
  - RMS noise of 15fC in high gain



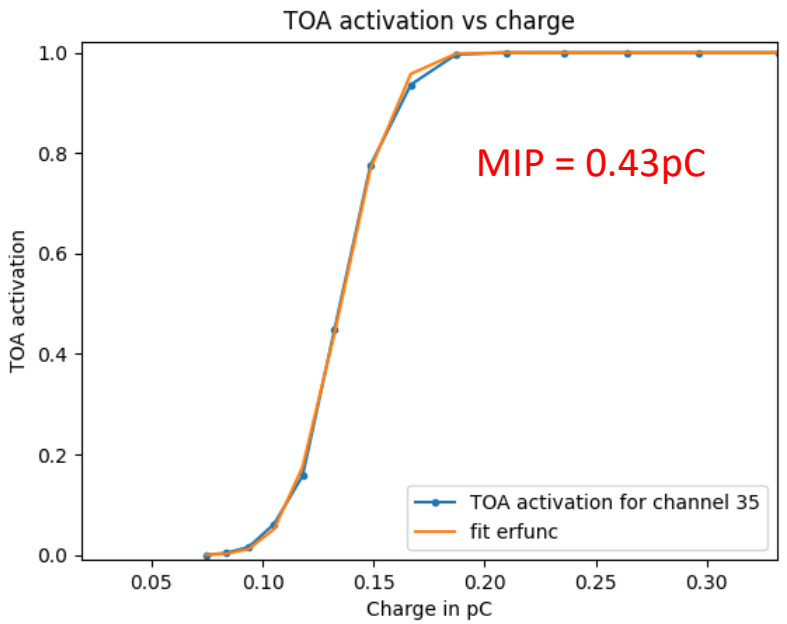
Setups	560pF detector (measurement)	2.2nF detector (measurement)	560pF detector (Simulation)	2.2nF detector (Simulation)
Cin	560pF	2.24nF	560pF	2.24nF
Noise	4.2fC	15fC	3.2fC	11fC
SNR @ 1p.e (≈30fC@gain=1.8e5)	7	2	9	2.6

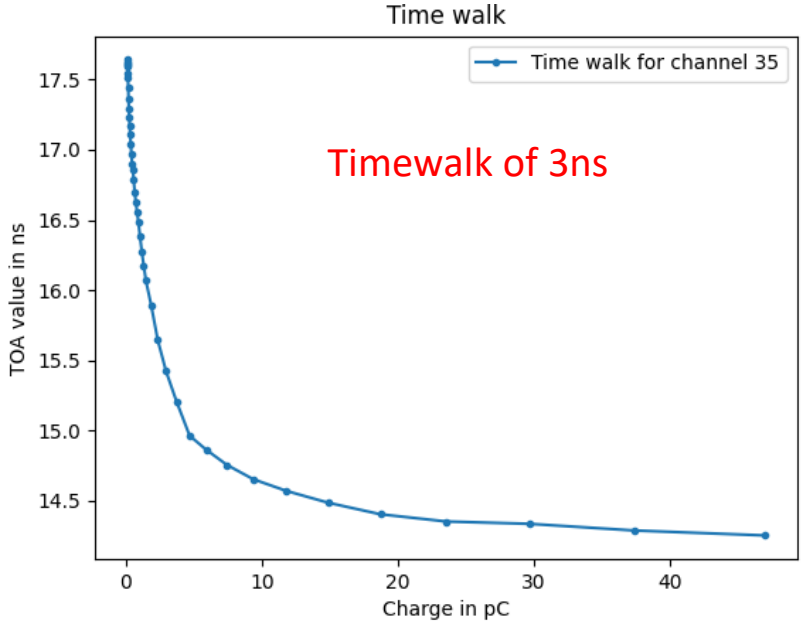
Timing measurements

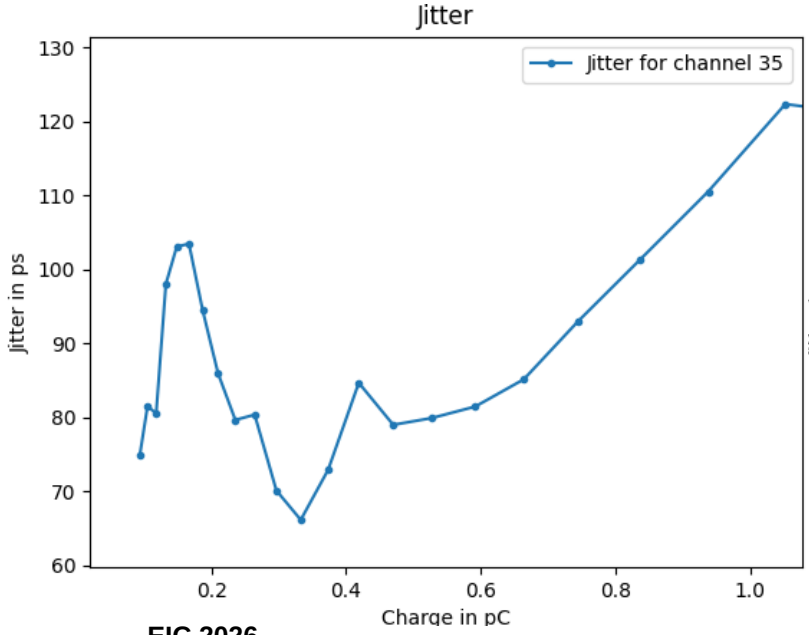
- External injection setup:
  - 2.2nF detector capacitance
  - 49pF injection capacitance

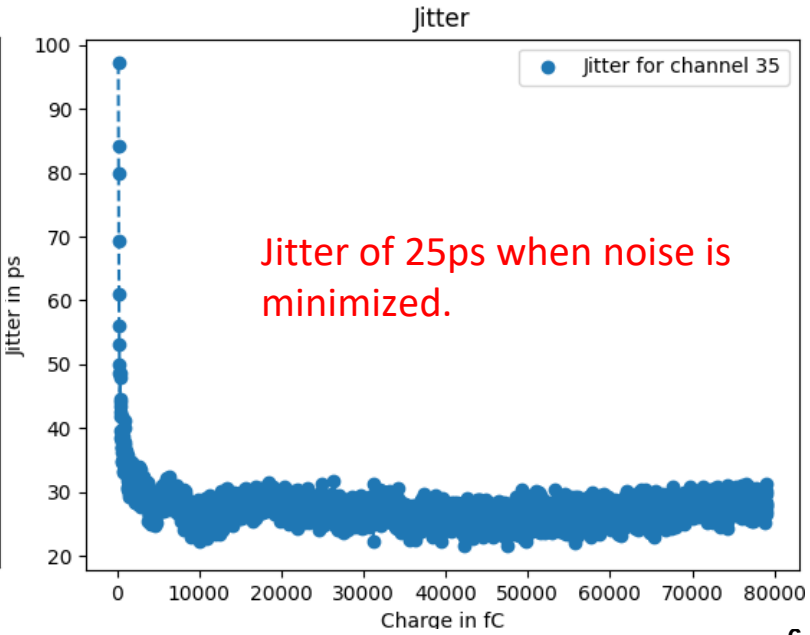
- External injection results:
  - TOA threshold at 180fC
  - 3ns Time walk
  - Jitter under 100ps for the MIP (432fC)
  - Jitter saturates at 125ps (it should saturate at 25ps)

- Regarding the jitter issue:
  - Jitter saturates at 5 times the expected value
  - The error was identified and reproduced in simulations
  - A fix has been proposed for CALOROC2
  - When reducing the noise of the preamplifier (by reducing the gain), the jitter saturates at 25ps. This shows that the TDC is working correctly and that the issue is slew-rate related.



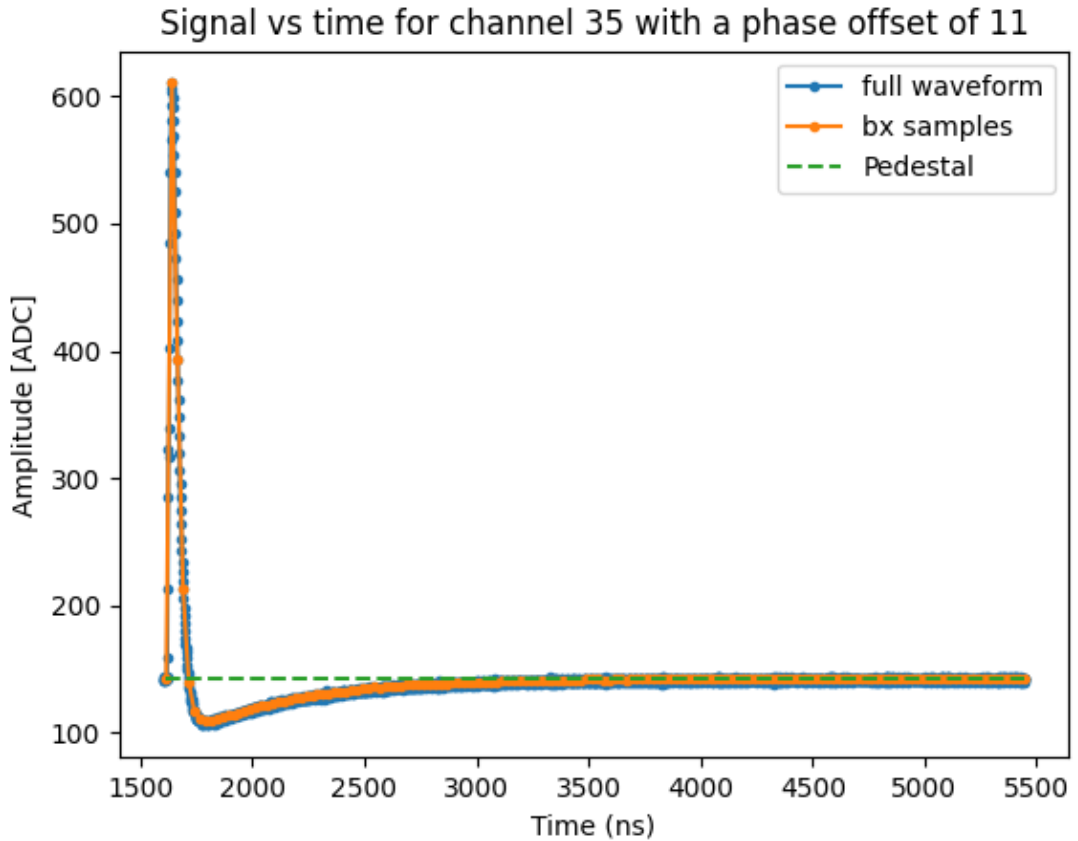


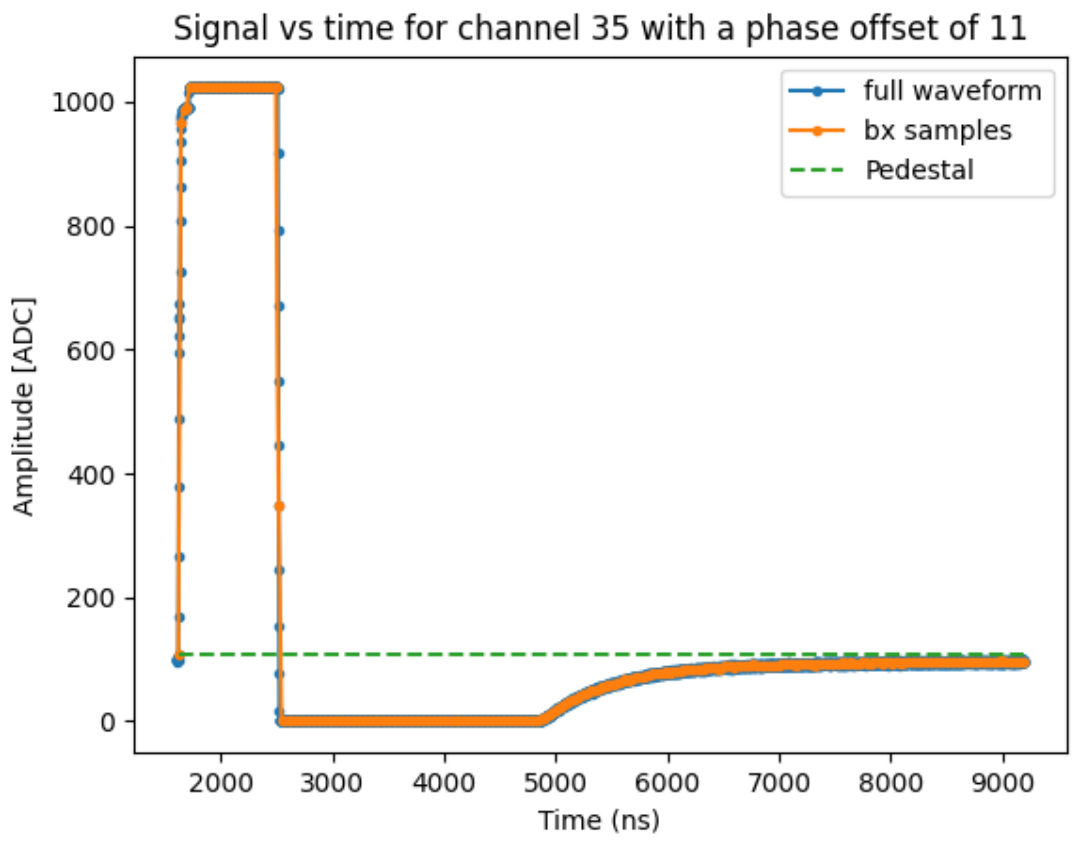




Time to baseline measurements

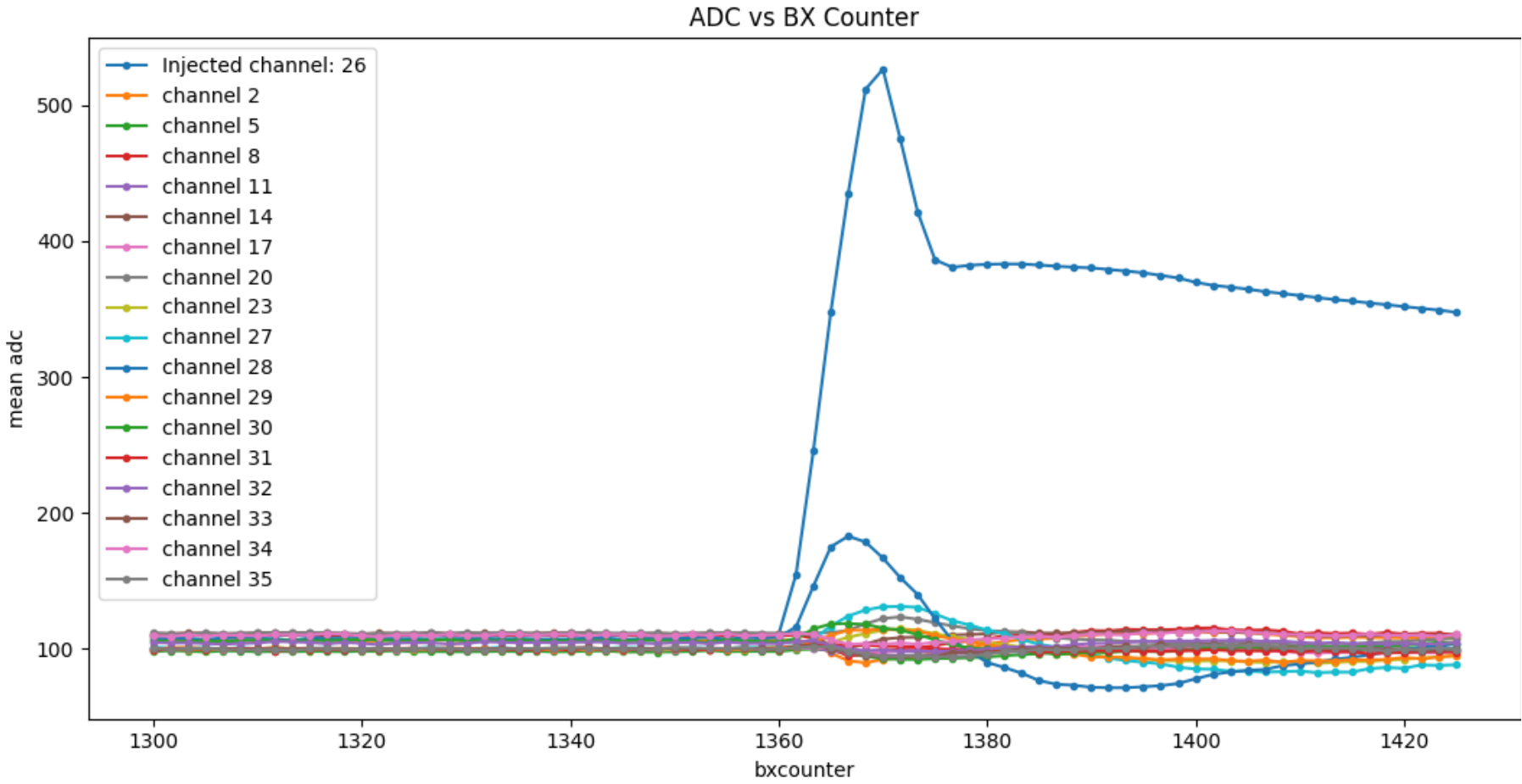
- Time to baseline is given by the time constant $\tau = R_{in}C_{det} = 500ns$
- Low charge inputs take up to $1\mu s$ to go back to the baseline due to the undershoot.
- For large signals over the dynamic range capabilities of the ASIC, the time to baseline can take up to $6\mu s$
- Remainder: Per channel hit rate is 100kHz ($10\mu s$)





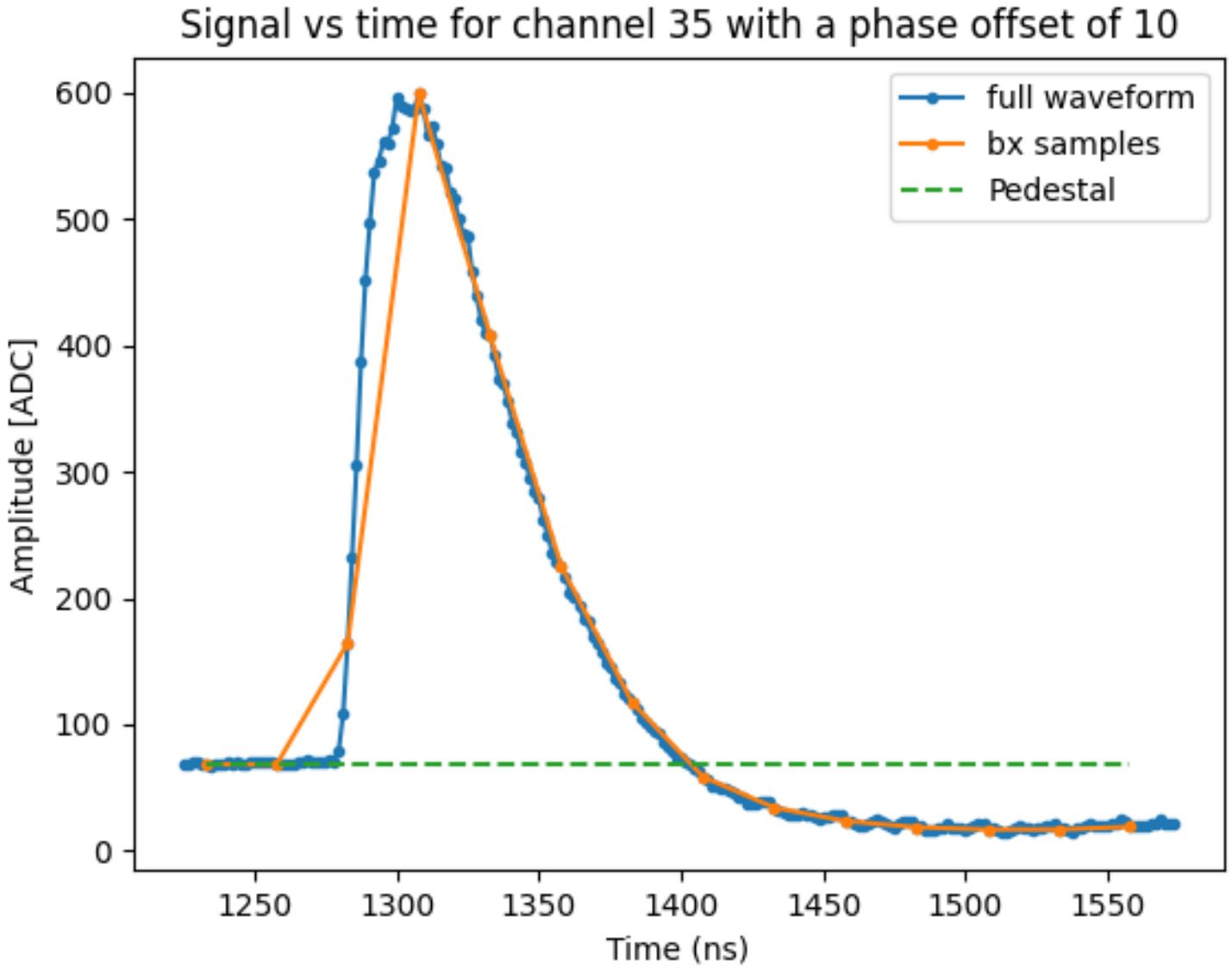
Crosstalk measurements

- Crosstalk measurements:
  - Max crosstalk was 0.3%
  - The highest crosstalk when injecting a charge in a channel X is seen in the X$\pm$2 channels.
  - This is due to a capacitive coupling in the substrate and PCB between those channels.
  - The channels with the second highest crosstalk are the channels: X$\pm$2 with a crosstalk of 0.12%
  - New PCB in development



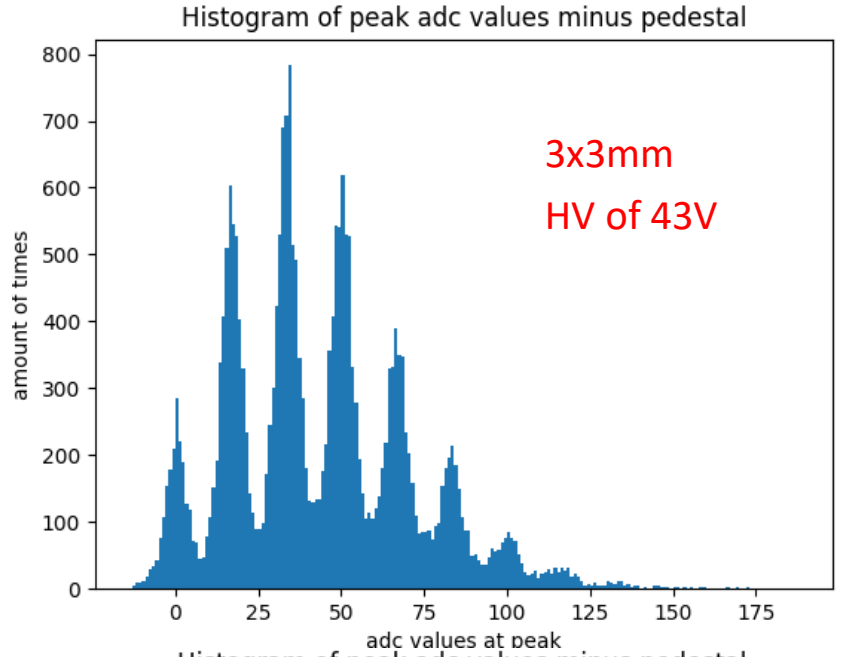
SiPM measurements

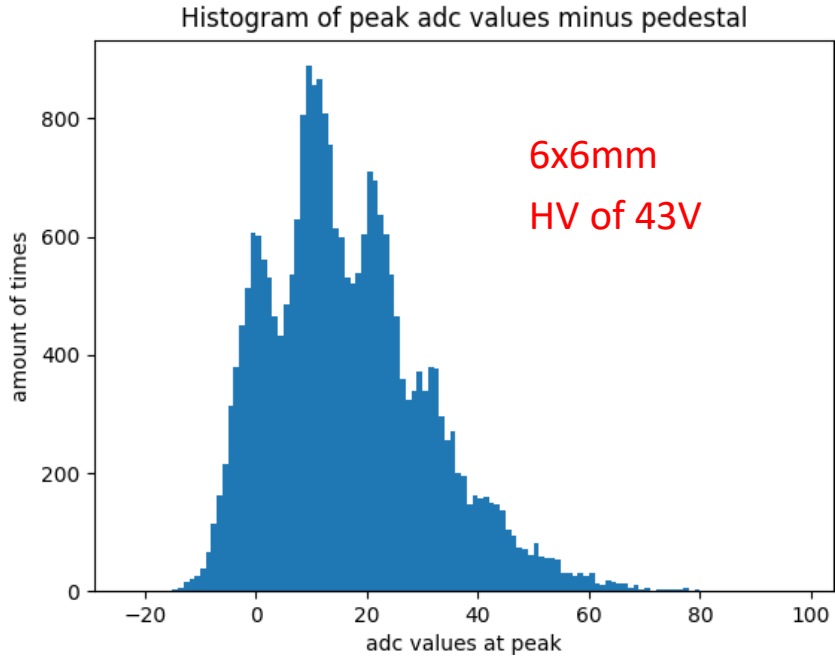
- SiPM setup:
  - 3x3mm and 6x6mm SiPMs used
  - SiPM nominal gain of $1.8 * 10^5$ for both SiPMs (30fC per p.e) at HV = 43V
  - Laser setup used to observe the single photo-electrons
- Waveform:
  - Waveform is in line with what was expected
  - Time to peak of 25ns
- Noise:
  - Noise is twice larger than expected
  - Detector doesn't receive a fixed amount of photons
  - Noise is dominated by the dark noise from the SiPM
  - Parasitic inductance can increase the noise, inductance should be minimized.

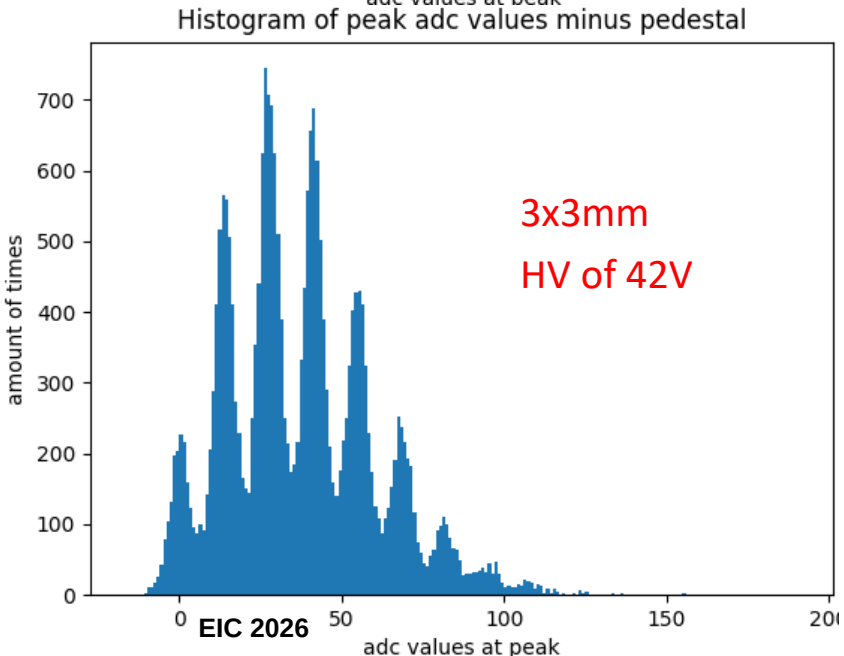


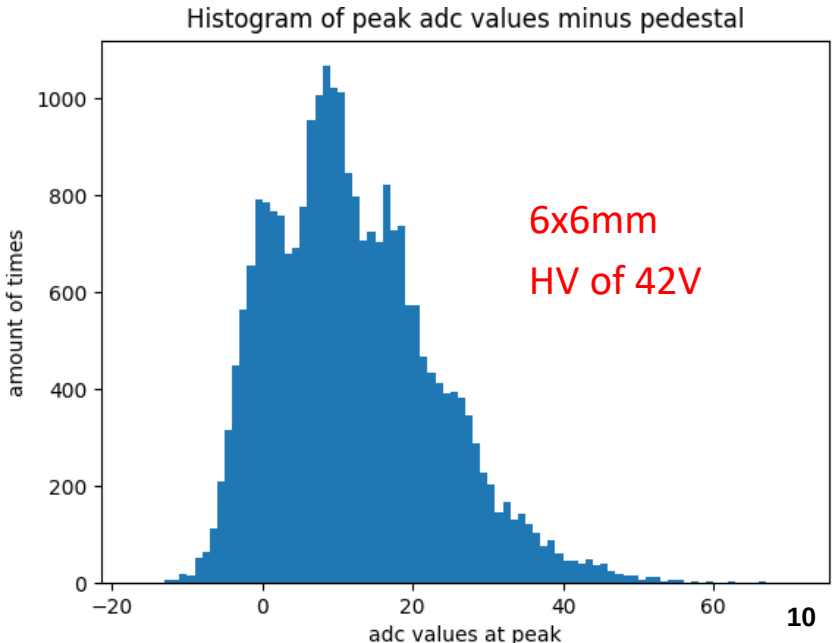
Single photo-electron measurements

- SiPM setup:
  - 3x3mm and 6x6mm SiPMs used
  - SiPM nominal gain of $1.8 * 10^5$ for both SiPMs (30fC per p.e) at HV = 43V
  - Laser setup used to observe the single photo-electrons
- 3x3mm SiPM results:
  - SNR is 4.9 at nominal HV
- 6x6mm SiPM results:
  - Dark noise is significantly higher and the signal is smaller
  - Single photo-electron is still distinguishable
  - SNR is 2.8 at nominal HV
- Dark noise:
  - Most of the dark noise can be filtered out by subtracting the pedestal



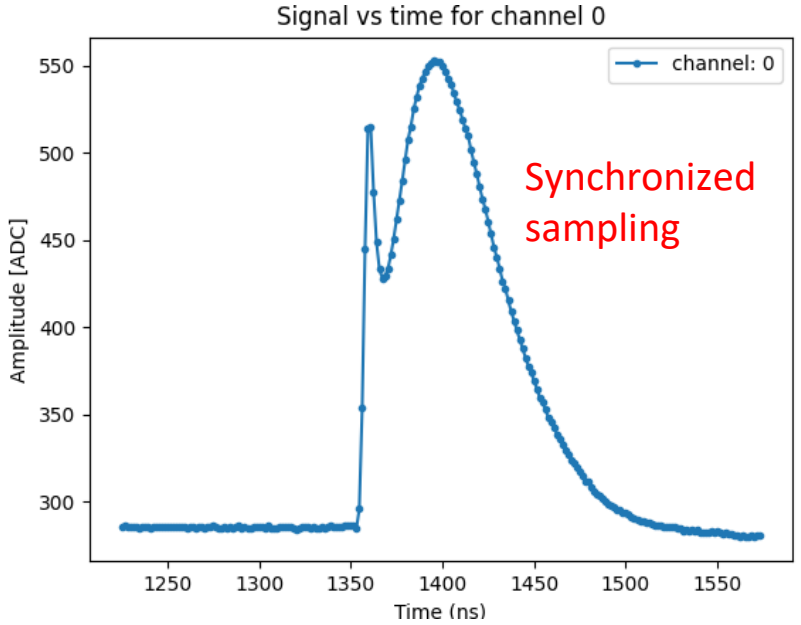


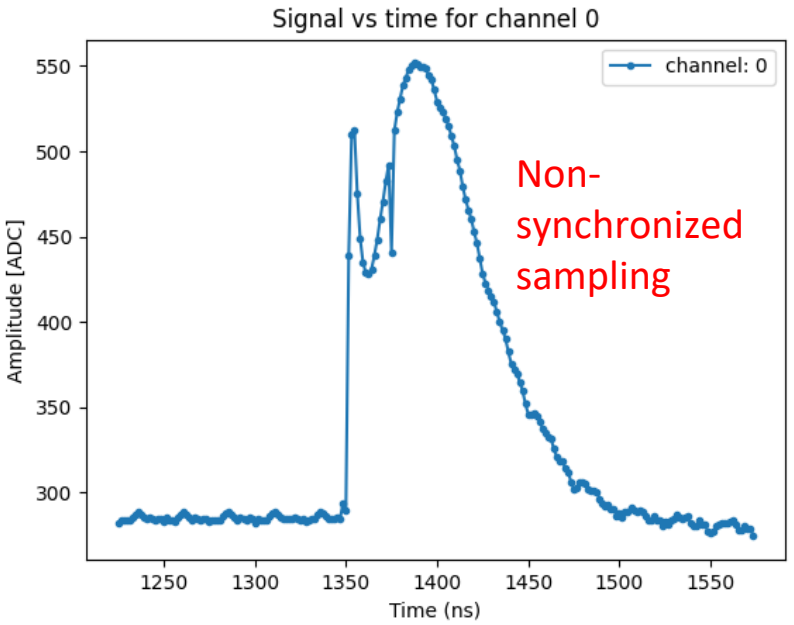


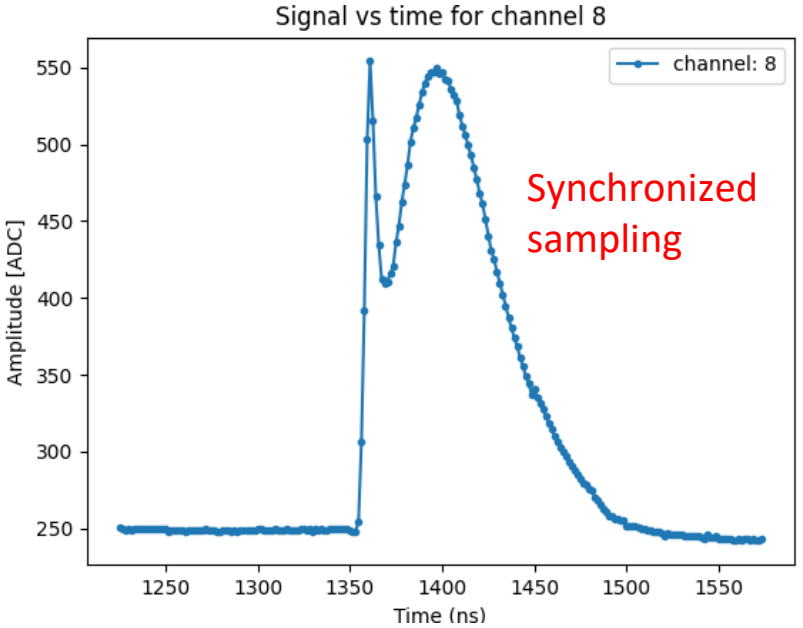


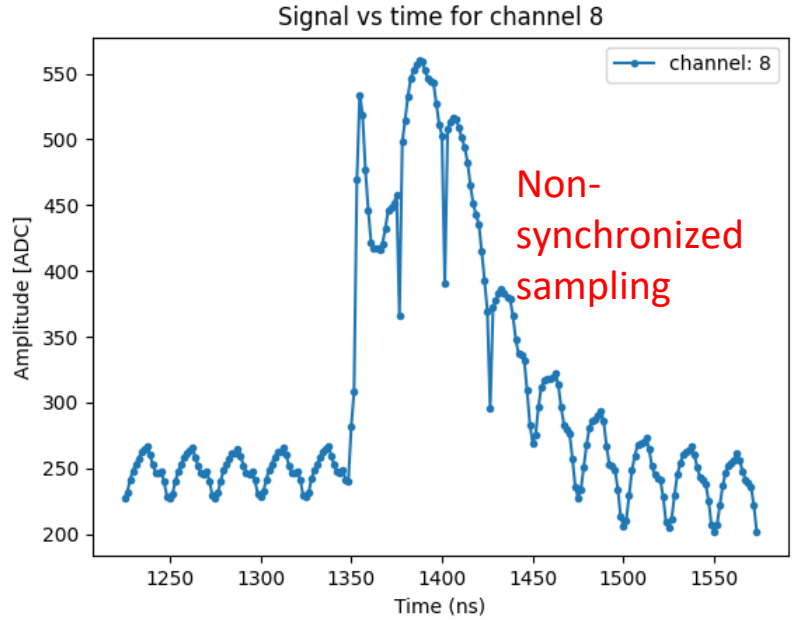
Current issues under study

- Setup:
  - Using the internal injection
- Large digital noise:
  - When doing a non-synchronized sampling, a large digital noise appears
  - The noise correlates strongly with the routing of the channels in the PCB (layer 6 has more noise due to being close to the digital power layer)
- Double peak at waveform:
  - Only when doing the internal injection
  - Issue related the parasitic inductance between the channel and the detector capacitance.
- The issue is understood and related to the PCB, a new PCB is under development to solve this issue
- FEB design should consider:
  - Channels should be routed between gnd layers to avoid digital coupling
  - Inductance should be minimized









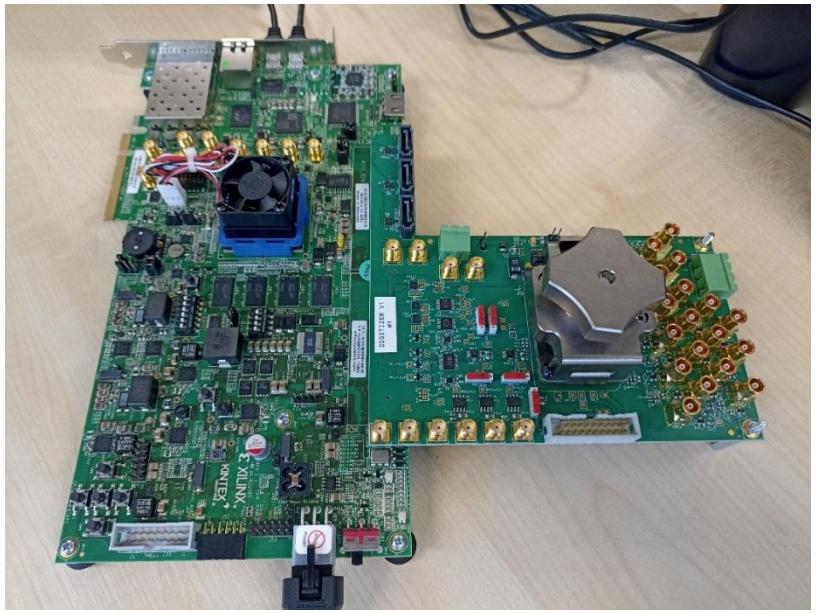
Summary and next steps

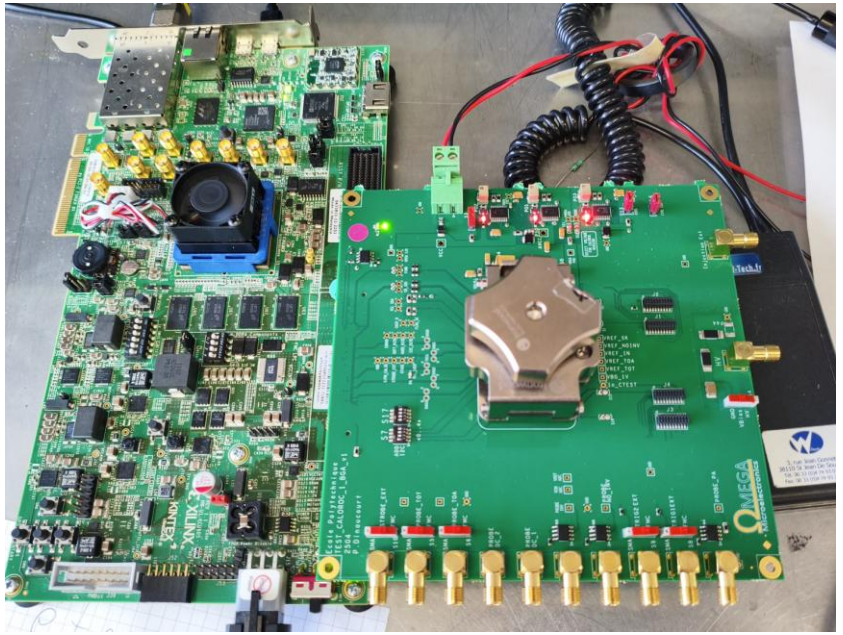
- CALOROC-A analog measurements underway, first results similar to H2GCROC

- CALOROC-B first measurements are encouraging:
  - Dynamic range of 200fC up to 1.5nC using a 2.2nF detector
  - Jitter under 125ps for all samples with a trigger efficiency of 1 (the origin of this error was identified and should be corrected for CALOROC2B)
  - SNR of 5 using a 3x3mm SiPM and 3 using a 6x6mm SiPM, both with a gain of 30fC per photon

- Possible actions for investigation
  - New PCB in development, schematic already finished
  - FEB crosschecks
  - Zero suppress measurements and 39.4MHz tests

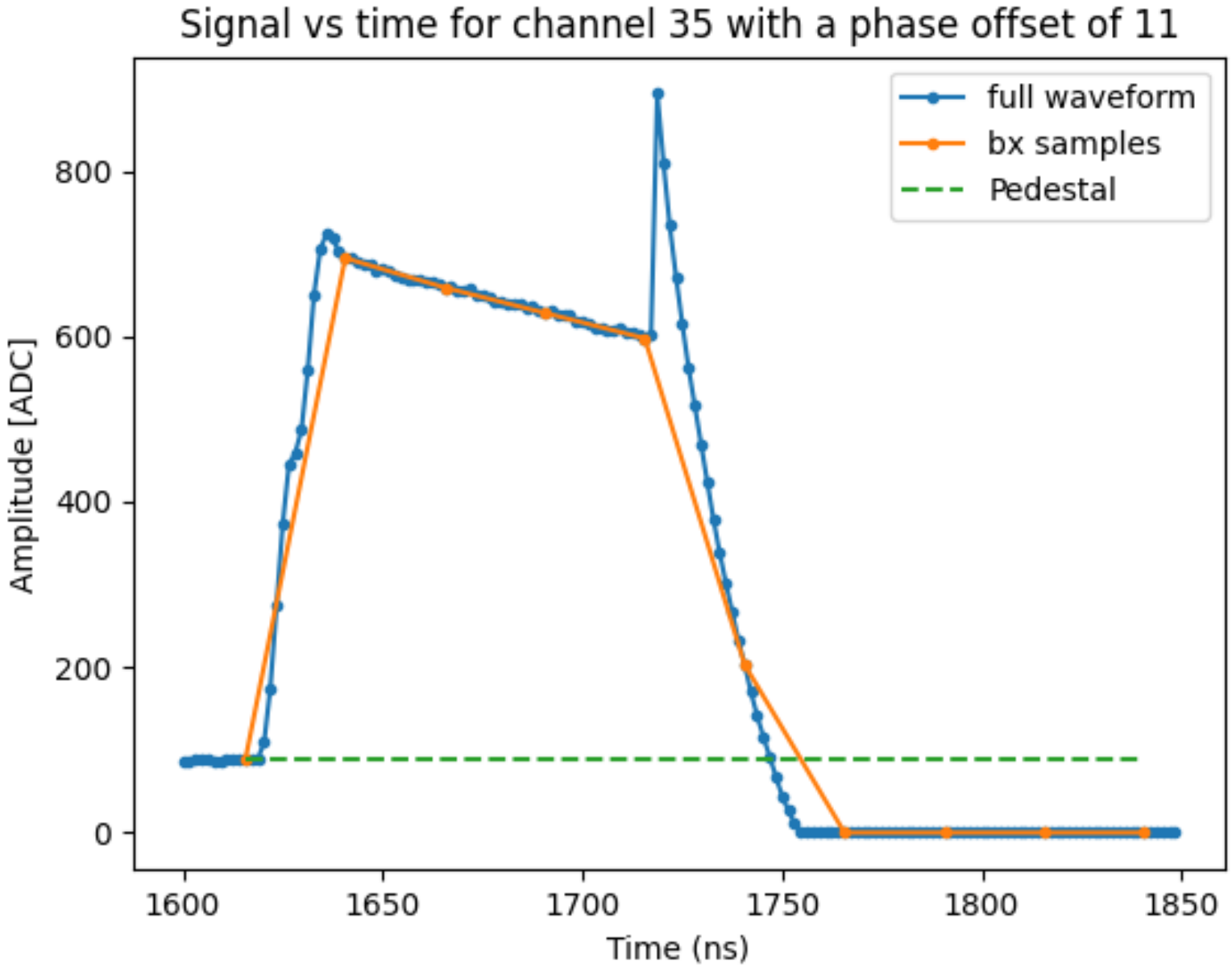
- CALOROC2 timeline (next presentation)
  - If TSMC130nm is available in March 2027
  - Otherwise there would be a 12 to 18 month delay due to the migration to a new technology



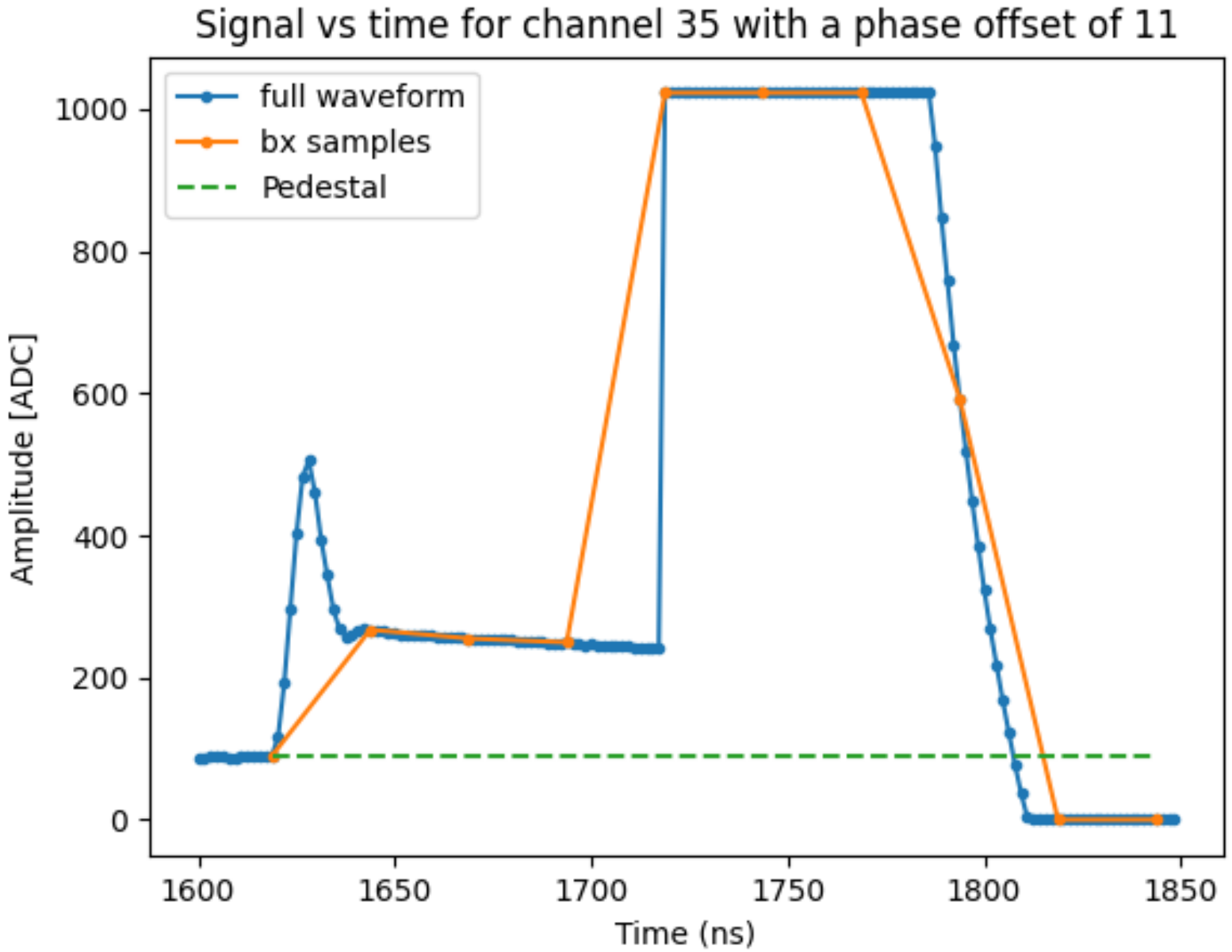


Backup

First gain switching waveform

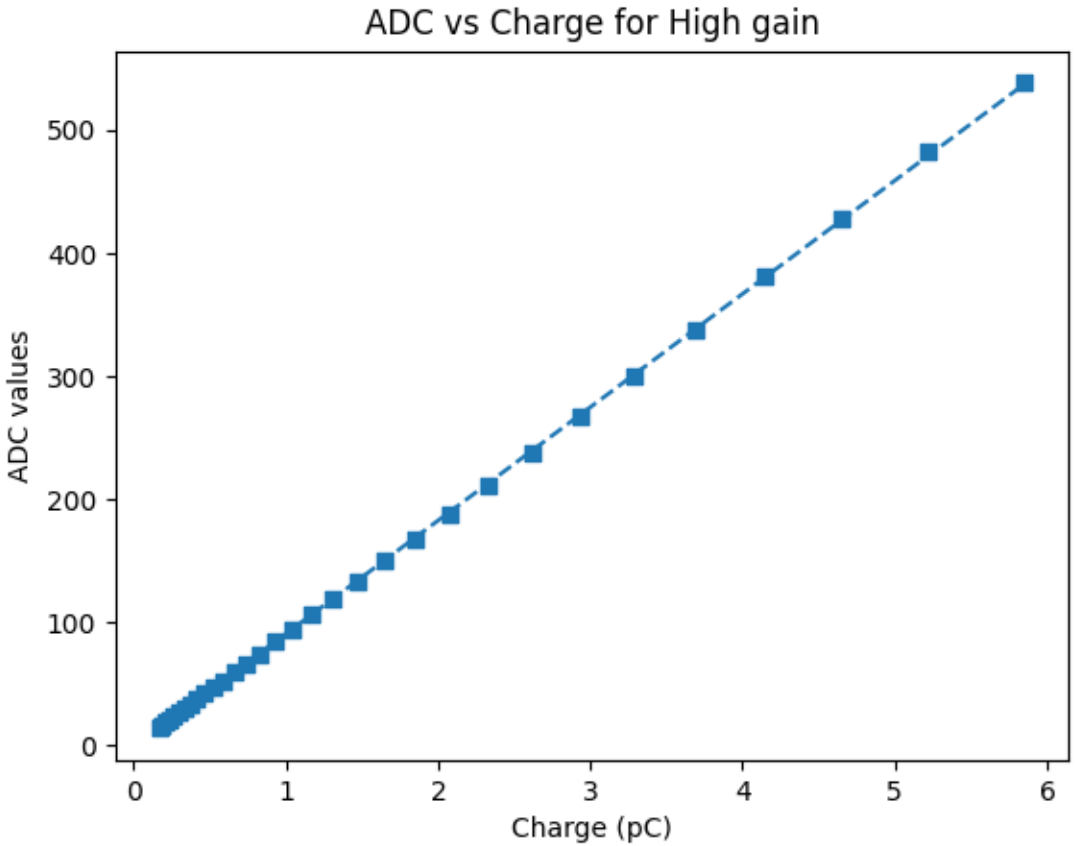


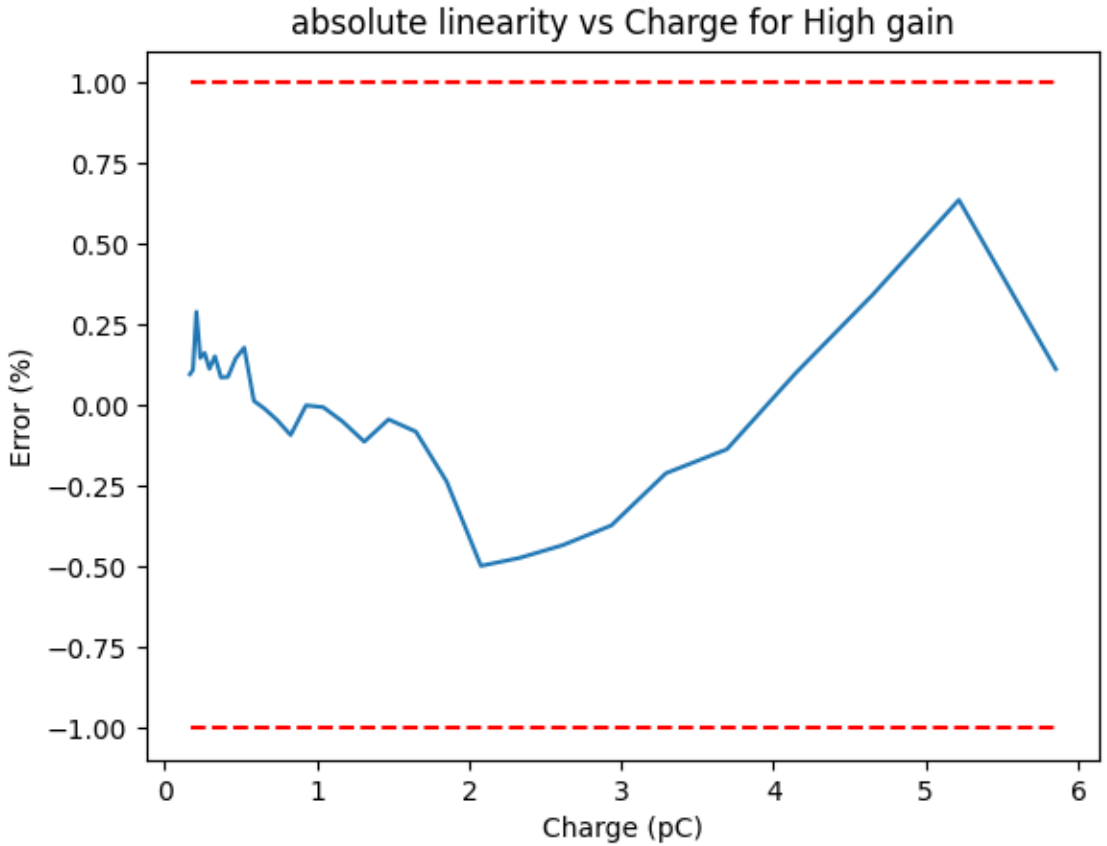
Second gain switching waveform



Absolute linearity for the high gain second point

We tested the linearity of the second point of the high gain waveform (after the peak) to see if the linearity is consistent for all the points of the waveform.

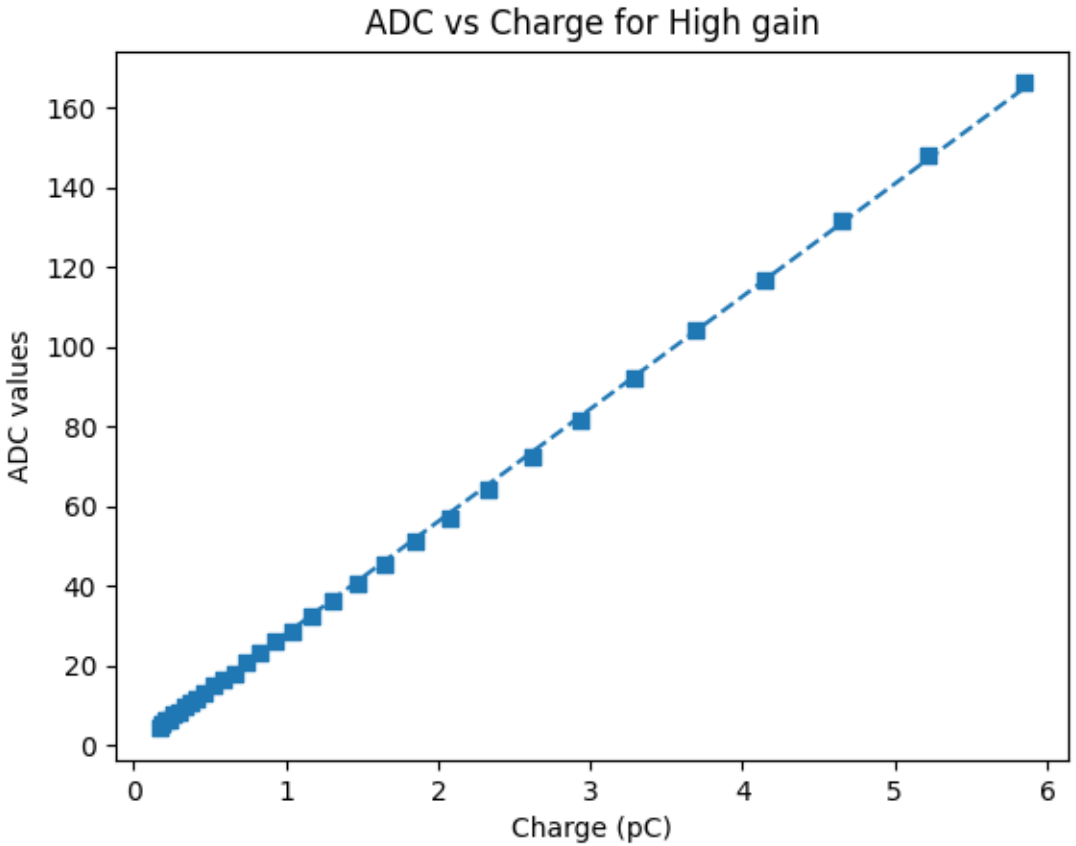


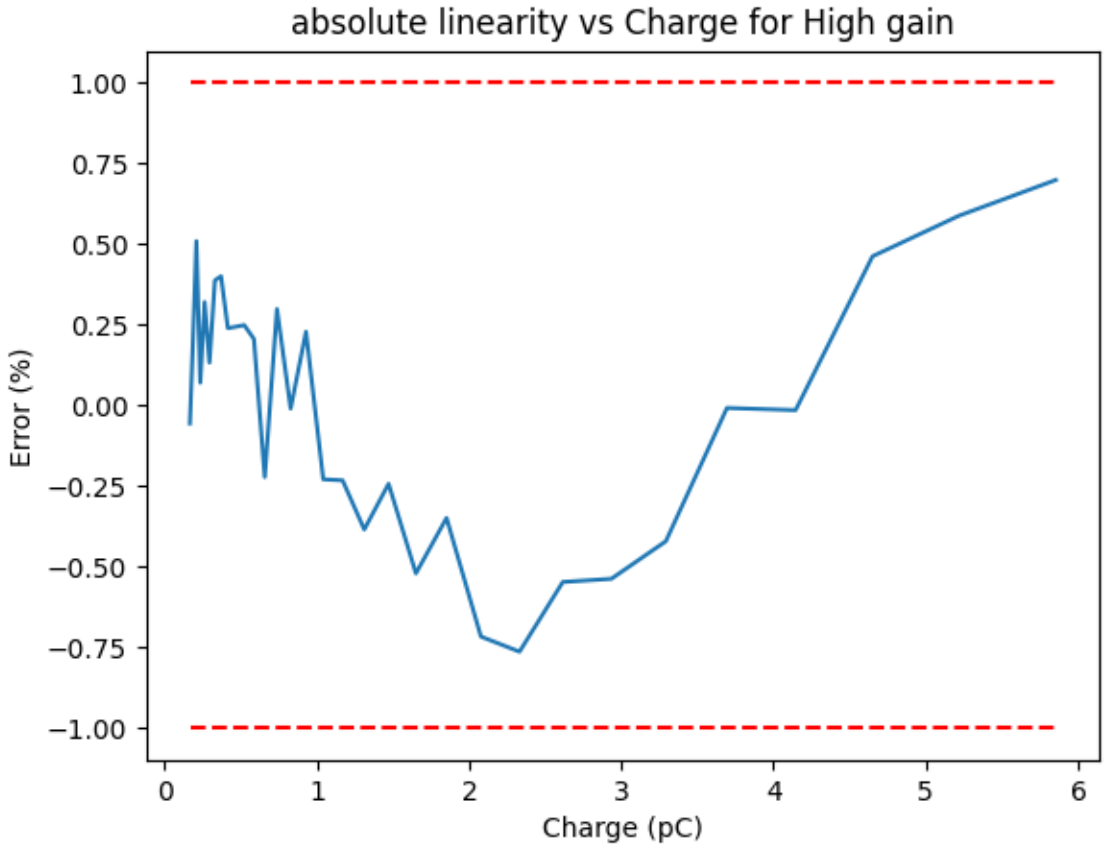


Amplitude is lower and nonlinearities are slightly higher, yet well within the requirements

Absolute linearity for the high gain third point

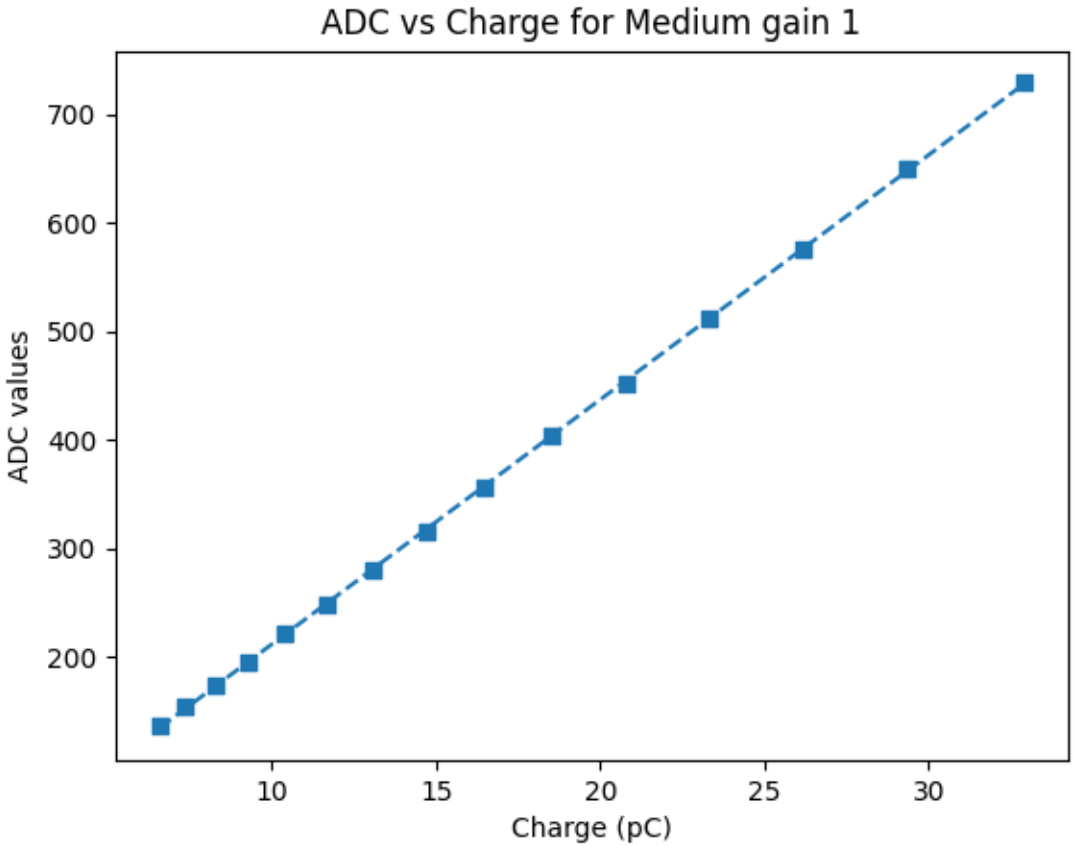
Amplitude is even lower, yet we still keep a good linearity

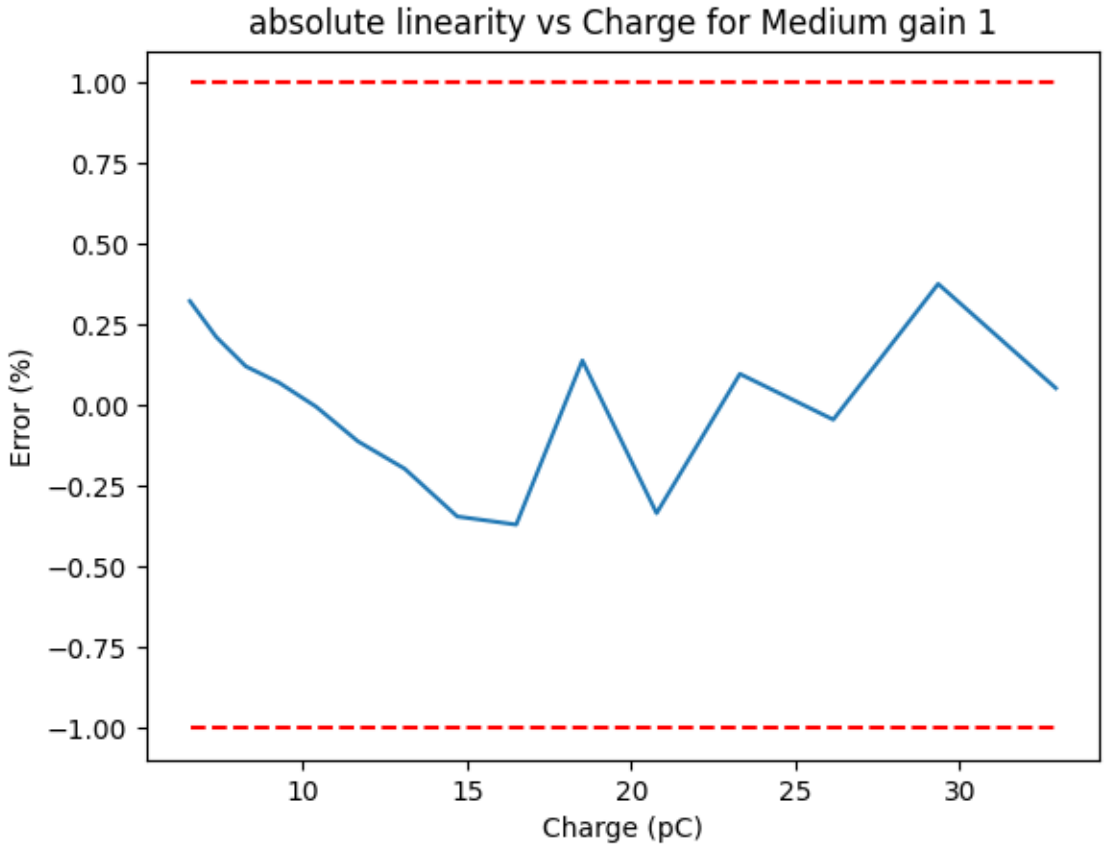




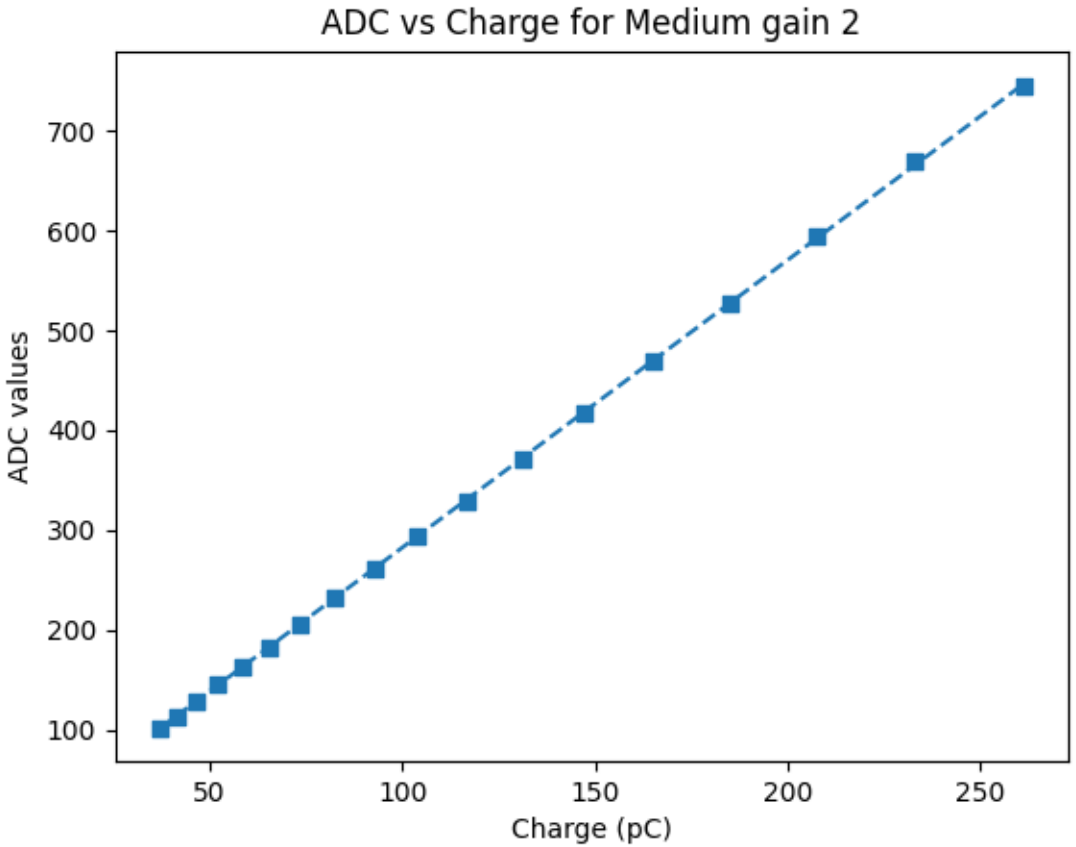
Absolute linearity for the Medium gain 1 third point

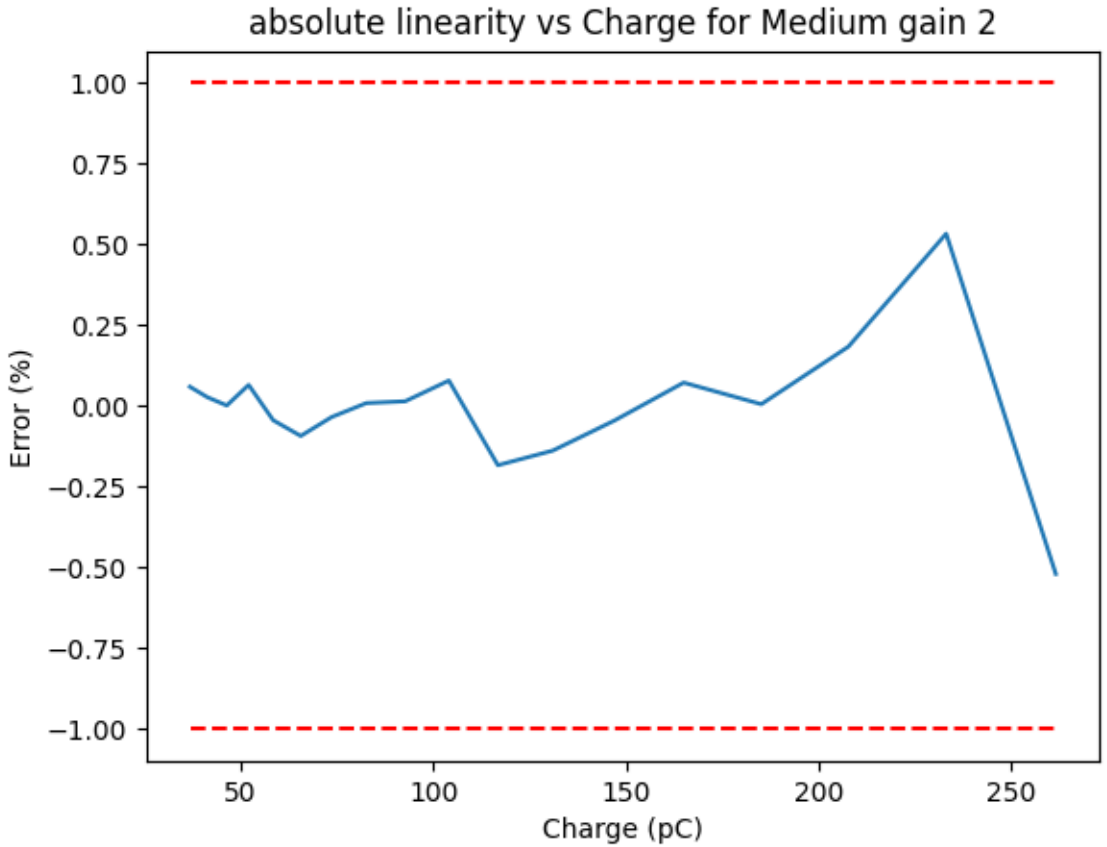
We did the same tests for the medium gain 1, 2 and low gain



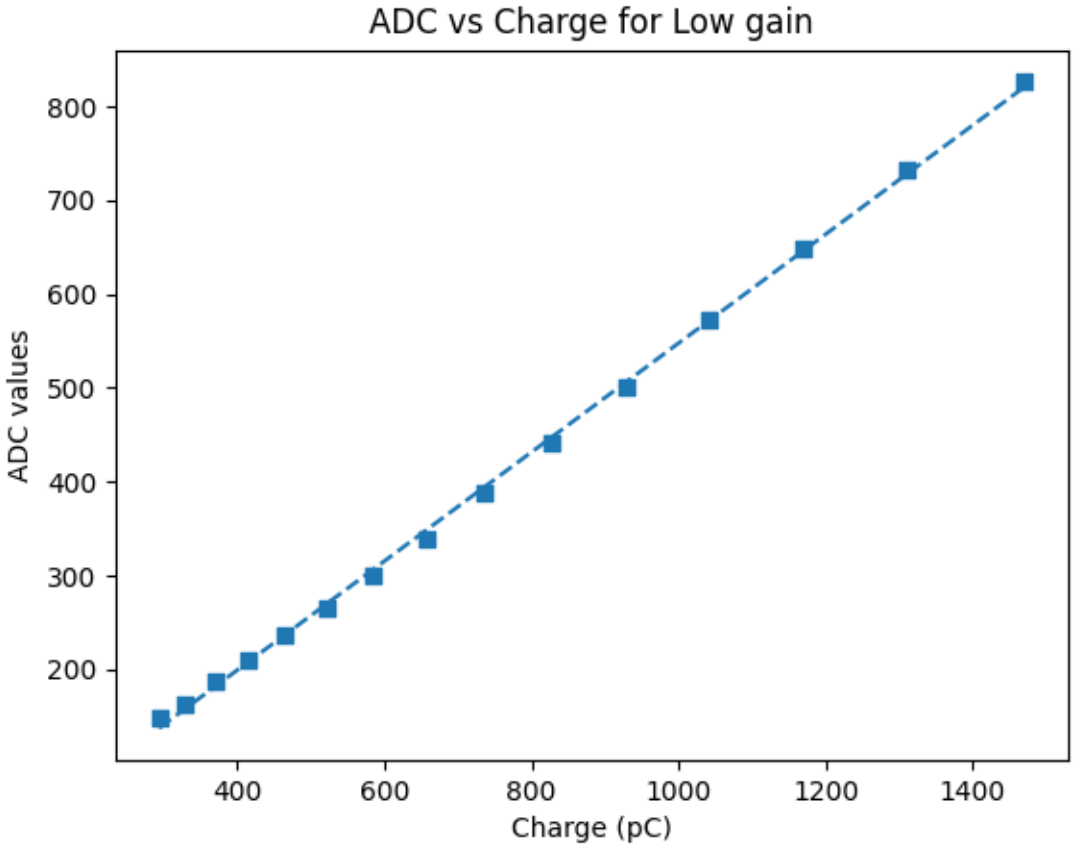


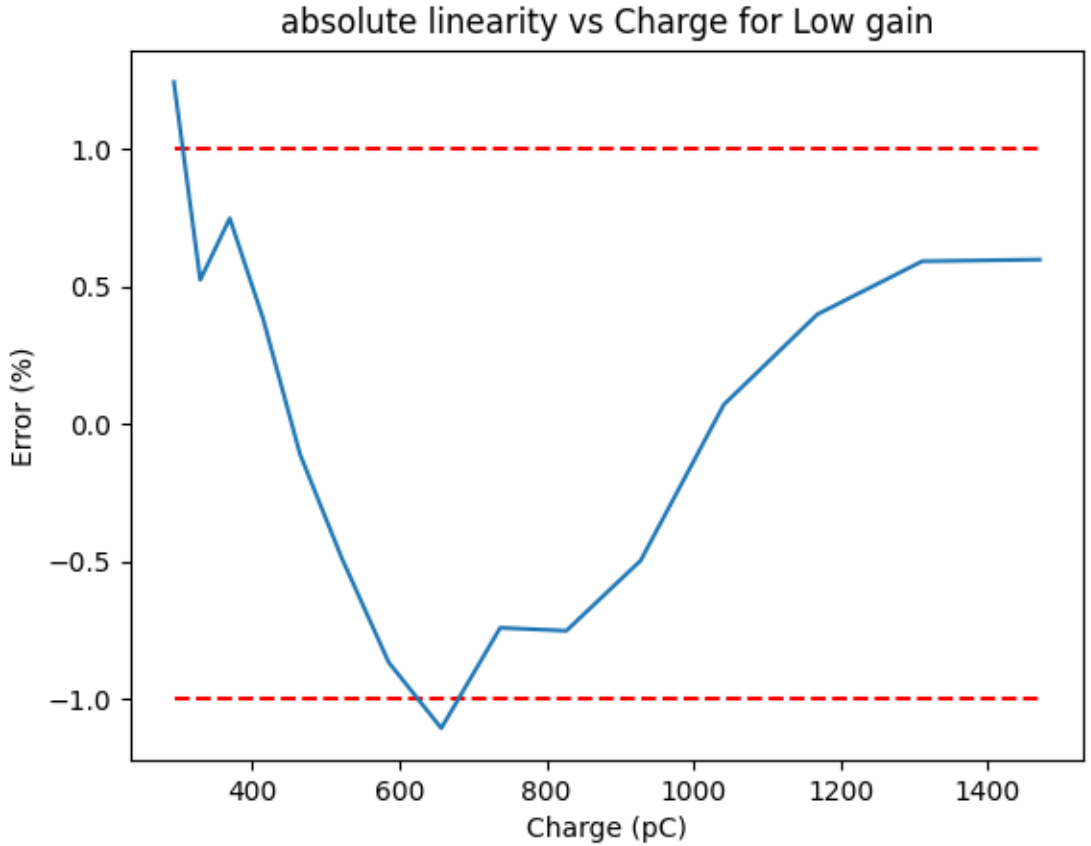
Absolute linearity for the Medium gain 2 third point





Absolute linearity for the Low gain third point



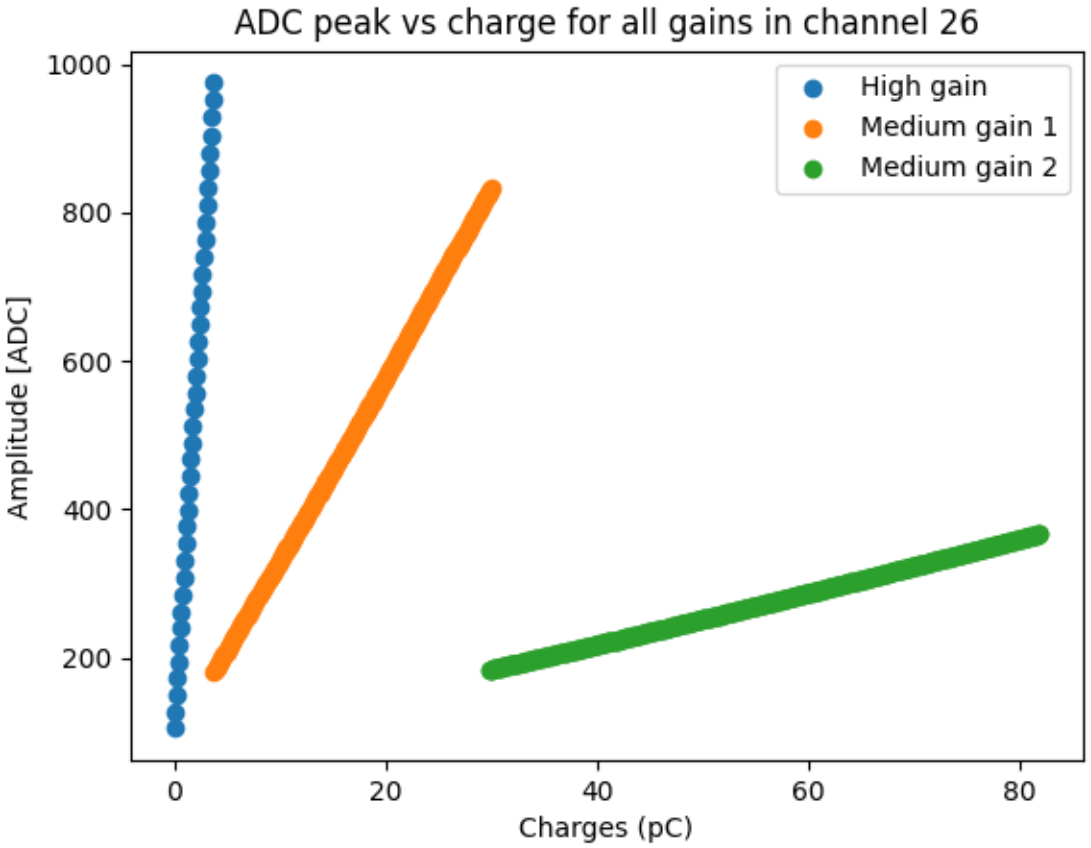


2ADC mode

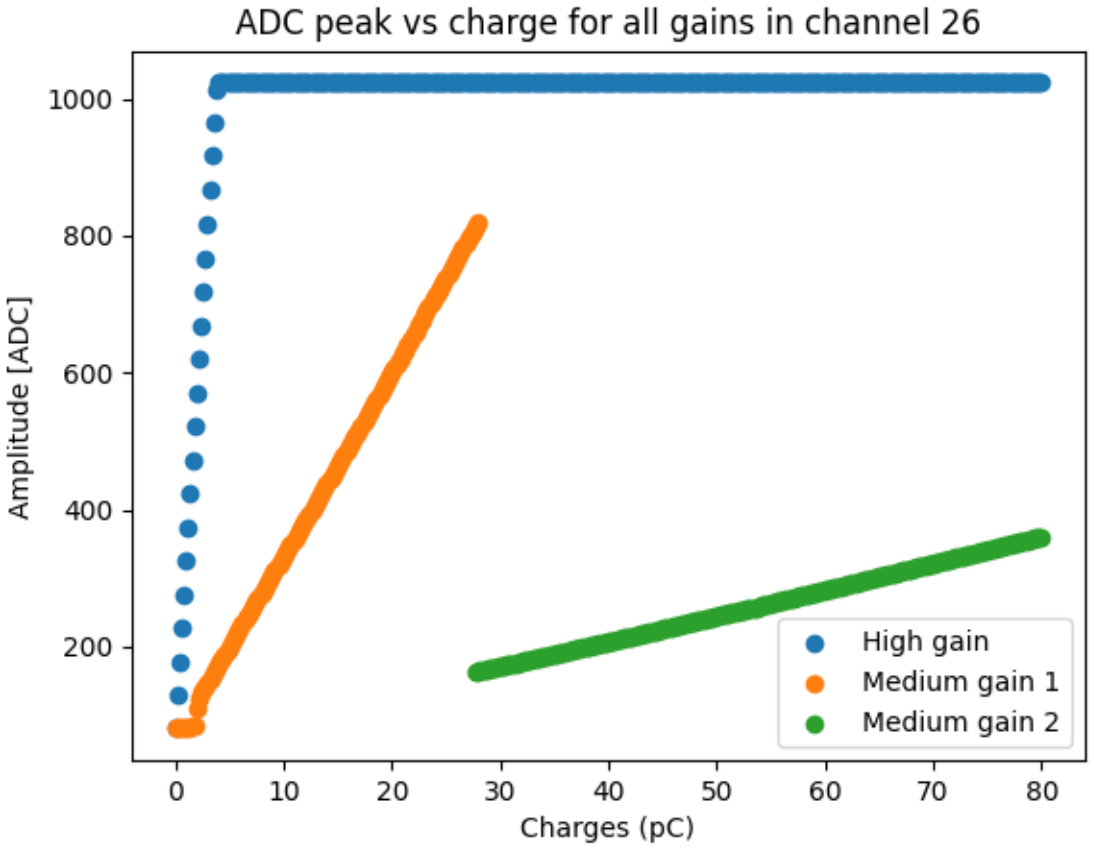
Using the 2ADC mode with the first ADC set to HG and the second ADC set to the gain switching we obtain similar results with the addition of an overlap for low charges.

For low charges the second ADC show some nonlinearities, which is expected due to the resistance switching.

1ADC mode

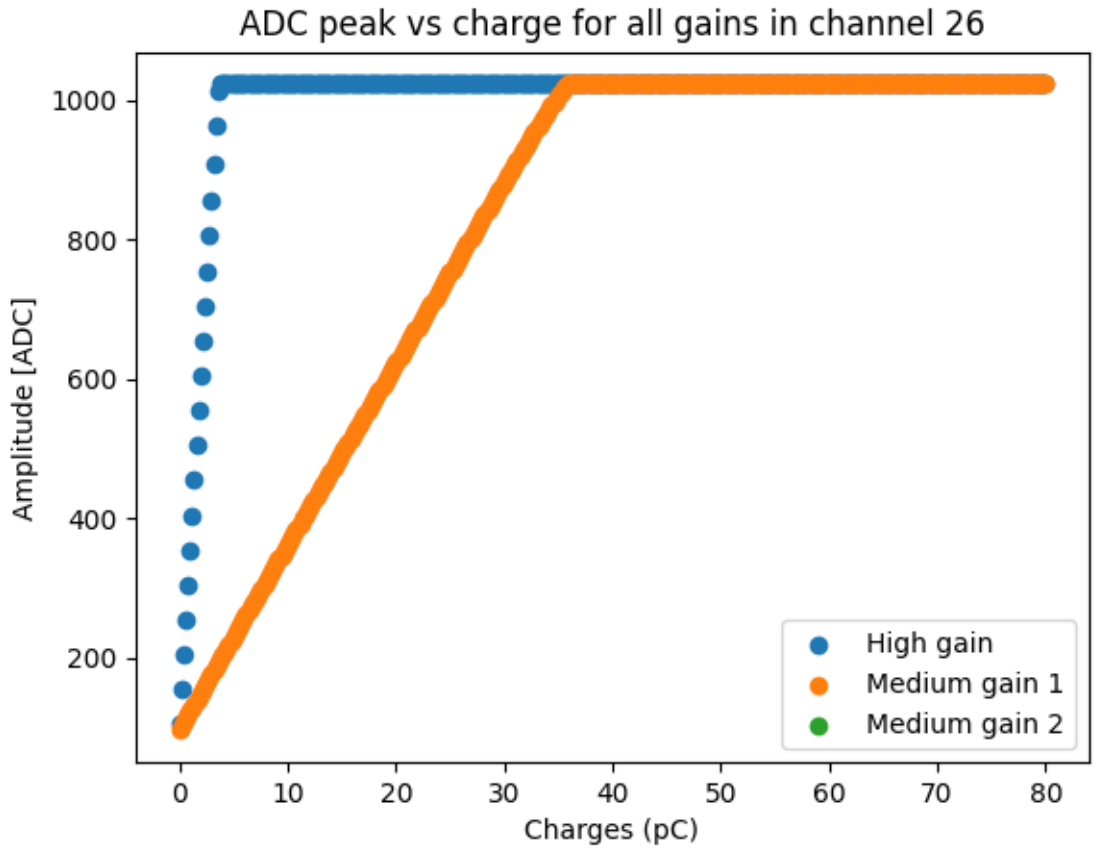


2ADC mode



2ADC mode without gain switching

The “no gain switching” mode was tested, we keep a good linearity although the dynamic range is quite limited.



Short term plans regarding the technology issue

- Prepare CALOROC2 in TSMC 130nm (just in case)
  - If TSMC 130nm is still available we will have a CALOROC2 prepared for submission by march 2027

- UMC 110nm:
  - NDA was signed in preparation for a possible technology shift
  - If UMC 110nm is chosen we expect an 18 month delay
  - Rad hard only up to 1 Mrad

- TSMC 65nm:
  - PDK already available
  - All programs installed for being able to start working using the 65nm
  - If TSMC 65nm is chosen we expect a 12 month delay
  - Price is 2.5 times more expensive
  - We may risk having the same issues as with TSMC 130nm