Generic RDO Status

ePIC/EICUG Meeting

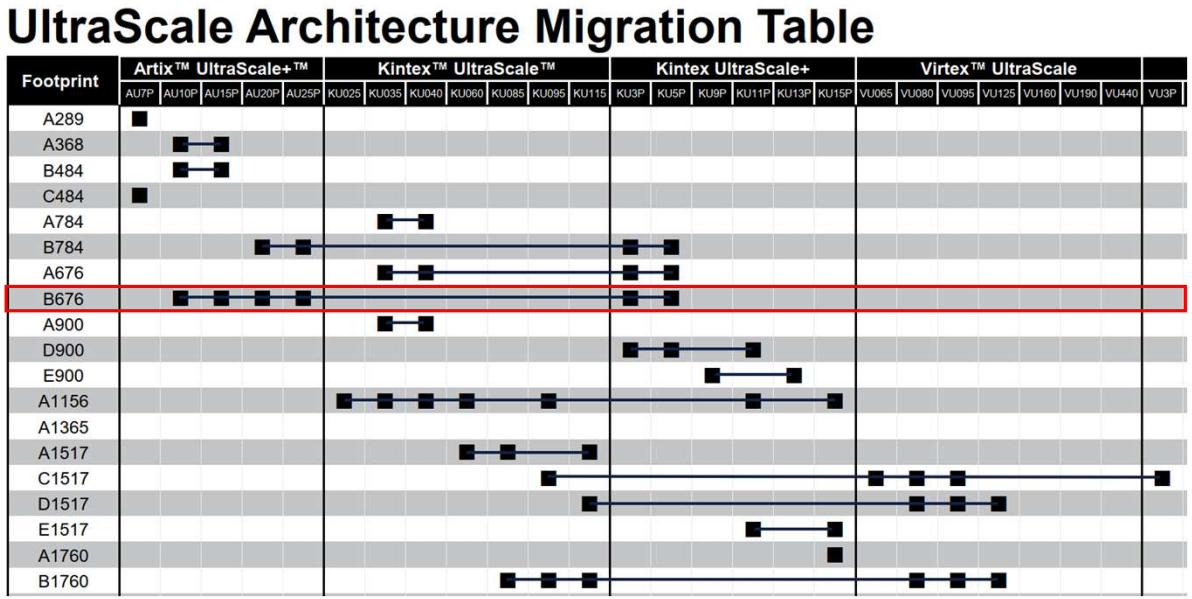
Short overview

- The original cencept: to design a reusable FPGA module that is scalable, easy to maintain, and replaceable
- The selected FPGA family is from AMD (or aka Xilinx) – UltraScale+ Aritx / Kintex, 16nm

Criteria:

- Relatively well-priced FPGAs
- Long-term availability is critical (2045*)
- The scalability is also very important factor
- Support CERN specific signals - CLPS (xROC), 10G (LPGBT, VTRX)
- Keep in house the design and the manufacturing possibility

*https://www.amd.com/en/products/adaptive-socs-and-fpgas/fpga/artix-ultrascale-plus.html

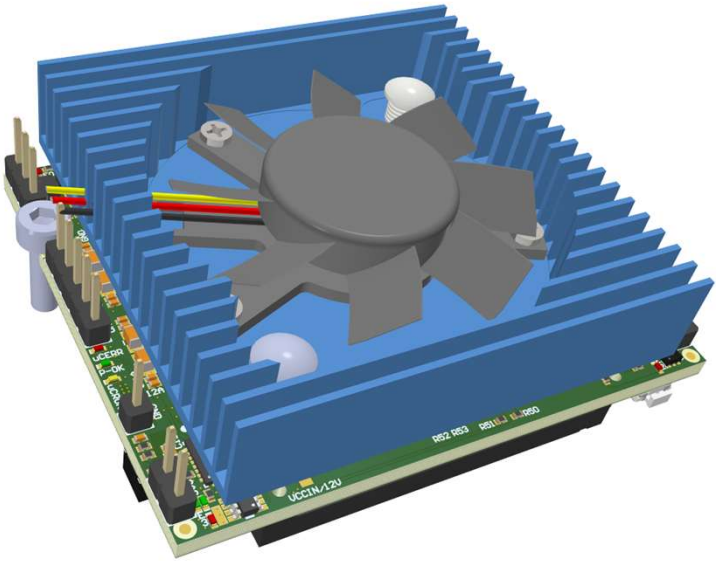


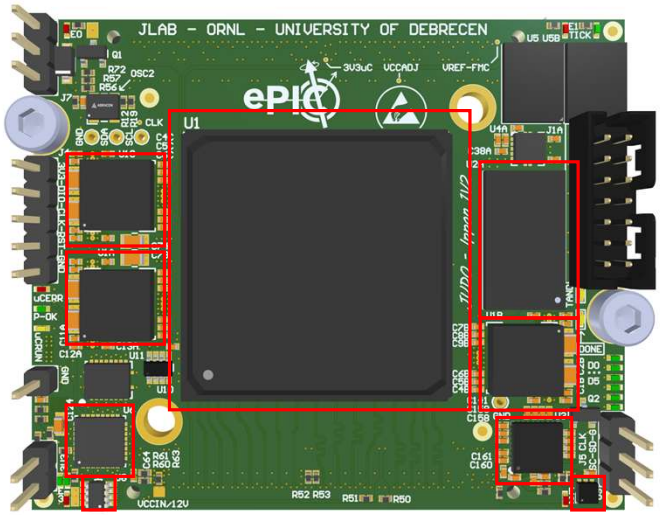
The planned module - Daughter board (DB)

- Based on these criteria, we need to talk two parts:
  - A relatively small daughter board (DB)
  - And a motherboard(MB) that depends on the application

→Based on previous discussions, the largest Artix (XCAU25P) and the second-largest Kintex (XCKU5P) would be the selected FPGAs. But that could still change...

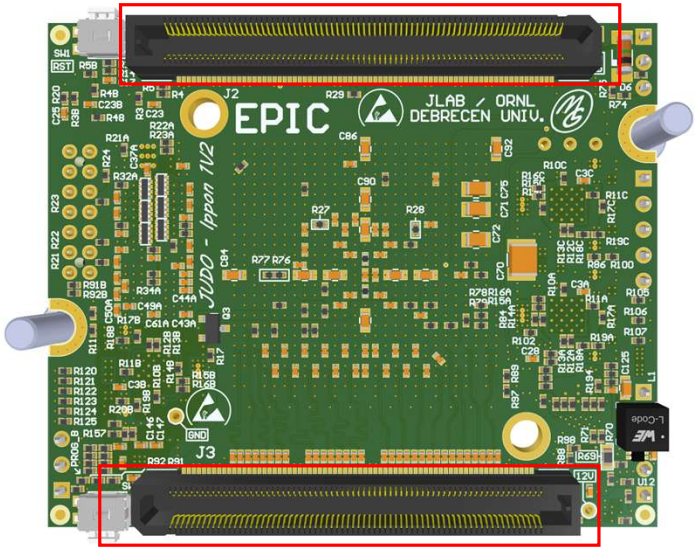
→The module size is: 60.5 x 50 mm





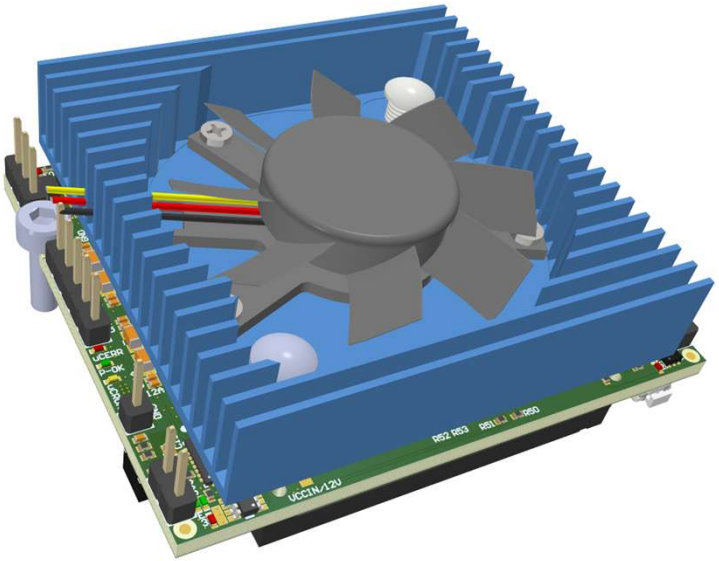
Components

FPGA
Power supplies
System monitoring / Sensors
Clock distribution
Memory
Expansion connectors

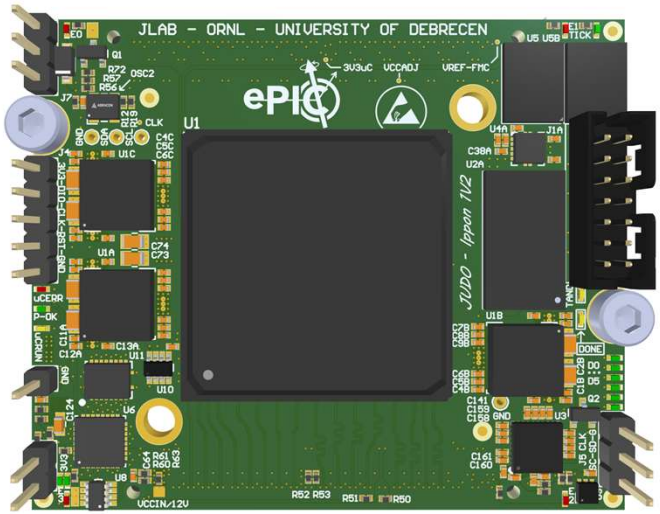


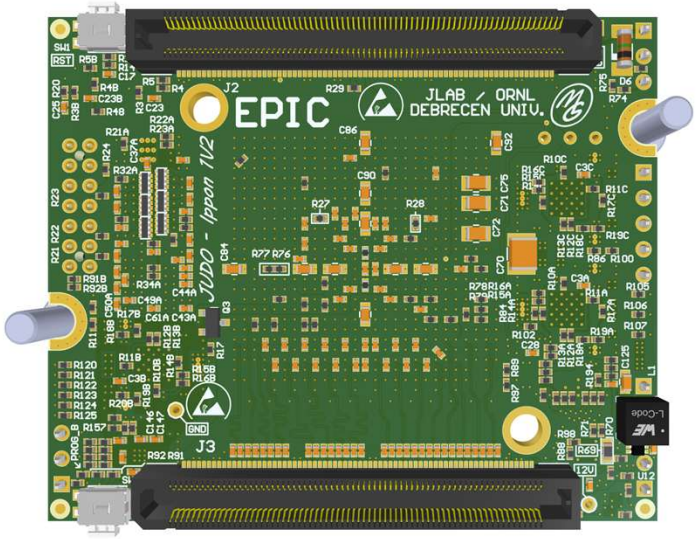
The planned module - Daughter board (DB)

- Aggregation is necesarry in many places



- In case of ***XCAU25P 12 GTY*** *are available (Max. 16.3Gbps)**
- In case of ***XCKU5P 16 GTY*** *are available (Max. 32.75Gbps)**

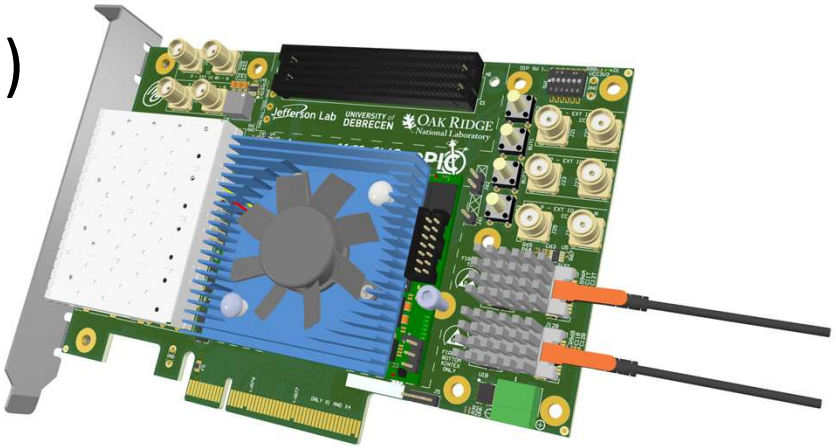


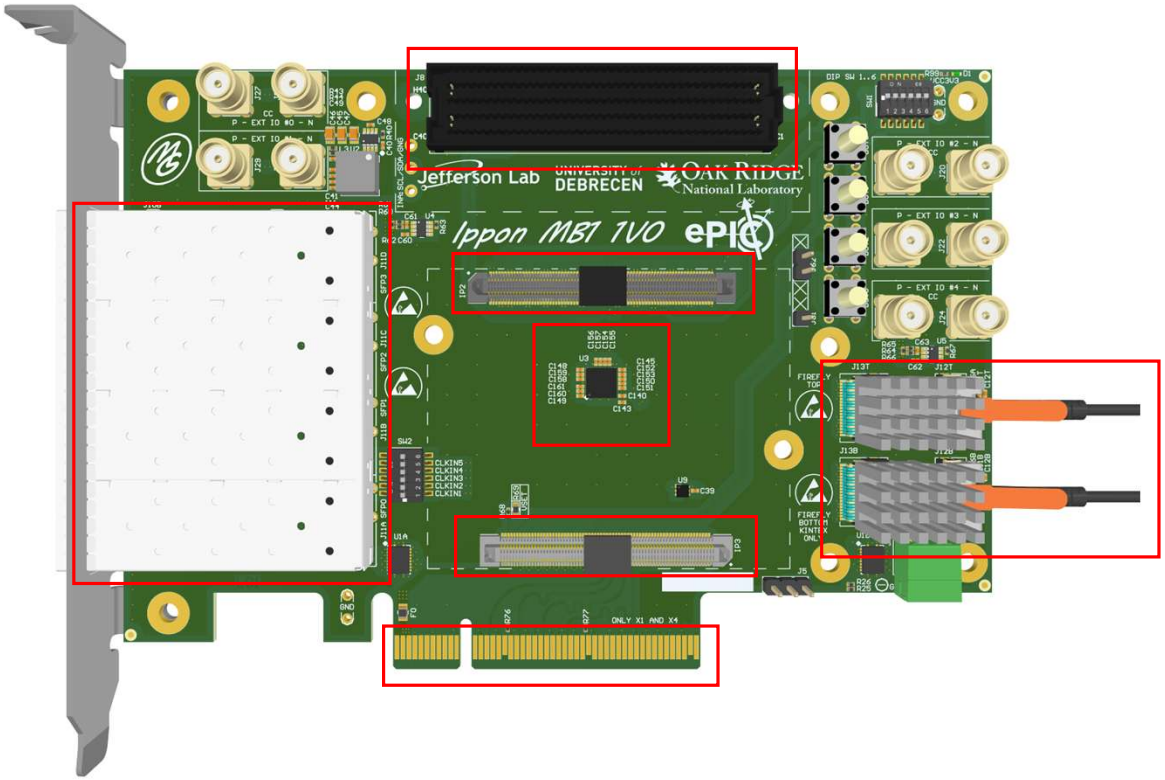


* https://docs.amd.com/api/khub/documents/Fz8MLna3N2KIo_xWN_Iv3w/content

The planned module – Motherboard (MB)

- Based on these criteria, we need to talk two parts:
  - A relatively small daughter board (DB)
  - And a motherboard(MB) that depends on the application





Components

Expansion connectors - FPGA
Expansion connectors – FMC
SFP+
FIREFLY
PCIe x4
Clock distribution

This MB is designed specially for testing the DB
(And replace the KCU-105)

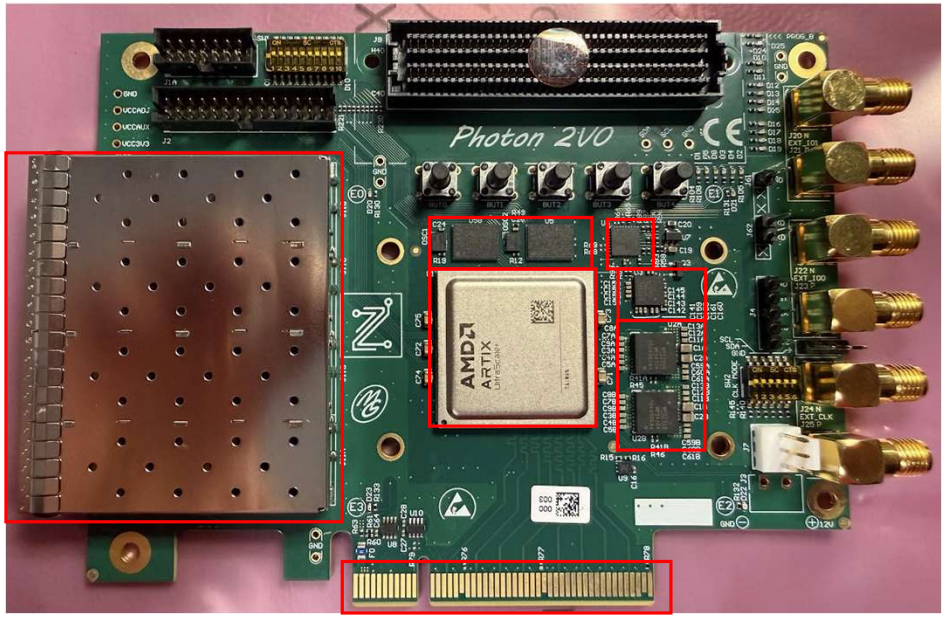
When are we now?

- The designs - containing simulations also - are ready
  - FPGA translation / IP-s
  - High speed signaling with HyperLynx
  - StackUp planning and optimalization with PCB manufacturers

- We have already tested the main components and circuit structures on another panel
  - DCDC converters
  - Clock distribution
  - FPGA Boot
  - System monitoring / controlling
  - 10G SFP+
  - PCIe

- Both boards – DB / MB – are in 99% ready for production

- Production of the first prototypes could begin any time
- No unresolved technical issues, only administrative issues left



When are we now? – Production (DB, MB)

- Discussions regarding production have concluded (Stackup, Component sources, Panelization)
- Production takes 4–6 weeks

- Steps:
  - First round will be populated only some boards (4-6) with a smaller / cheaper FPGA (*XCAU10P or XCAU15P*)

  - In the second step, we will manufacture several panels, using the final FPGA parts. This will be available for testing.

  - **Please let us know if you would like to participate in the testing!** (A few people have already done so)

  - The start of production has been delayed due to administrative and financial reasons.

  - If everything goes well, the samples will be available in 10-12 weeks (Of course, starting from the time the order is placed)

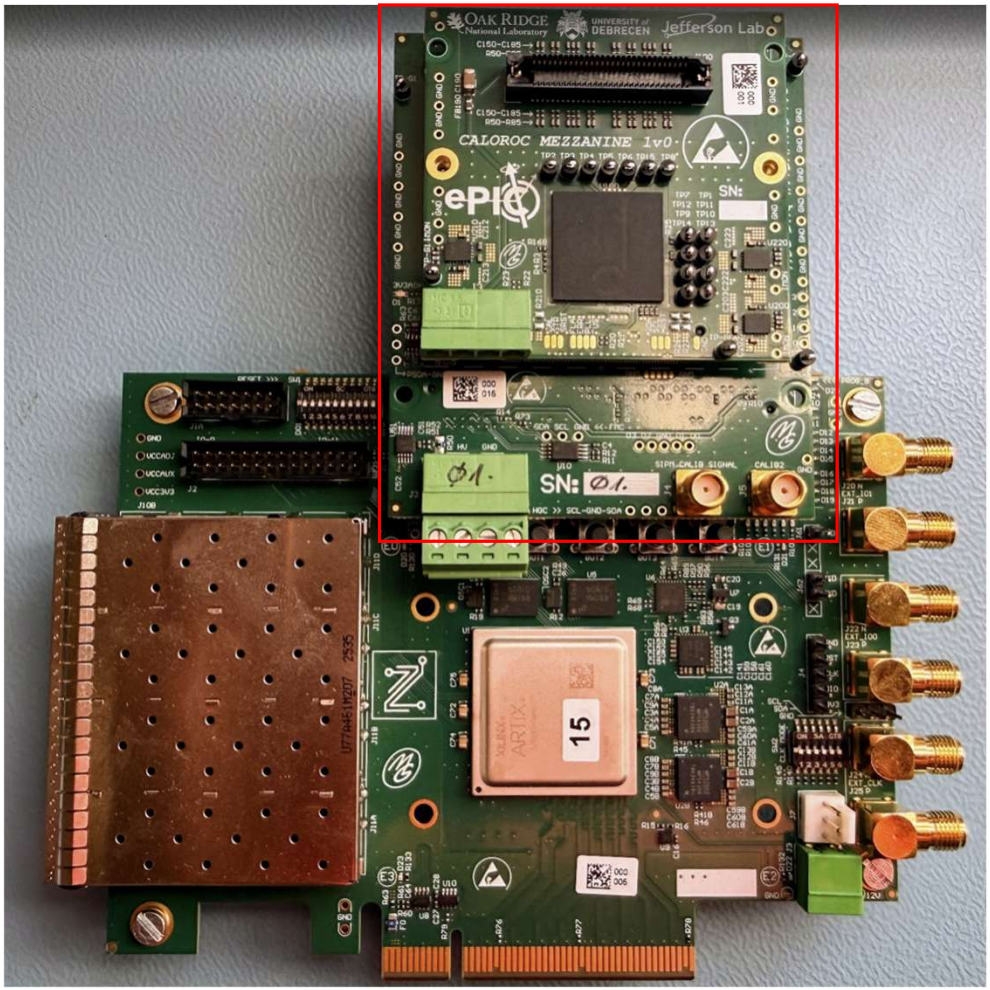
- Of course, we're open to support other groups with motherboard design as well. If there is a need for it

When are we now? - CALOROC

- The CALOROC mezzanine is available
- With A and B version

- This mezzanine will be available in the DB-MB setup
- The FW is currently under development

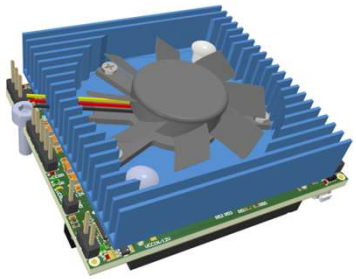
(On the temporary board shown above.)



Aggregation – Full Chain test 4:1

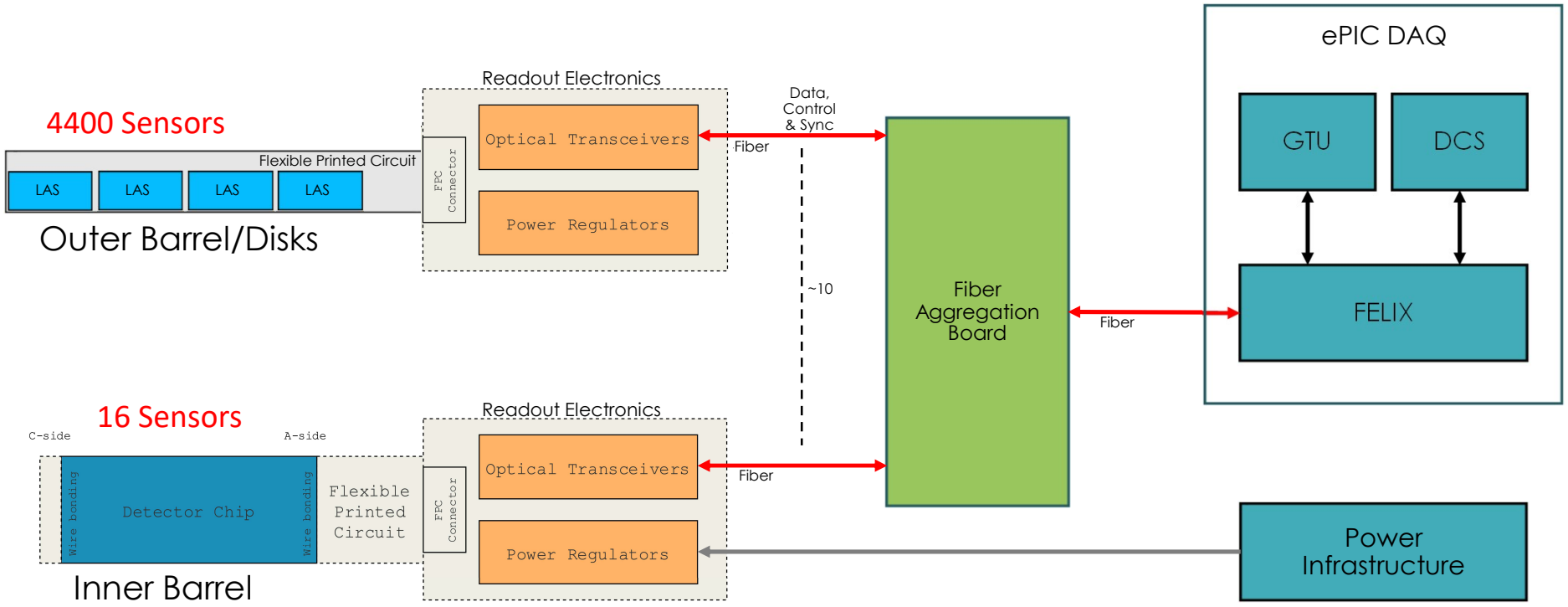
- Data receiveing from LpGBT chips via 4 lanes at a speed of 10 Gbps
- Do the aggregation with GRDO
- Then forward it to FELIX at a speed of 25 Gbps

4:1



This or a similar configuration could be used in several places

MAPS Tracker “SVT” Readout Concept



When are we now? – Rack mounting

- A couple of initial proposals have been drafted
- We're still in the very early stages, and there's still a lot of work to be done

SVT version 1

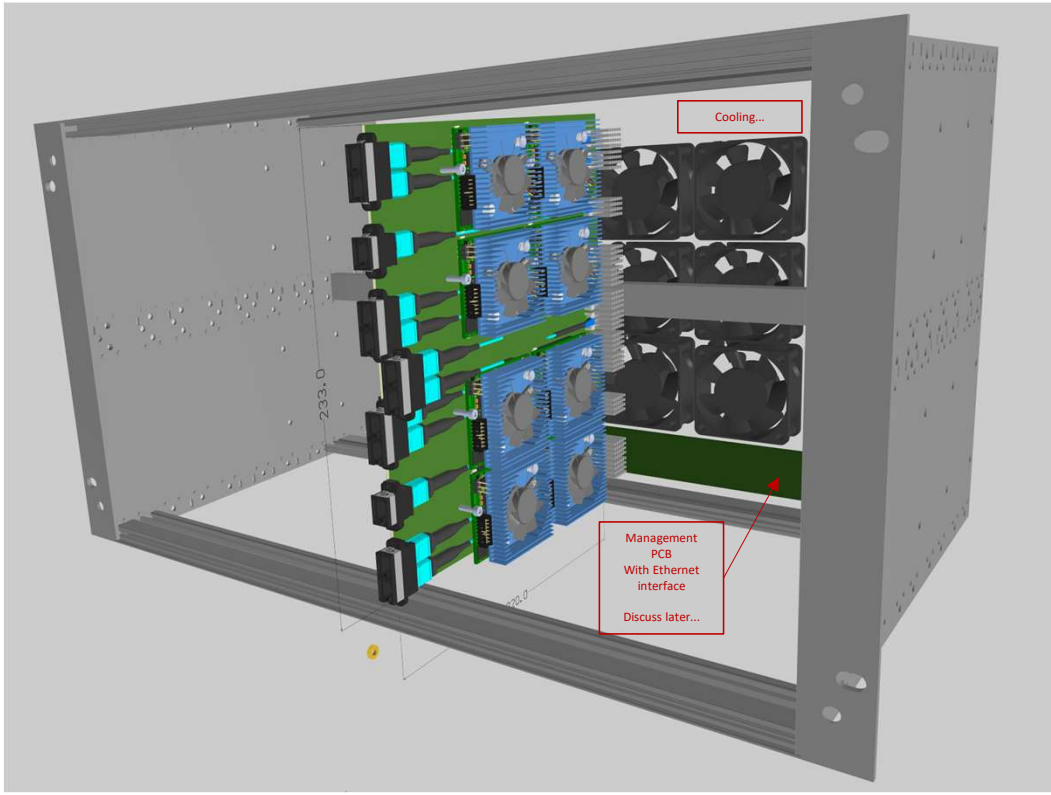
- Standard 6U height 19” rack from Fischer elektronik
- The space is enough for 10 boards
- BaseBoard size: 233x220 mm

Heights (mm):
- Cooler (passive) : 10.5
- FPGA : 3.5
- PCB (RDO) : 2.0
- BB CON ERF5/ERM5 : 9.0 - 12.0
- BaseBoard PCB : 1.6
  Total : **26.6 - 29.6**

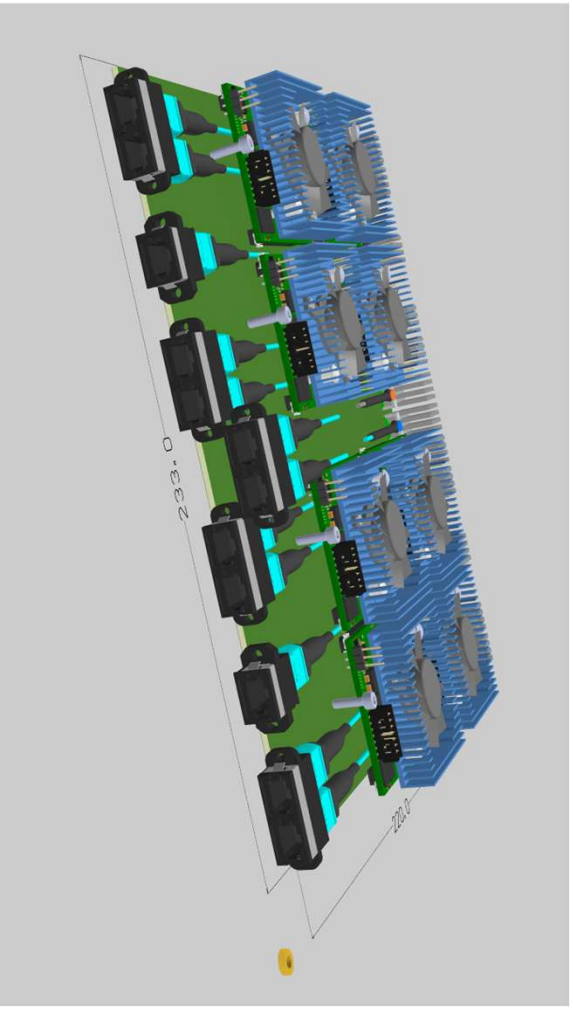
- OPA (Single, Dual) : 25x9.8, 34.8x9.3
- RACK 19 internal width : 431.8

- Available space for / 8 baseboard = 53.97 mm
- **Available space for / 10** baseboard **= 43.18 mm**
- Available space for / 12 baseboard = 35.98 mm

- Maybe even 12 is possible...



SVT version 1



8x

12 RX Only Input (10G) from detector patch panel

Each RDO has one FIREFLY connector

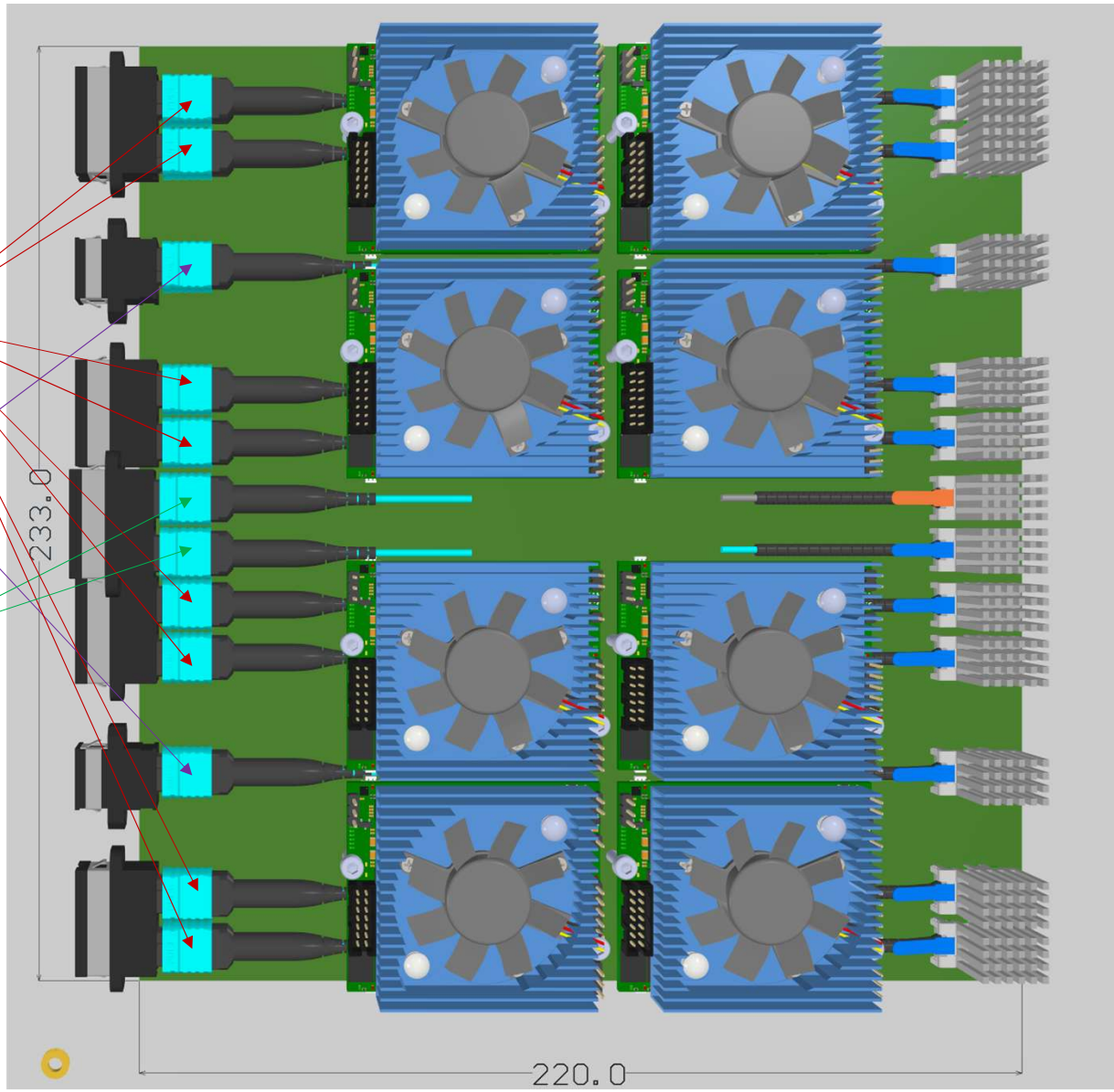
2x

TO/FROM FELIX FIREFLY 25G 4RX / 4TX

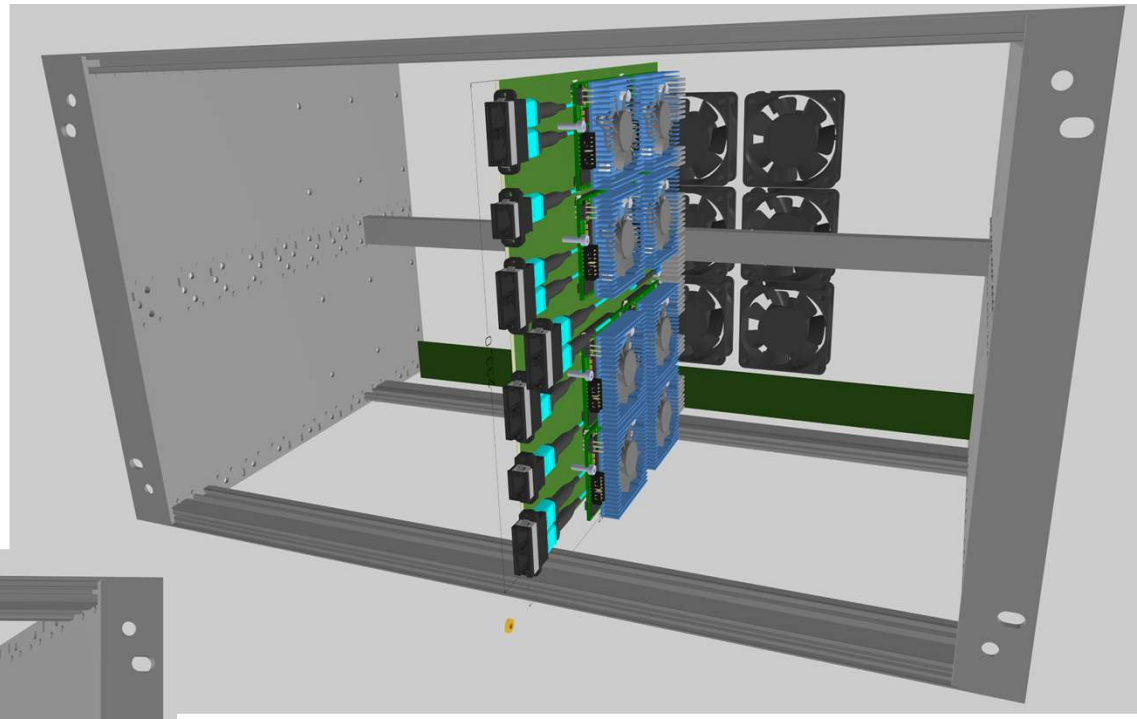
Each RDO has one 25G RX/TX connecton to FELIX

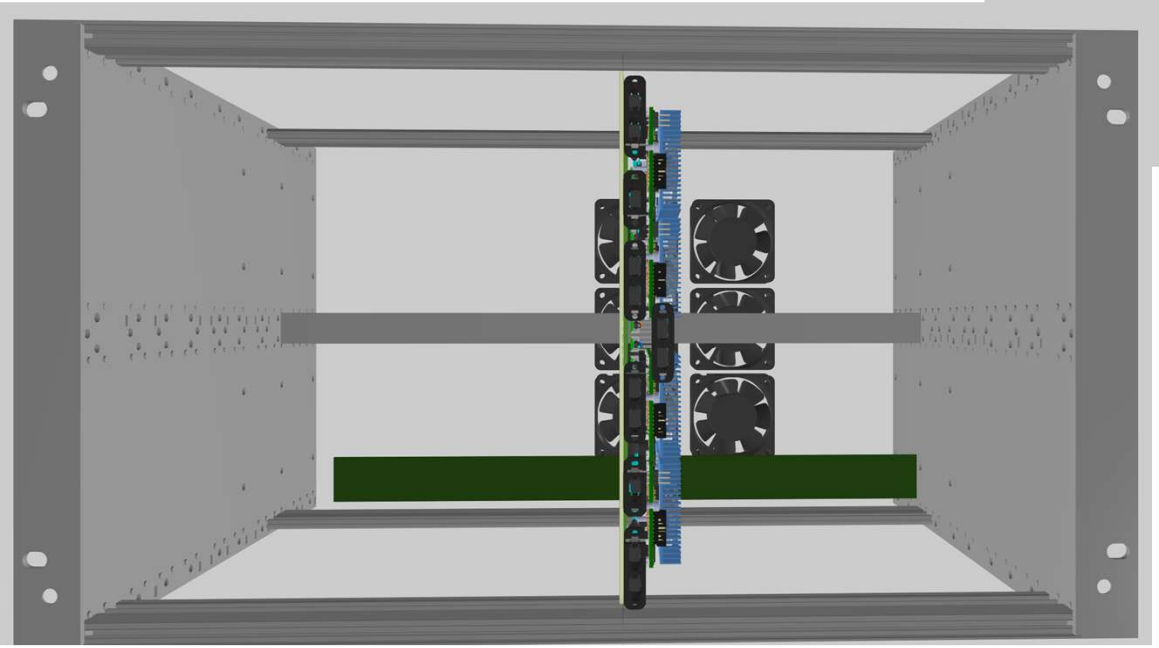
Each RDO has 1-1 TX/RX lines to detector because slow control...

1-1 TX/RX Output (10G) to detector patch panel

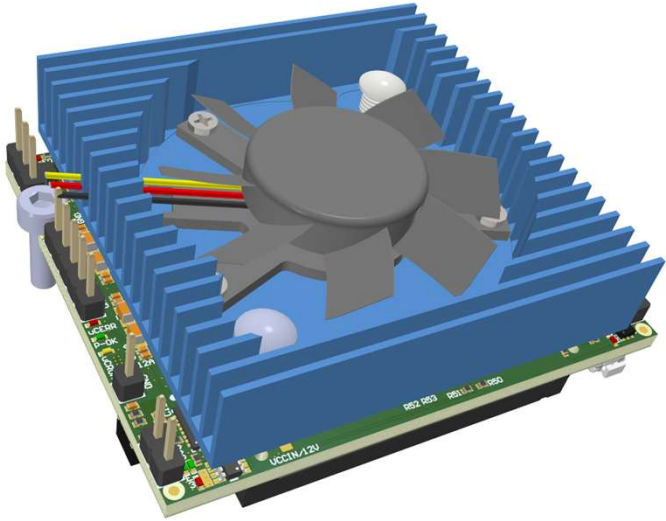


SVT version 1





Summary



- RDO: The design is pracically ready to order → Available: 3 month from order
- RDO: If You need test article please let me know
- RDO: the first MB-DB combination is suitable for testing the
  - DB itself (Production test)
  - CALOROC – chip testing
  - CALOROC – calorimeter full chain test - 4:1 aggregation
  - FIREFLY loopback
  - SVT full chain test – Further planning is needed
- Many FW activity needed
- If HW/FW design support needed from us please let me know
- Rack mounting: it's in the brainstorming phase. Discussions and decisions are needed

?


Thanks!