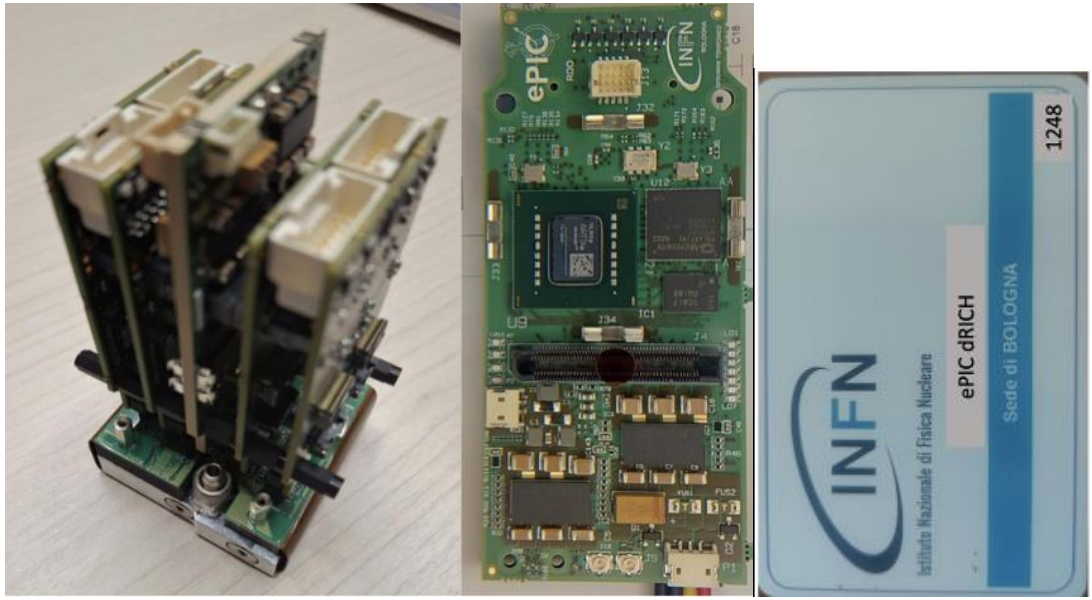

ePIC dRICH RDO

Status of dRICH DAQ

P. Antonioli – INFN Bologna
on behalf of ePIC dRICH Collaboration

July 16, 2026

What you will not hear in this talk

- ✓ ALCOR updates: → see Fernando's talk
  F. Cossio, last eRD109 update
  F. Cossio and G. Dalla Casa, ALCOR Internal Review
- ✓ dRICH DAQ backend setup & studies for data reduction → see Cristiano's talk
  C. Rossi, Real Time 2025 Conference

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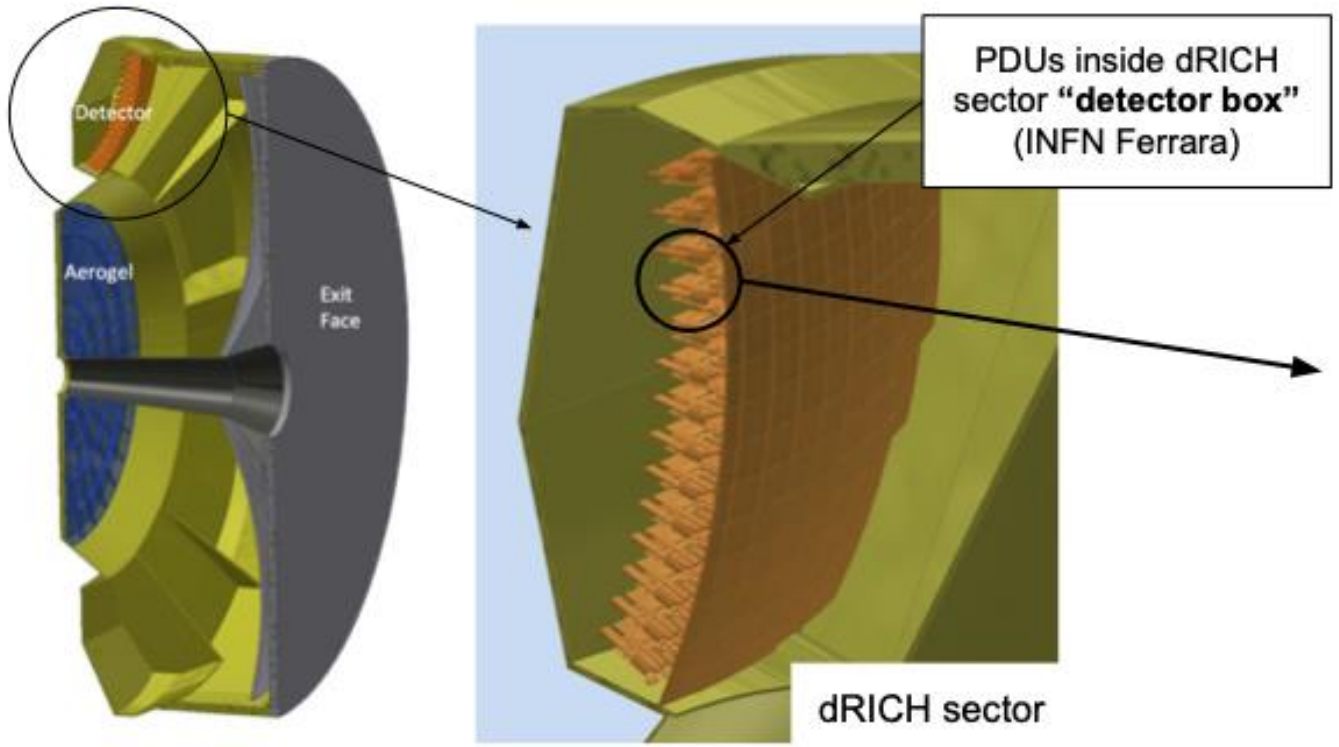
  C. Rossi et al., Real Time 2025 Conference

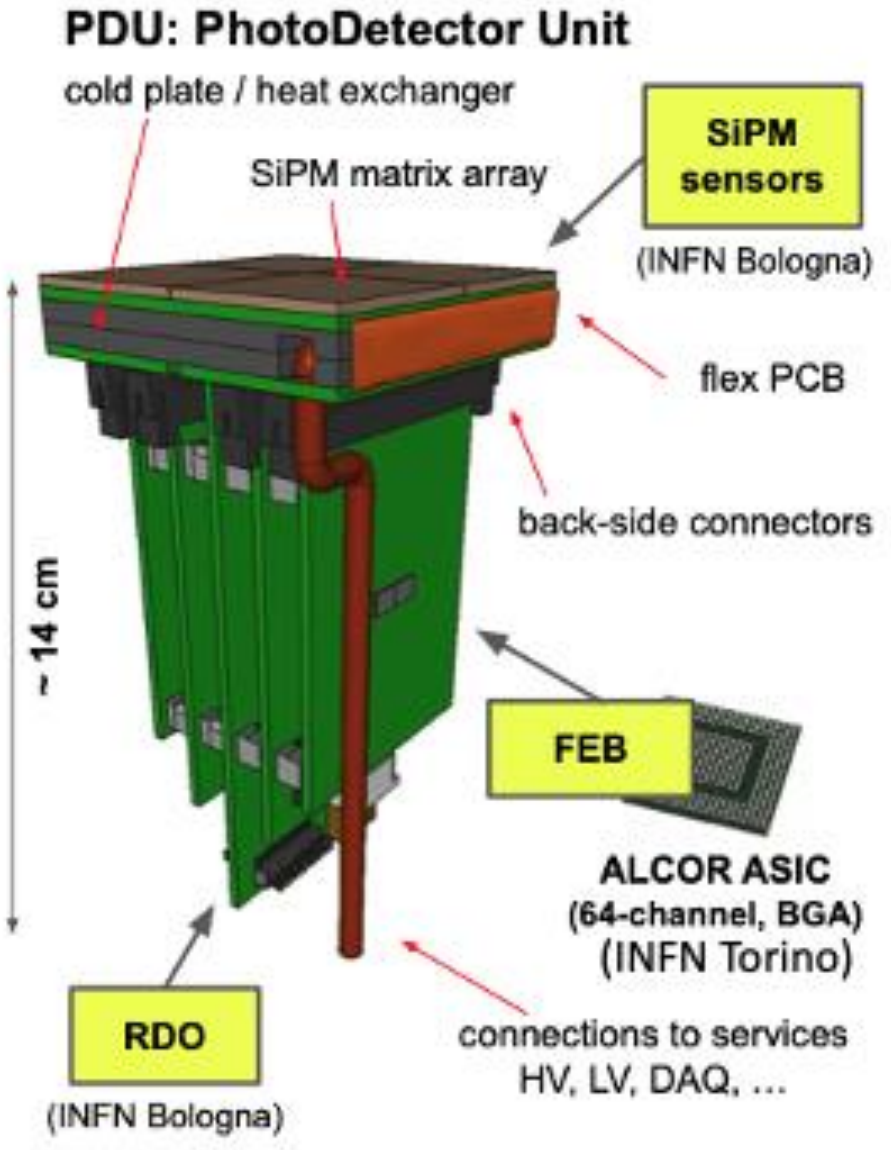
- ✓ Clock recovery & phase
- ✓ Protocols & data format
- ✓ Radiation tests
- ✓ Data Rate Summary updates
- ✓ Towards RDO v1.1

Plans 2026/Q4 + 2027

(Provoking/Burning) Questions/Requests

dRICH recap in three slides (I): electronics





dRICH status & intro : M. Contalbrigo @RICH2025
Photosensors (SiPM): N. Rubini et al., NIM A 1082 (2026) 170890 (Wien 2025)
ALCOR (FEE ASIC): F. Cossio @PD2025
PID performance: T. Boasso @RICH2025
dRICH Interaction tagger: S. Vallarino @EICUG-ePIC 2025
RDO: P. Antonioli @EICUG-ePIC 2025
RDO rad. tests: S. Geminiani @TWEPP2025
ML for data reduction in DAMs: C. Rossi @RICH2025

dRICH recap in three slides (II): test beams

from the first prototype

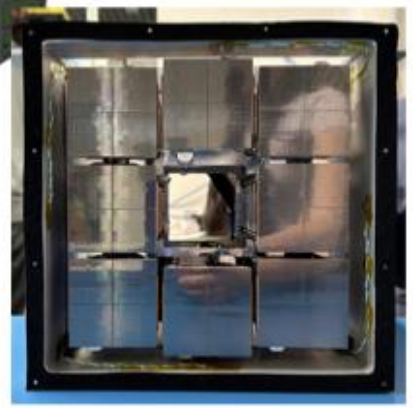
towards detector construction

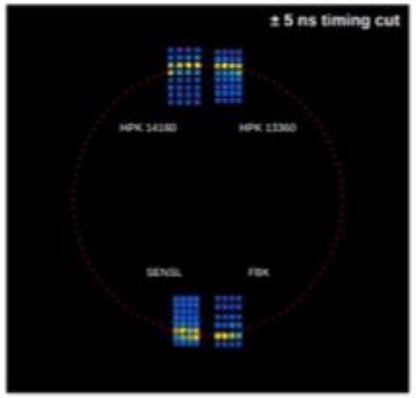
2022
electronics v1

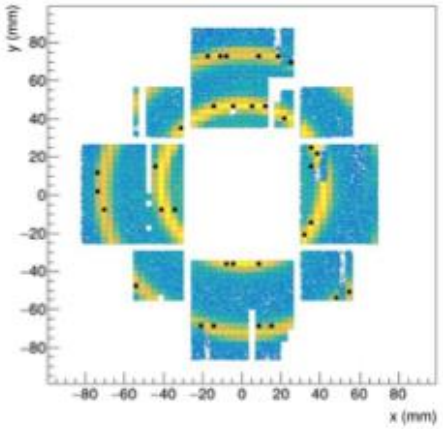
2023
electronics v2

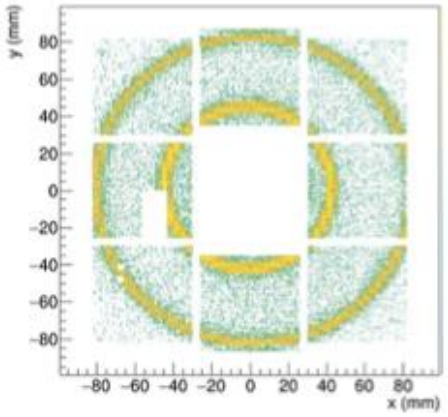
2024
electronics v2.1

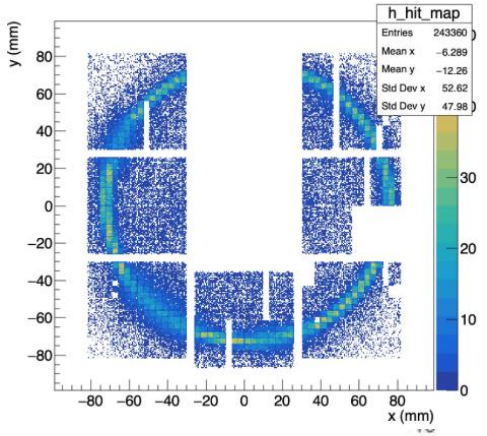
2025
electronics v3











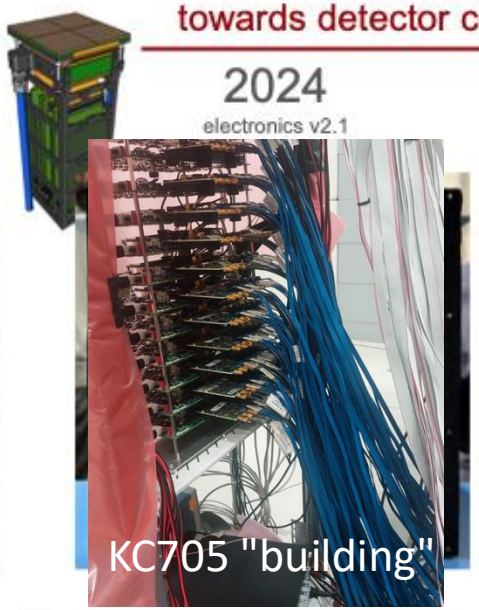
KC-705 readout + IPbus

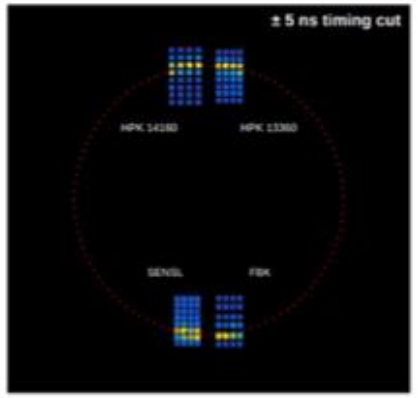
RDO readout + IPbus

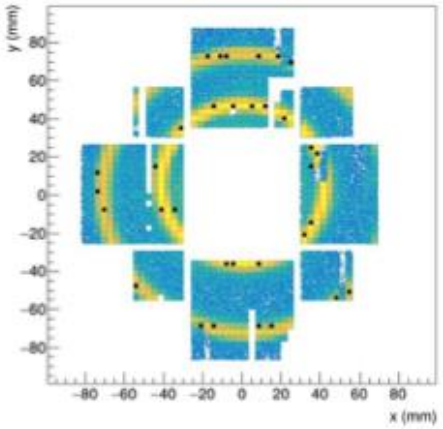
dRICH recap in three slides (II): test beams

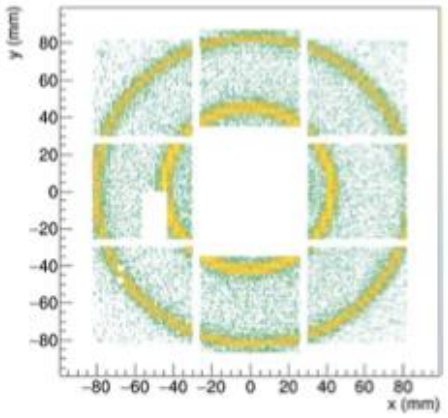
from the first prototype — towards detector construction

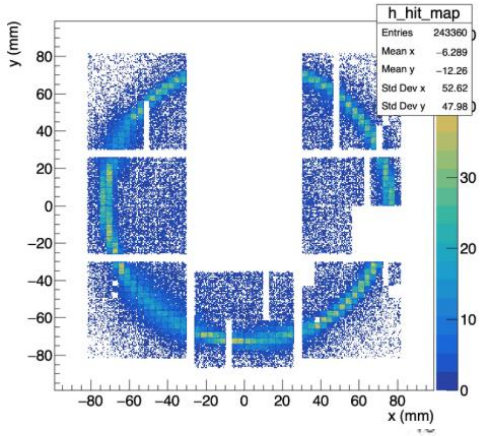
2022 electronics v1 | 2023 electronics v2 | 2024 electronics v2.1 | 2025 electronics v3











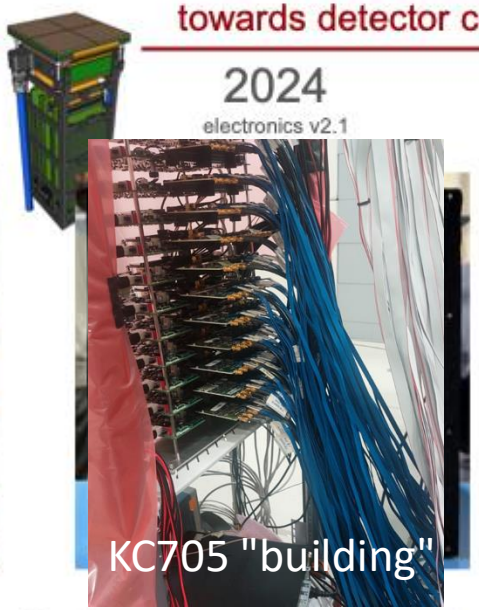
KC-705 readout + IPbus

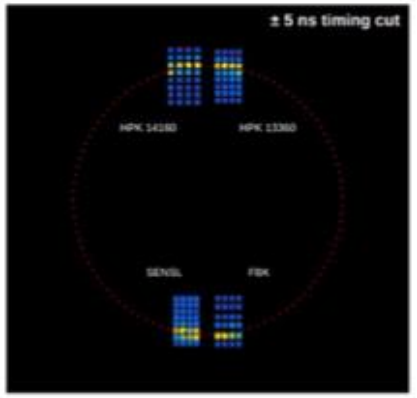
RDO readout + IPbus

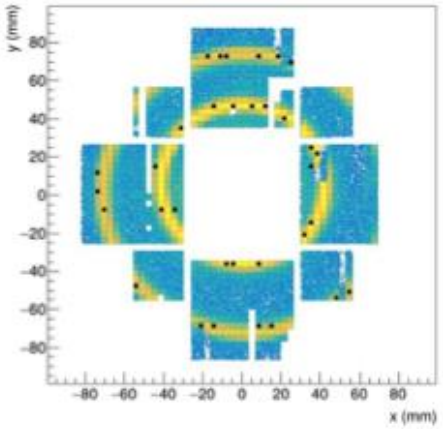
dRICH recap in three slides (II): test beams

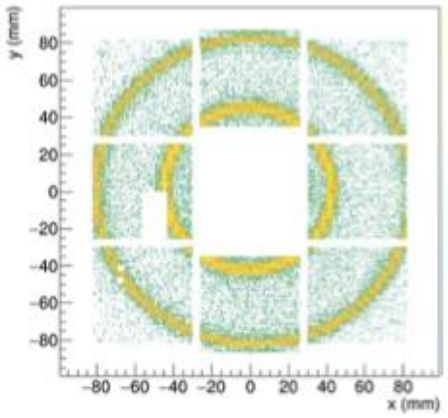
from the first prototype — towards detector construction

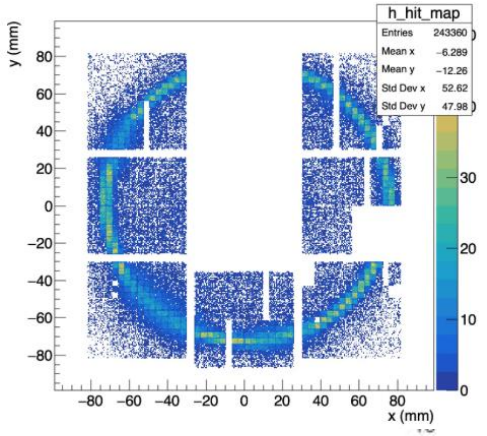
2022	2023	2024	2025
electronics v1	electronics v2	electronics v2.1	electronics v3











KC-705 readout + IPbus

RDO readout + IPbus

dRICH recap in three slides (II): test beams

from the first prototype — towards detector construction

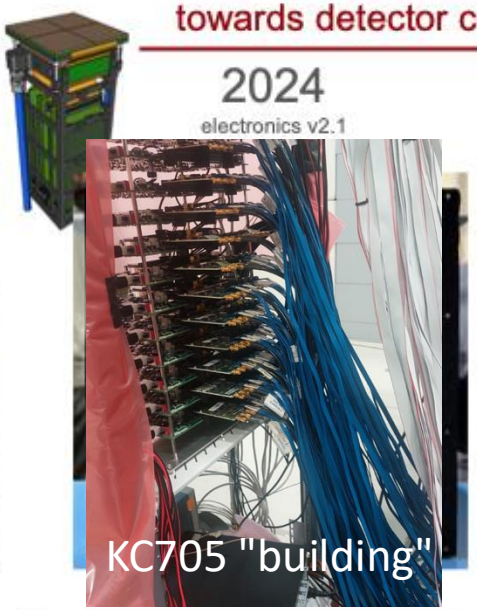
2022 electronics v1

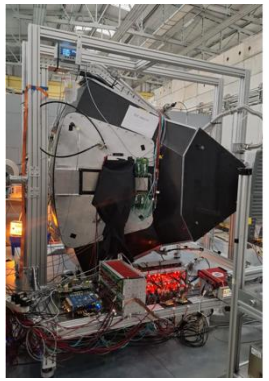
2023 electronics v2

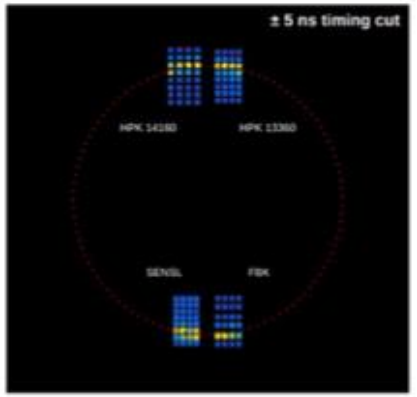
2024 electronics v2.1

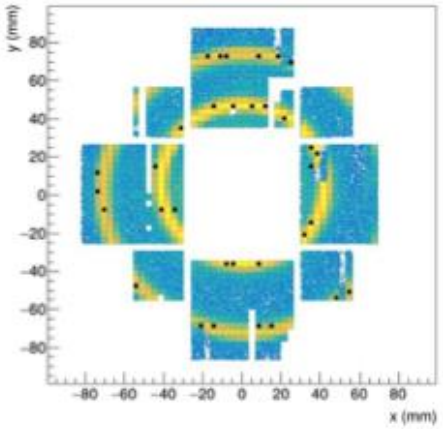
2025 electronics v3

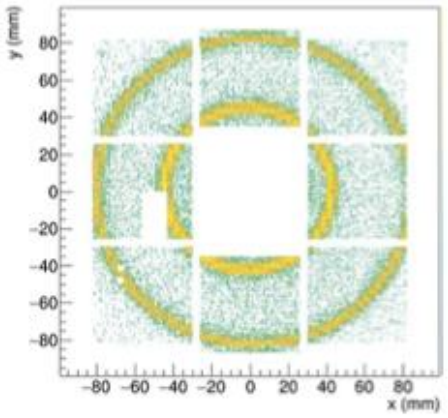
2026 Real scale prototype

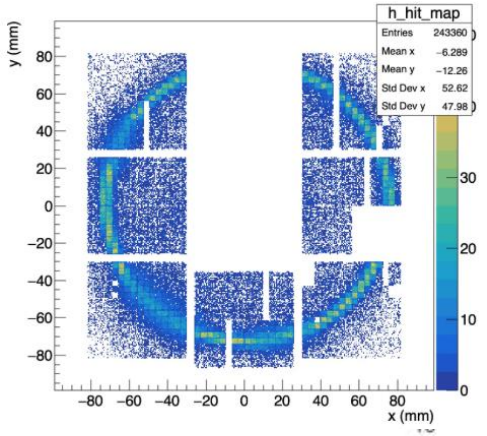


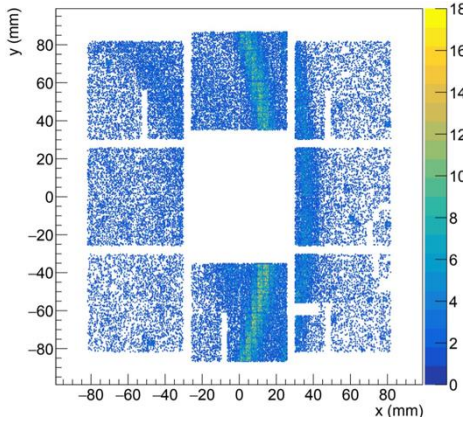










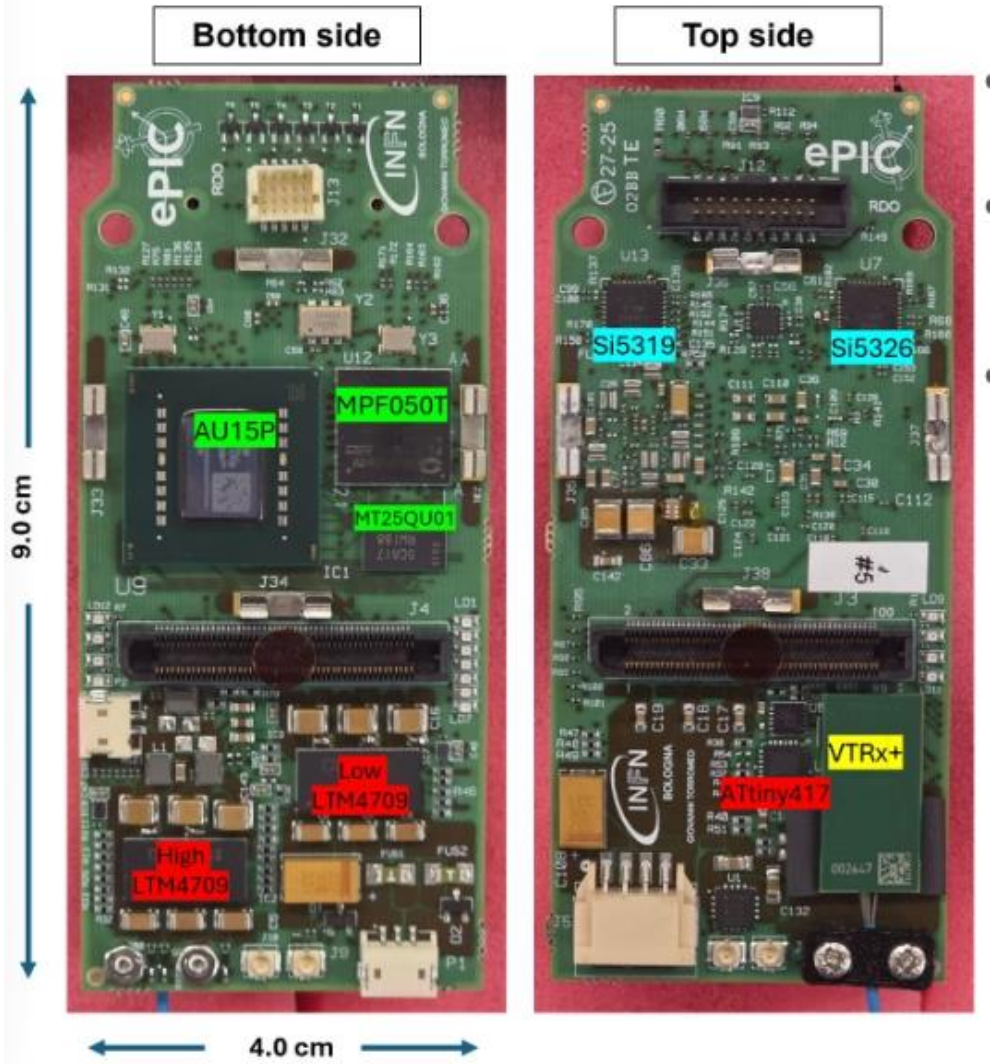


KC-705 readout + IPbus

RDO readout + IPbus

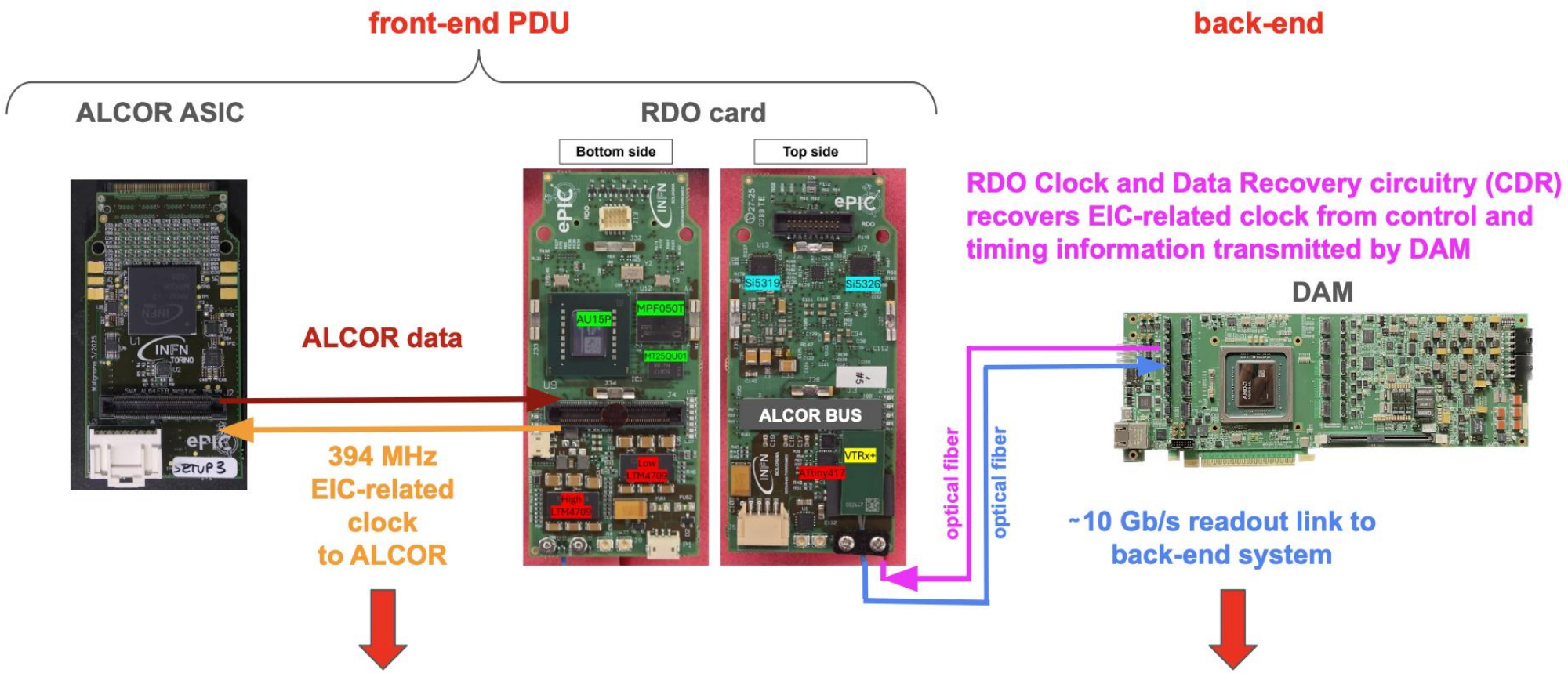
RDO readout + IPBUS

RDO recap in two slides (I)

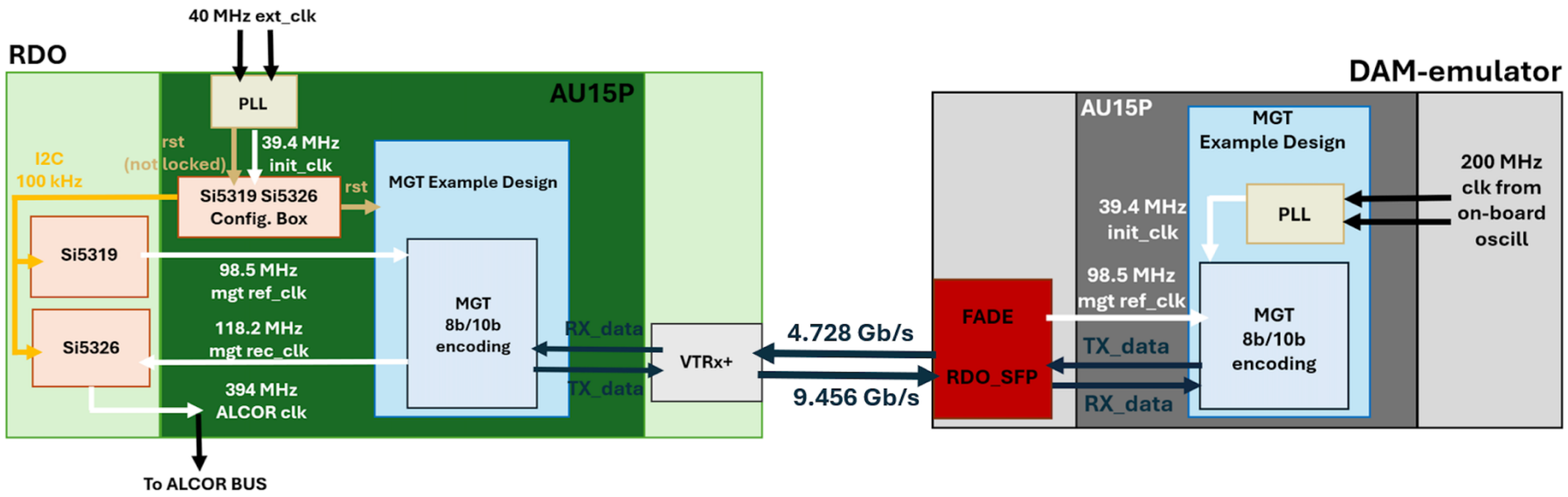


- High density
- Key FPGA architecture: Artix (SRAM-based) + PolarFire (Flash-based)
- Radiation tolerance achieved via scrubbing
- Double ALCOR bus towards FEB
- VTRx+ as optical transceiver
- Clock management supported by two SkyWorks jitter-attenuating clock multiplier

RDO recap in two slides (II)



RDO-DAM development: setup



FADE card received by JLab

We might move to 2.5 Gb/s downlink

RDO

Downlink (DAM→RDO), ~5 Gb/s

Optical fibers

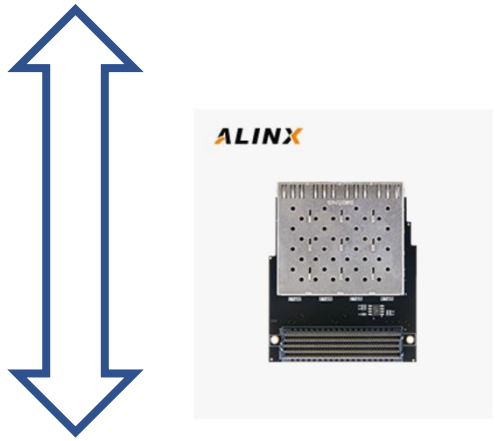
Uplink (RDO→DAM), ~10 Gb/s

DAM EMULATOR

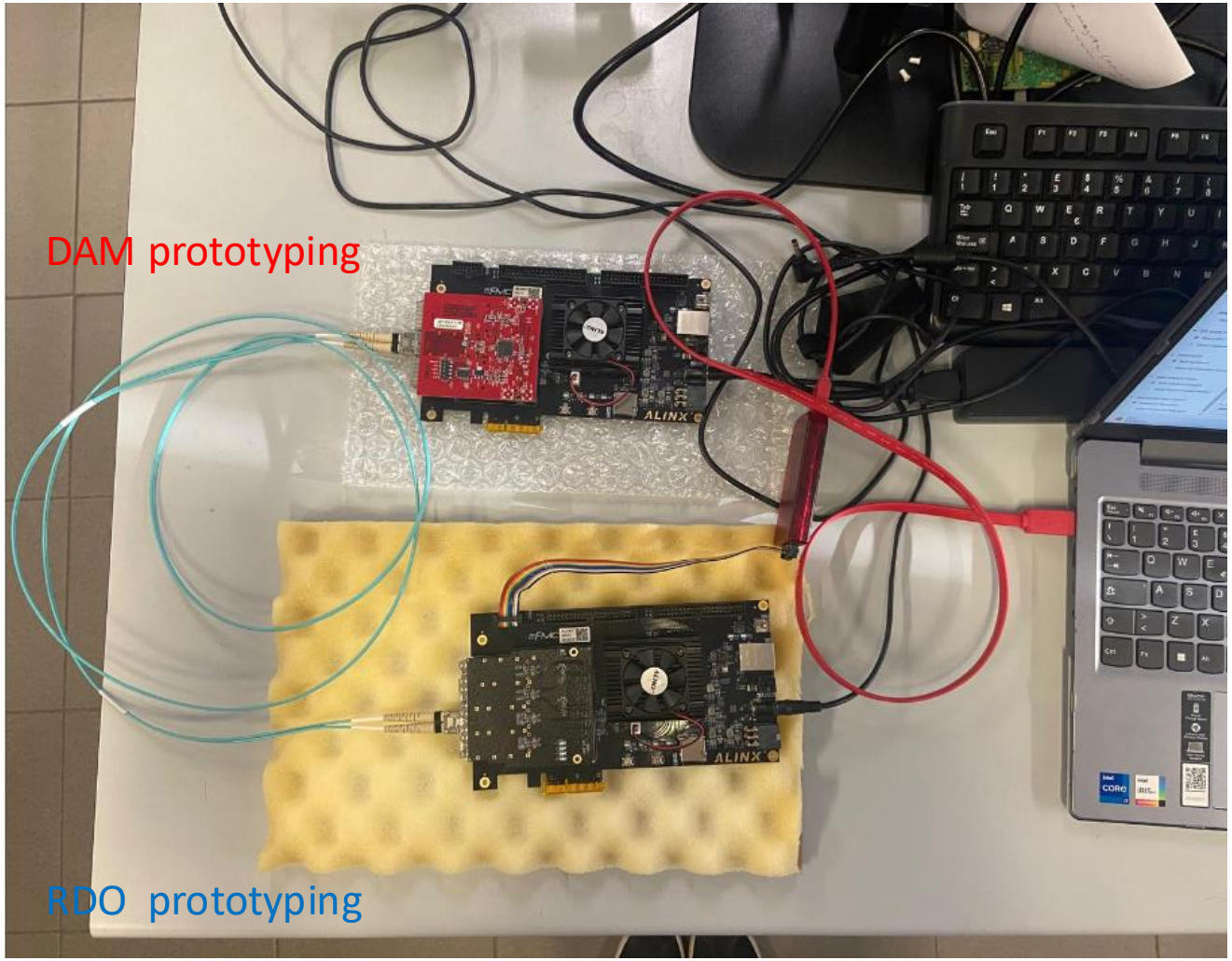
Alternative test setup

A valid test-bench for development is also this one. We have been “forced” to move to it during test-beam operations (all RDO @ CERN!)

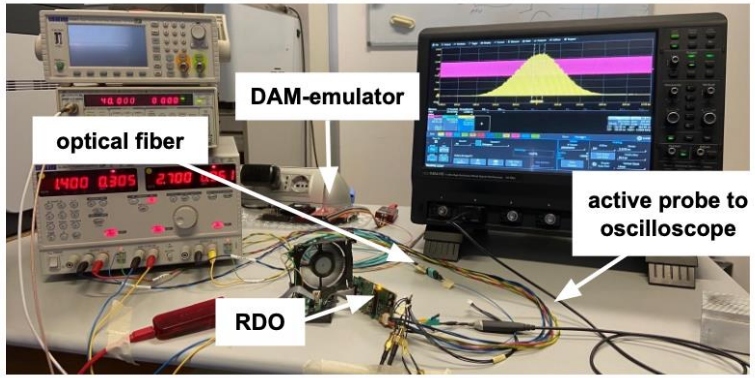
(ALINX AUX15P + FADE) → DAM emulator

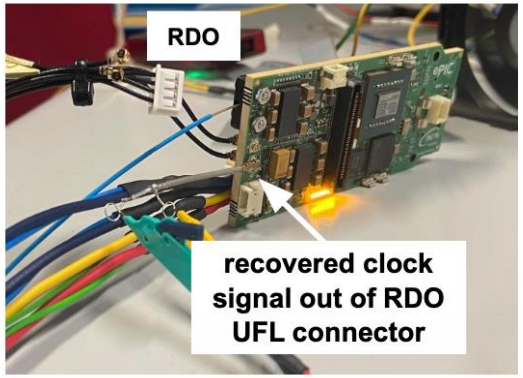


(ALINX AUX15P + FH1223) --> RDO emulator



RDO: recovered clock tests





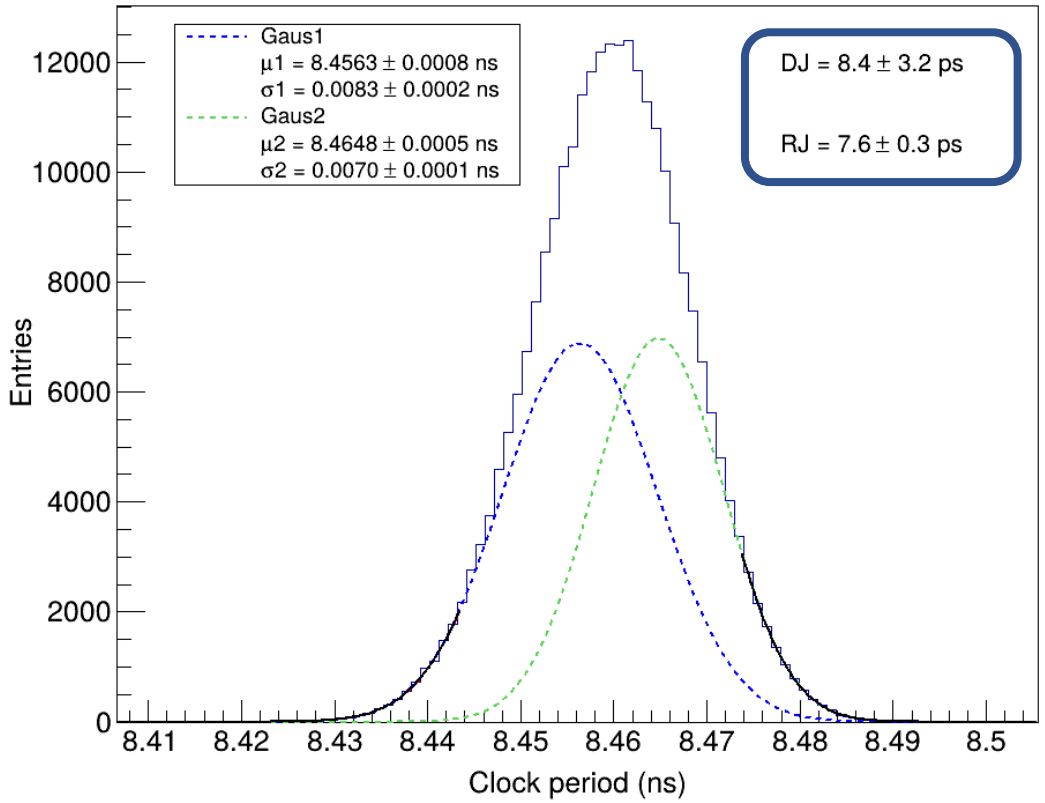
Several transceiver configuration tested
8b/10b encoding

$$REC_{CLK} = \frac{LineRate}{DataWidth} = \frac{4.728\ Gb/s}{40\ b} = 118.2\ MHz$$

$$REC_{CLK} = 3 \times EIC_{CLK}$$

Good result on jitter with Artix as expected

Next:
→ Go through Si5326 (x 10 → 394 MHz)
→ Phase stability: use CERN HPTD IP core?



Downlink operated at 9.456 Gb/s

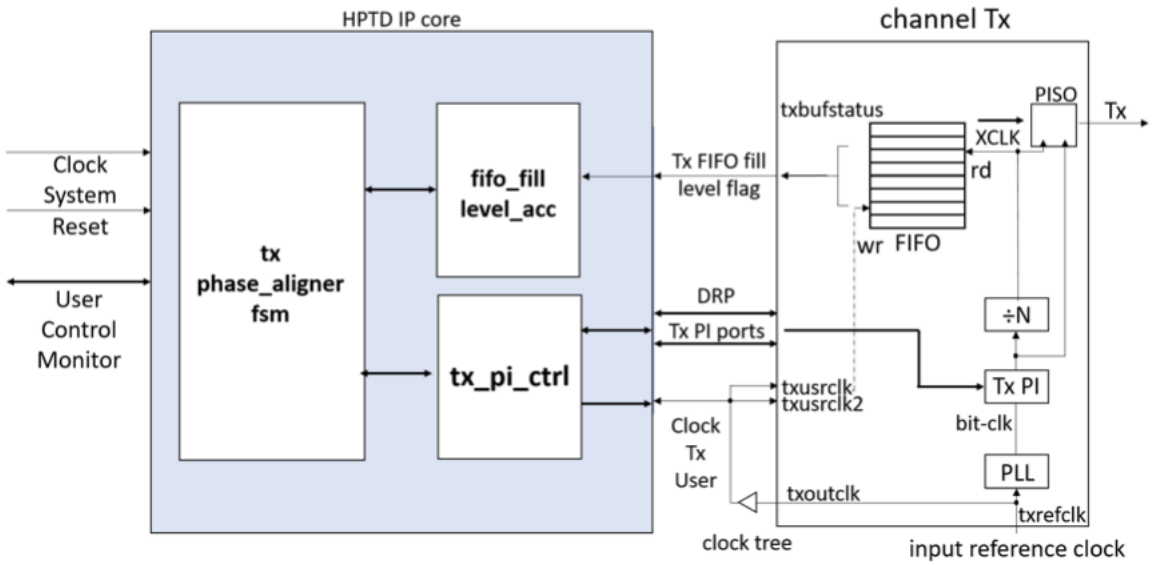
O(10) ps jitter

M. Panza, master thesis

RDO: recovered clock: phase stability (I)

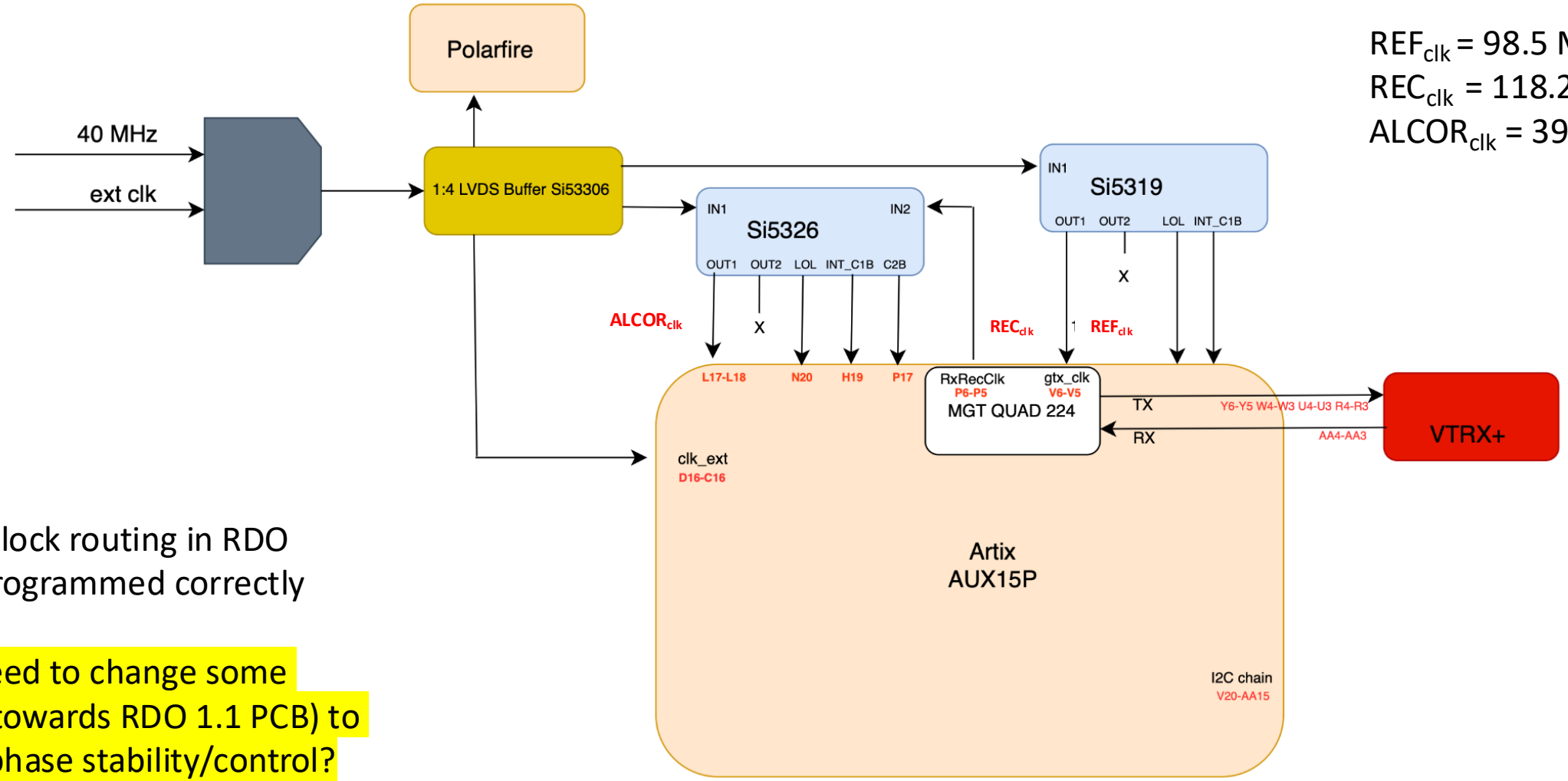
Next: study the issue

- Do we really need phase stability or we can quickly calibrate it?
- Is phase random set at every FPGA reset? Over which range?
- Test CERN system developed for Ultrascale: S. Baron et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL. 67, NO. 3, MARCH 2020
- P. Bacheck, (BNL) at FPGA Developer Forums (2025) presented implementation for Ultrascale+ for EIC



It would be helpful having common approach within ePIC, share know-how, etc.

RDO: phase stability (II)



REF_{clk} = 98.5 MHz
REC_{clk} = 118.2 MHz
$ALCOR_{clk}$ = 394 MHz

Current clock routing in RDO
Si5326 programmed correctly

Do we need to change some routing (towards RDO 1.1 PCB) to achieve phase stability/control?

RDO: protocols & data format

In the absence of centralized ePIC standards, we are going to select on our own link protocols

- dRICH forum setup (INFN BO/RM1/TO currently)
- Preparation of a formal URD → to be open to dRICH input by EoY + EL&DAQ WG/conveners?

dRICH ePIC DAQ

Synchronization, protocols and data format

User Requirement Document

Modification History

Version	Date	Description	Author
0.1	2026/04/10	First version	P. Antonioli
0.2	2026/04/13	Corrected error about EoC status word	PA
0.3	2026/04/23	Fixed uplink-downlink definition	AL
0.4	2026/07/10	Leading and trailing Orphans handling	PA/MD

RDO: protocols and data format

RDO-DAM

Under test:

- 8b/10b
- AURORA 64b/66b current baseline agreed between BO-RM1 (it implies no FEC, but maximize bandwidth)
- lpGBT (considering FEC5, no e-link)

Bits 21-11: EIC BC

50	49 48	47 45	44 42	41 40	39 33	32 24	23 22	21 9	8 0
0	FEB ID	Col ID	Pixel ID	TDC Id (trail)	Coarse (trailing)	Fine (trailing)	TDC Id (lead)	Coarse (leading)	Fine (leading)

RWORD=RDO word
51-bit word derived from two 32-bit ALCOR word

Note:

- RWORDs are transmitted for each FEB time-ordered encapsulated within an ORBIT FRAME
  - ✓ See F. Lo Cicero, ePIC Collaboration Meeting, January 2026
  - ✓ See P. Antonioli, SRO XIII Workshop, December 2025
- trailing edge (in TOT or Slew Rate) is encoded as a Time-Over-Threshold or Tine-Between-Thresholds i.e. always relative to matching leading edge

RDO: data encapsulation

- dRICH hits are encapsulated within ORBIT FRAMES (OF) → == 12 μs (not to be confused with TF and STF)
- OF header and trailer allows retrieval of EIC Orbit
- Status words used for debug purposes

Frame Header																		K28.0							
50	49	48	47	45	44	43	42	41	40	39		24	23	8	7								0
1	FEB ID		Col ID		C	0	0	0	0	RDO Orbit Counter (16-bit)			ALCOR FRAME Counter (16-bit)		0	0	0	1	1	1	0	0

End of Frame / Roll Over																		K28.2							
50	49	48	47	45	44	43	42	41	40	39		32	31	24	23	8	7								0
1	FEB ID		Col ID		0	0	0	0	0	OUT FIFO loss			IN FIFO loss		Frame length (coarse counter at RevTick)		0	1	0	1	1	1	0	0

Status word pixel [0-7]																		K28.3							
50	49	48	47	45	44	43	42	41	40	39				8	7										0
1	FEB ID		Col ID		0	0	X	X	X	Status Word Pixel XXX=[0-7]					0	1	1	1	1	1	0	0

CRC / frame trailer																		K28.4							
50	49	48	47	45	44	43	42	41	40	39			24	23		8	7								0
1	FEB ID		Col ID		E	0	0	0	0	Number of words in frame				CRC value			1	0	0	1	1	1	0	0

RDO-DAM: data format/communication

	Reserved		DF3	DF2	DF1	DF0	DCS (free)						RWORD	
"FULL"	320	256	255	254	253	252	251	204	203	153	152	102	101	51	50	0
lpGBT (*)	255	224	223	222	221	220	219	204	203	153	152	102	101	51	50	0
AURORA 64/66	66	64	63				62	51	50							0

(*) for lpGBT bits 255-224 are reserved by the protocol (FEC5) encoding/load balancing is obtained via a low-level 64-bit word

- 4 RWORDs can be packed in 256 bits (“FULL ready”), 204 bits (“lpGBT ready”) or 1 RWORD in 66 bits (AURORA ready), leaving spares for DCS
- DCS bits to be used to pass info like temperature, voltages, current, status, etc.

64-bit dRICH word finally passed by DAM to ECHELON (note we pass OF and then can be packed in TF)

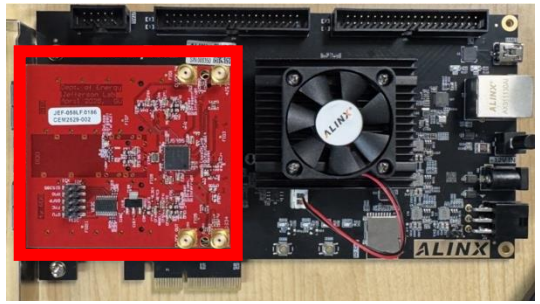
Is **TF-encapsulation** DAM FW responsibility or HOST server software responsibility?

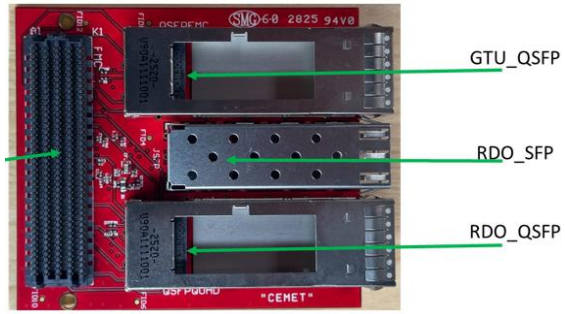
63	62	61	60	50	49 48	47	45	44	42	41 40	39	33	32	24	23 22	21	9	8	0
0			RDO ID		FEB ID	Col ID		Pixel ID		TDC Id (trail)	Coarse (trailing)		Fine (trailing)		TDC Id (lead)	Coarse (leading)		Fine (leading)	

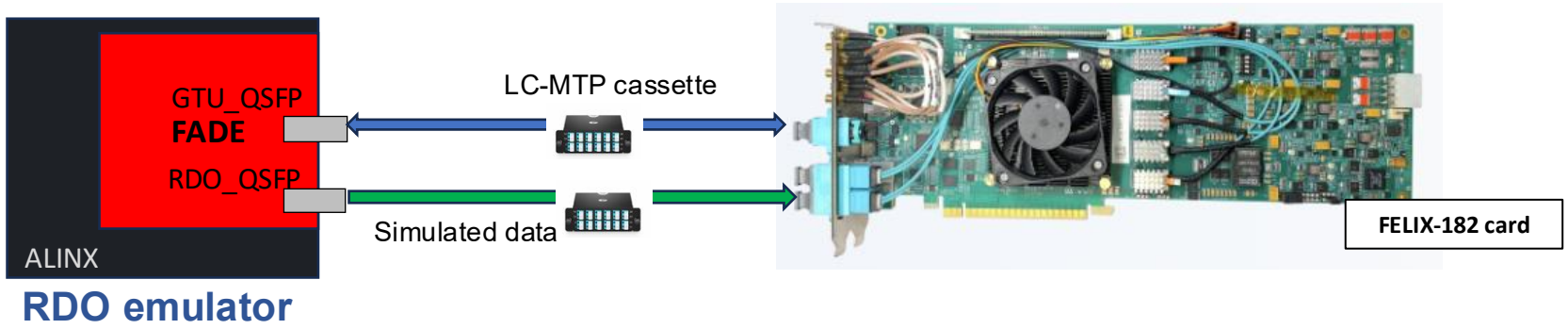
FLX-182 – RDO/GTU connection test

FMC FADE Adaptor card module as RDO/GTU emulator:

- ALINX+FADE sends the RDOWORDs via the RDO_QSFP
- ALINX+FADE sends the System clock (19.7 MHz) and the run control (7.88 Gbps), it receives the 'DAM' status via the GTU_QSFP connector





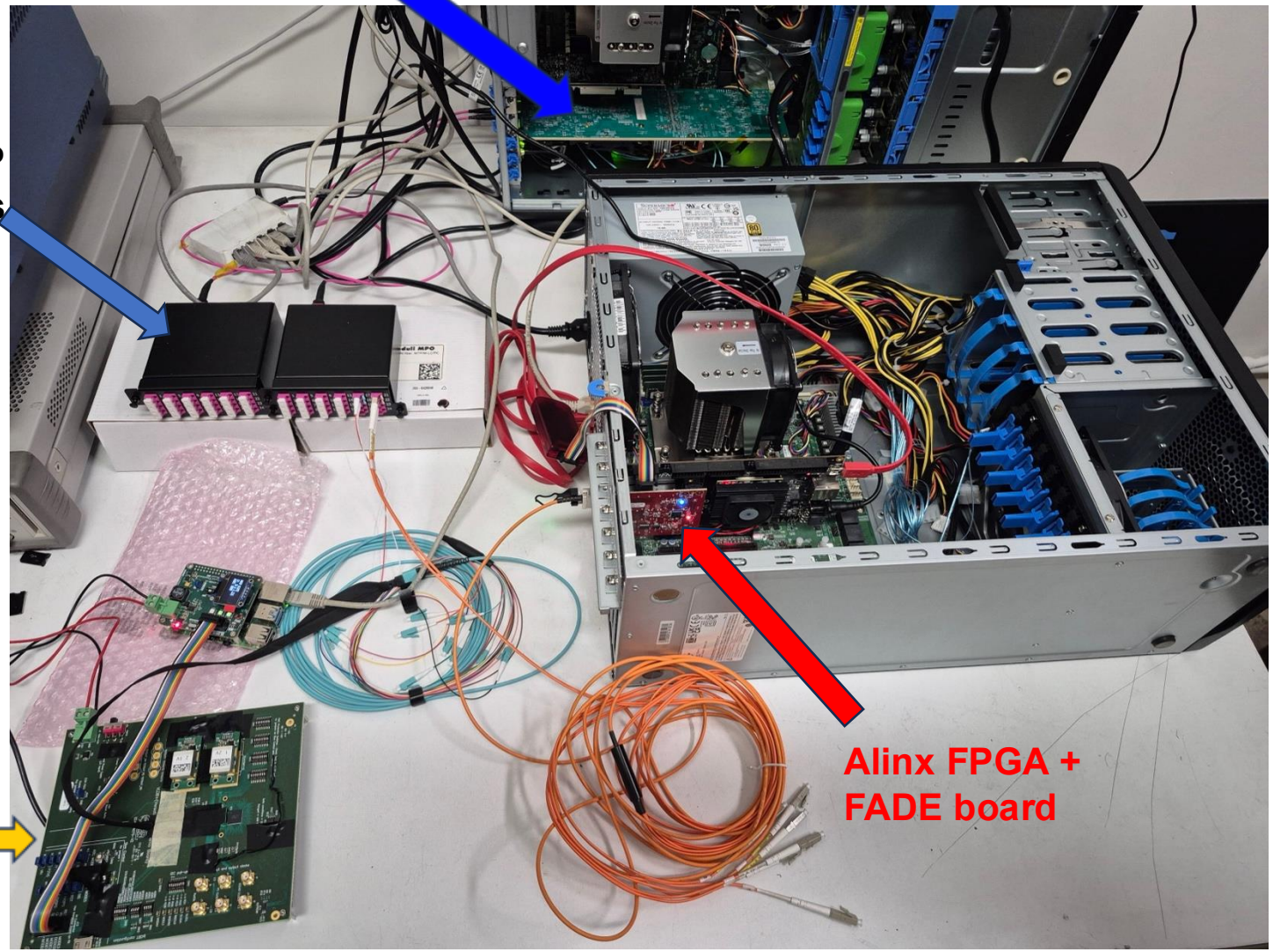


- GTU-DAM Communication based on Aurora 8b/10b protocol
- RDO-DAM Communication based on Aurora 64b/66b protocol
- DAM-DAM(TP) Communication based on Aurora 64b/66b protocol

DAM –RDO/GTU emulator TB

FLX-182

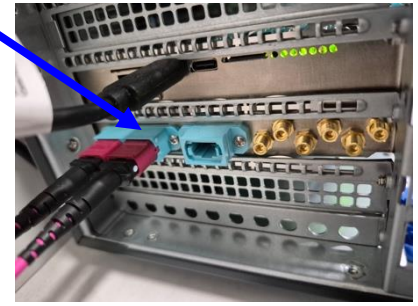
2 x cassette MTP
to 24 LC ports



Alinx FPGA +
FADE board

VLDB+

FLX-182: 2 MTP TX/RX
24 channels ports



Alinx+FADE: 2 QSFP+
ports + 1 SFP port

FLX-182–RDO/GTU Test

- ALINX+FADE: GTU-DAM connection (8b/10b):
  - FADE card's GTU qsfp connected in loopback

Data generated by internal random generator (LFSR) received with NO ERROR

- FLX182: GTU-DAM connection (8b/10b):
  - Test of Versal transceivers in 8b/10b encoding mode (7.88 Gbps) ongoing

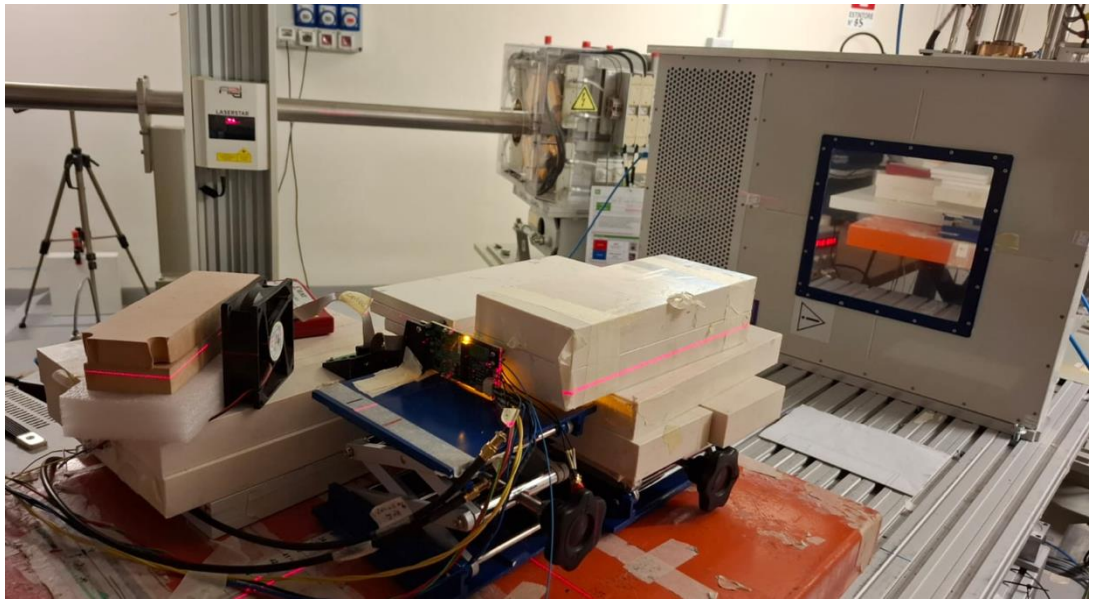
- FLX182: RDO-DAM connection (64b/66b):
  - FELIX MTP channel set in loopback using LC optical cables

Error-free data transmission at 10 Gbps

RDO radiation tests (update & plans)

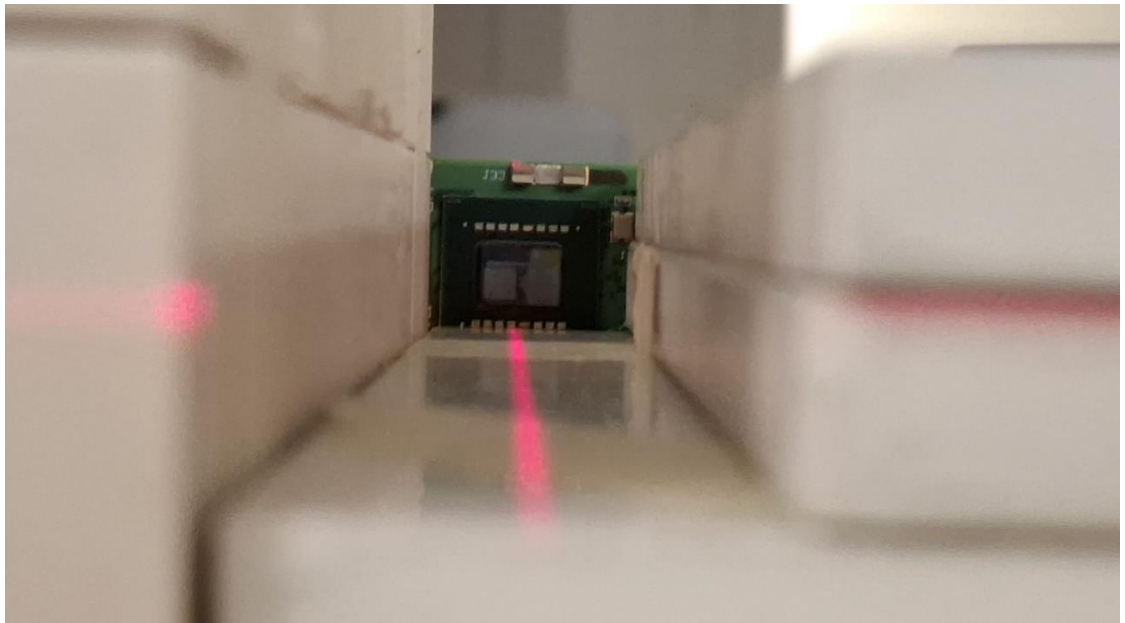
All components individually validated
Artix scrubbing (on error detection via PolarFire) implemented and tested (March 2026)

- S. Geminiani et al., *JINST* 21 (2026) 04, C04039
- D. Falchieri, eRD109 update, April 2026



TODO:

Artix blind-scrubbing → (September 2026)
Full RDO card exposure → (December 2026)
comparing lpGBT-FPGA IPCORE vs AURORA



Update on Data Rate Summaries

Not sure we are consistently filling this

ePIC Data Rate Summary

Detector			Readout Limitations					
System	Detector	Section	Readout / Element	Maximum Data Rate / Element	Maximum Hit Rate / Element	Minimum Distinguishable Hit Separation in Time	Likely Aggregation Limit Source	Hit Rate Capability including Aggregation (pro-rated to readout element)
	Lumi PS Tracker		EICROC (1024 Channel)	256 Mb/s	204 kHz	100 ns	EICROC	204 kHz
	Direct Photon Calorimeter		CALOROC (36 Channel)	2.52 Gb/s	7.8 MHz	125 ns	RDO	975 kHz
PID-TOF	Barrel		FCFD (32 Channel)	80 Mb/s	3 kHz	200 ns	FCFD	3 kHz
	Endcap		EICROC (1024 Channel)	256 Mb/s	204 kHz	100 ns	EICROC	204 kHz
PID-Cherenkov	dRICH		ALCOR (64 Channel)	1.7 Gb/s	21.1 MHz	125 ns	DAM	78 MHz
	pfRICH		FCFD (32 Channel)	80 Mb/s	3 kHz	100 ns	FCFD	3 kHz
	hpDIRC		FCFD (32 Channel)	80 Mb/s	3 kHz	100 ns	FCFD	3 kHz

Suggest to review comments with WG conveners

No instructions

I unilaterally split values!

Office on the web

Data Volume					
	Bits/Hit	Data Reduction Expected	Readout Elements / Section	Data Rate Full Section (Gb/s)	Allocated Data Volume To Tape (Gb/s)
	320.0			0.00	
	320.0			0.00	16.0
	100.0			0.00	
	320.0			0.00	
	160.0			0.00	
	80.0		4992	0.00	32.0
,000	160.0		2176	14.51	
	160.0			0.00	
				352.91	109.0

Simulated Rates						
Max Hit Rate / Readout Element (Physics) (Hz)	Max Hit Rate / Readout Element (SR) (Hz)	Max Hit Rate / Readout Element (Other Backgrounds) (Hz)	Expected Noise Hit Rate / Readout Element (Hz)	Max Hit Rate (All Sources) (Hz / Readout Element)	Avg Hit Rate / Readout Element (Hz)	Total Hit Rate for full Section (Hz)
			19,200,000			
14,100	No/Estimate	113,000	320	640,000	41,700	90,700,000

dRICH simulations still missing → working on simulations 26/04

RDO: towards RDO 1.1

By end of 2026 we want to order RDO v1.1, in principle “ePIC-ready”

Main/planned changes:

- Fix several mistakes (wrong routing of a signal needed by scrubbing, fix a footprint of a component, …)
- Add LVCMOS → LVDS
- Use different uC → SAMD21
- Different routing for clock?
- Shielding system for VTRX+ (light leak)
- (don’t mount the LEDs if we go inside PDU…)

Key points to be (still) investigated: checks on FPGA resources + routing for clock
Note: AU15P currently difficult to find on stock on main distributors
(and up to 52 weeks lead-time then!)

(+ FW: replace IPbus, matching, time-ordering)

Plan as a summary

Today — Sep 2026 — Oct 2026 — Dec 2026

This talk

blind scrubbing test

RDO-DAM(FADE) protocol
V 0.1 released

RDO v1.1 PCB →

Protocol test under irradiation
Full RDO irradiation

RDO – DAM (FLX) implementation

← *RDO pre-production* →

Jan 2027 — Mar — Jul — Nov

FLX – prototype integration (lab)

Test beam (“full chain”)
ALCOR64+RDO+*FLX-155*

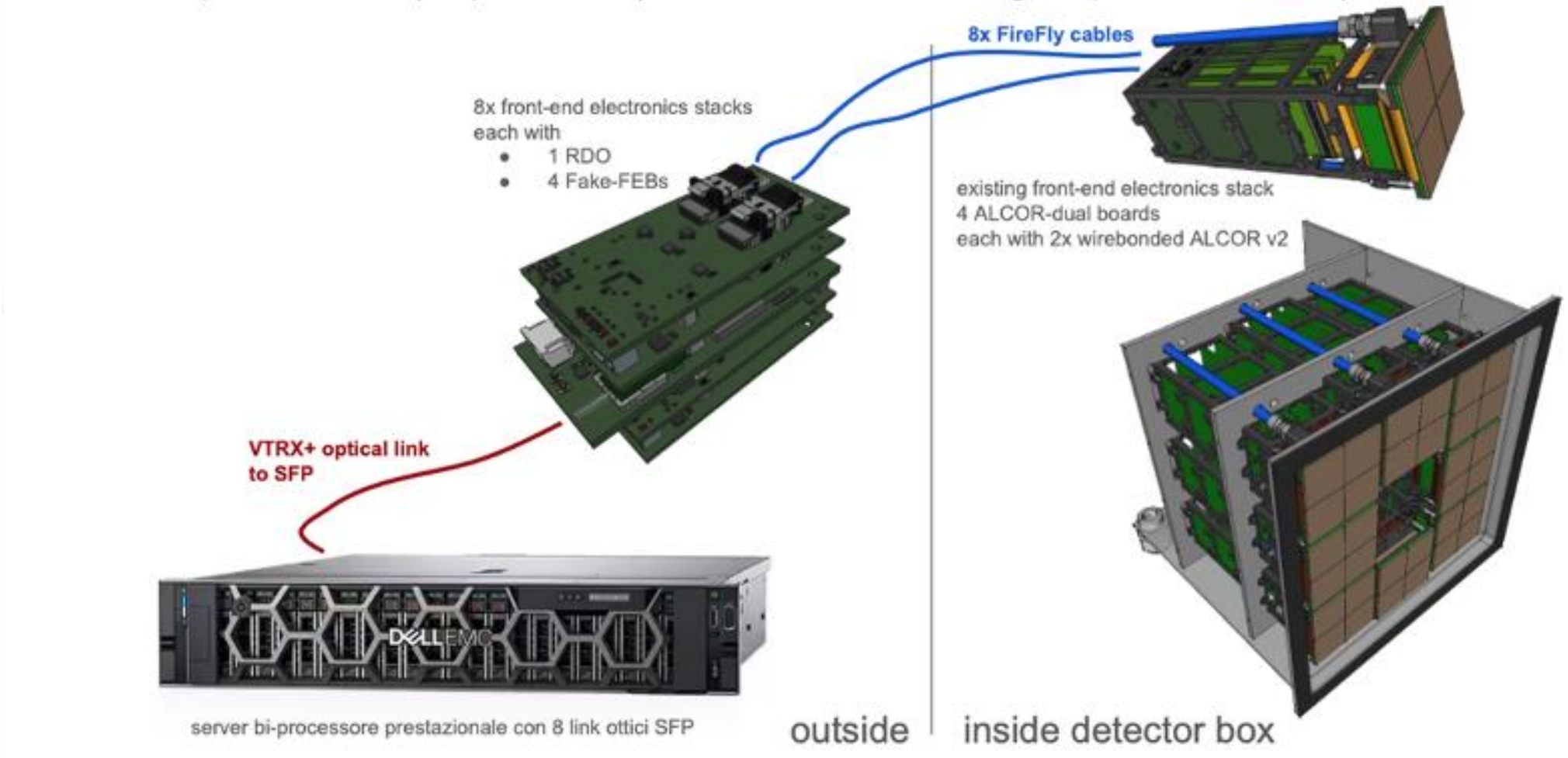
Credits: many colleagues in Turin, Bologna, Rome: F. Cossio, G. Dalla Casa, D. Falchieri, C. Ferrero, O. Frezza, S. Geminiani, F. Lo Cicero, A. Lonardo, M. Panza, L. Pontisso, L. Rignanese, C. Rossi, G. Torromeo, P. Vicini, …

Questions


BACKUP

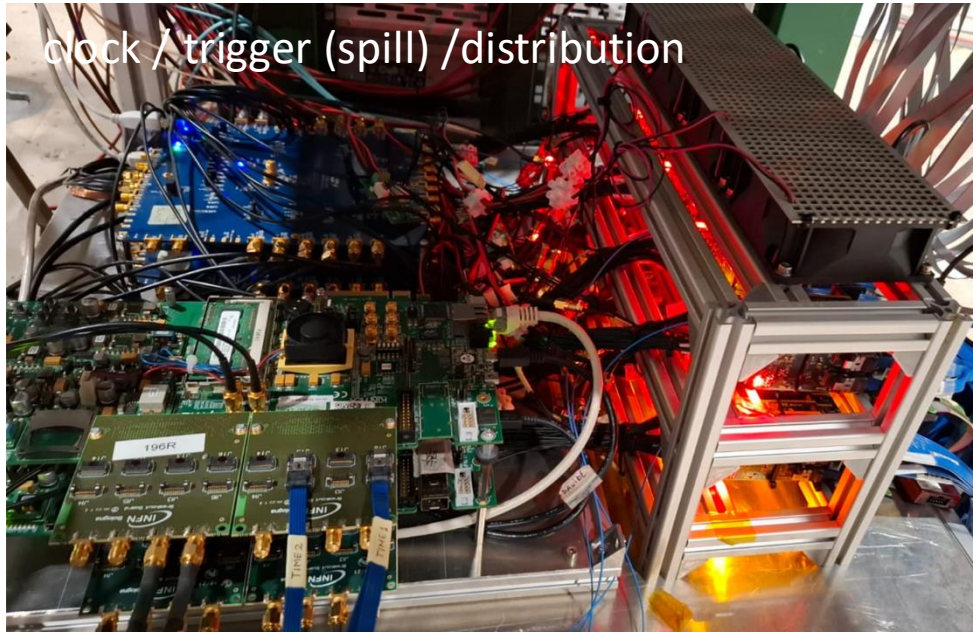
RDO test beam setup

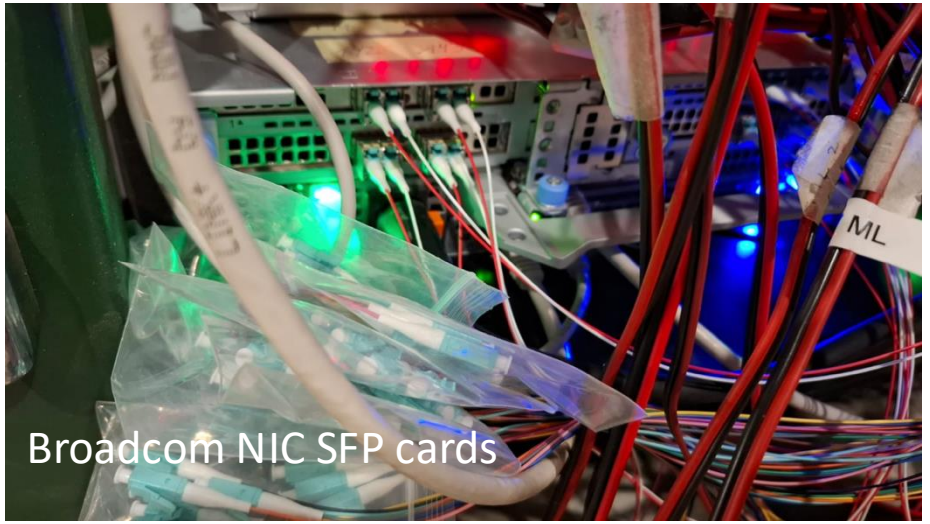
- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- "fake-FEB" (ALCOR v2.1 adaptor) : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)



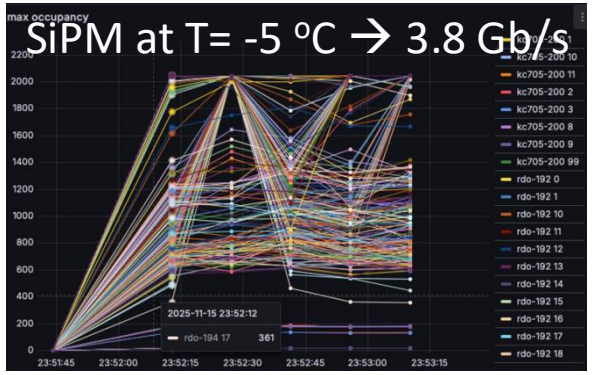
RDO test beam setup (2025)

dRICH protoype in Bo-Lab
with RDO "crate"





streaming DAQ: data-push to RDO FIFO then IPbus



T=-35 °C → T=-5 °C
DCR increases
mimic radiation damage

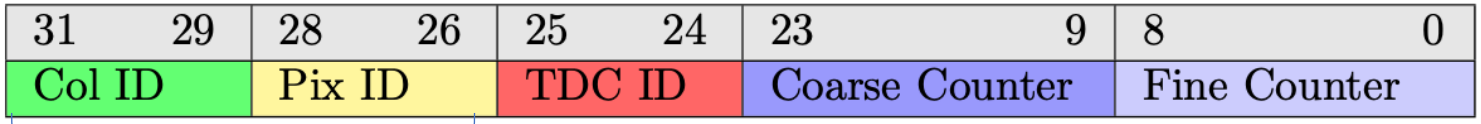
full setup @ SPS

(for general dRICH test beam results see M. Giacalone @TB2024)

ALCOR data (raw) and ePIC data (I)

ALCOR hits "event word" are timestamps

accelerator BC: bits 23 – 11



3 bits to identify the column (LVDS TX lane) [0 to 7]

3 bits to identify the pixel [0 to 7]

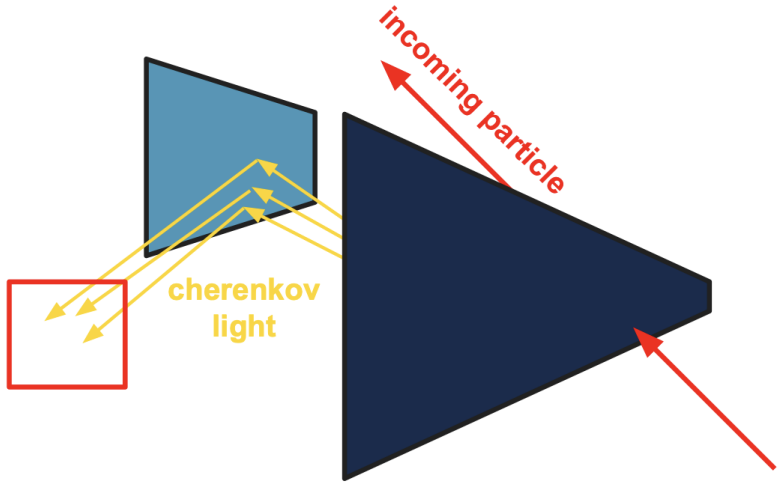
4 TAC TDC IDs: 2 bits
→ 2 TDCs for leading edge
→ 2 TDCs for trailing/slew rate

these nine bits are the measurement of the TAC
you can reach 20-40 ps LSB at 394 MHz.
Calibration needed → can't be used at DAM level

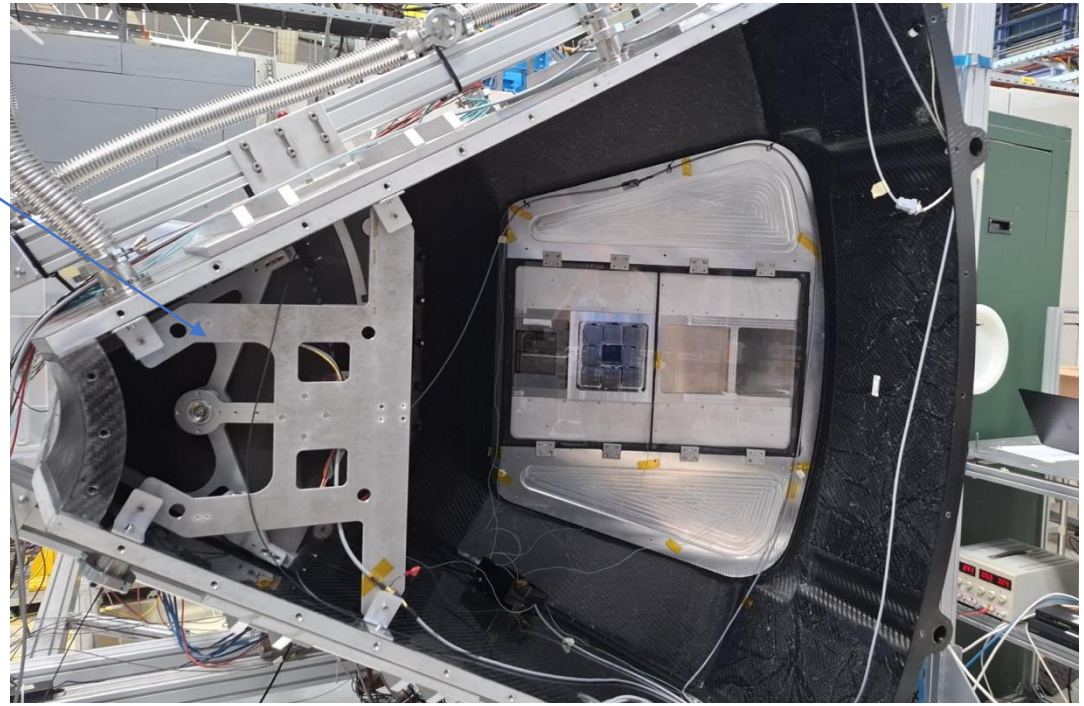
394 MHz → coarse counter LSB 2.54 ns (currently 320 MHz → 3.125 ns)
15 bit coarse counter (0x7FFF = 32767)

Coarse counter expires every 83.228 µs > 12.78 µs (EIC orbit)
At each EIC orbit we get a RevTick signal from DAM (main EIC "synch")
→ this trigger a coarse counter reset and a frame structure injected in data flow

CERN PS 2026 test beam setup



MIRROR



dRICH throughput modelling (I)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM	30
Input link in DAM	42
Output links from DAM to TP	1
Number of DAM Trigger Processor	1
Input link to DAM Trigger Processor	30
RDO-DAM Link Bandwidth (VTRX+) [Gb/s]	10
DAM to Echelon-0 Switch Bandwidth [Gb/s]	100
dRICH Interaction tagger reduction factor	1
Interaction tagger latency [s]	1,00E-04
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	(if you put 10 ns == no shutter)

There are two reduction handles in this table:
- the shutter
- something external (can be NN on DAMs, dIT or ..?)

dRICH backend DAQ reorganized following studies from INFN Rome (see next slides) from 27+1 to 30+1 FLX-155: 30 DAMs + 1 Trigger Processor (TP)

Reduction factor via shutter
RF = 10 ns/(shutter width)

Reduction factor provided by whatever external trigger (including NN on dRICH DAMs)

dRICH throughput modelling (II)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	1		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	2	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

This is worst case!

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	55,20	800,00	
Throughput to serializer [Mb/s]	34,50	788,16	
Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
Input at each DAM [Gbps]	45,28	420,00	
Buffering capacity at DAM [Mb]	4,64		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	1.358,44	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

*Take home message

Using only the shutter with a reduction factor 5 (2 ns over 10 ns BC) we keep 1.3 Tbps throughput and we stay within all limits (including transfer from DAM to Echelon-0)

dRICH throughput modelling (III)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	5		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	10	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	276,00	800,00	
Throughput to serializer [Mb/s]	172,50	788,16	
Throughput from ALCOR64 [Mb/s]	1.380,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	5,39	10,00	based on VTRX+
Input at each DAM [Gbps]	226,41	420,00	
Buffering capacity at DAM [Mb]	23,18		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	6.792,19	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

10 ns means no shutter

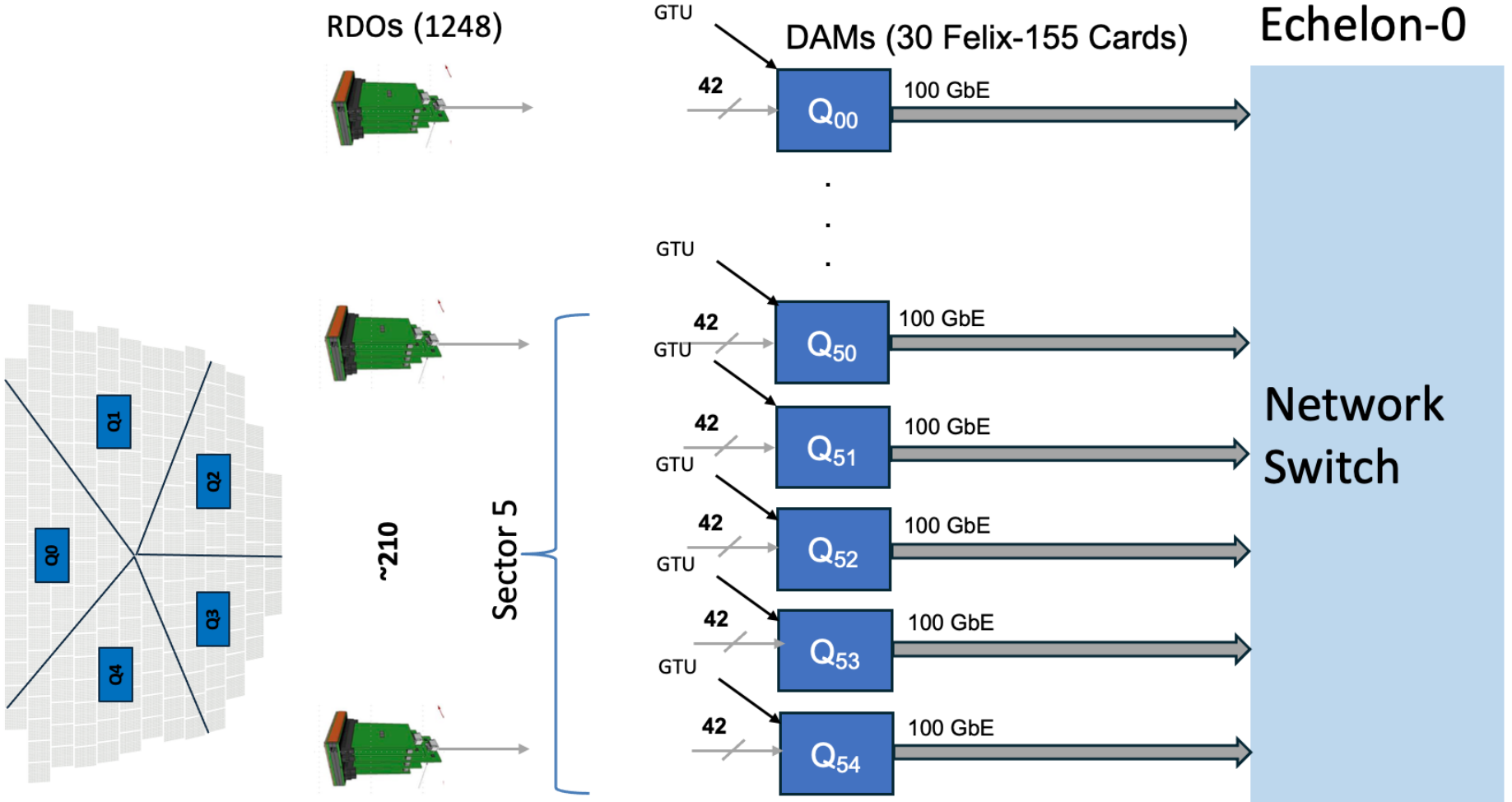
data reduction via "another method"

further risk mitigation here might be applied using two TX links instead of one

*Take home message

If shutter is not effective we need a reduction factor 5 from a dRICH interaction tagger method and we stay within all limits (including transfer from DAM to Echelon-0)

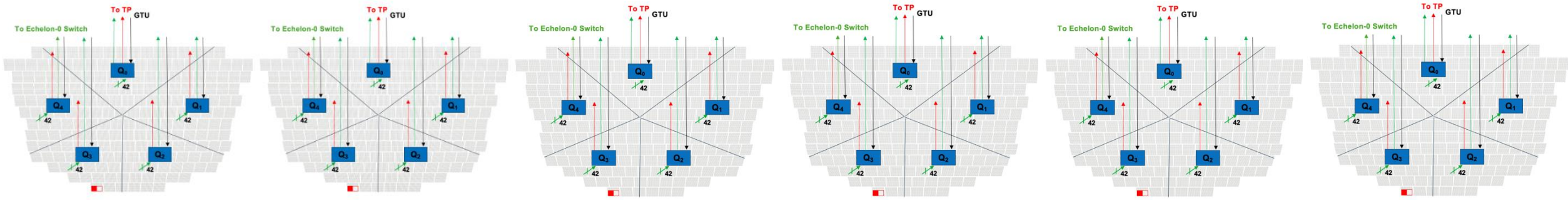
dRICH DAQ: the backend

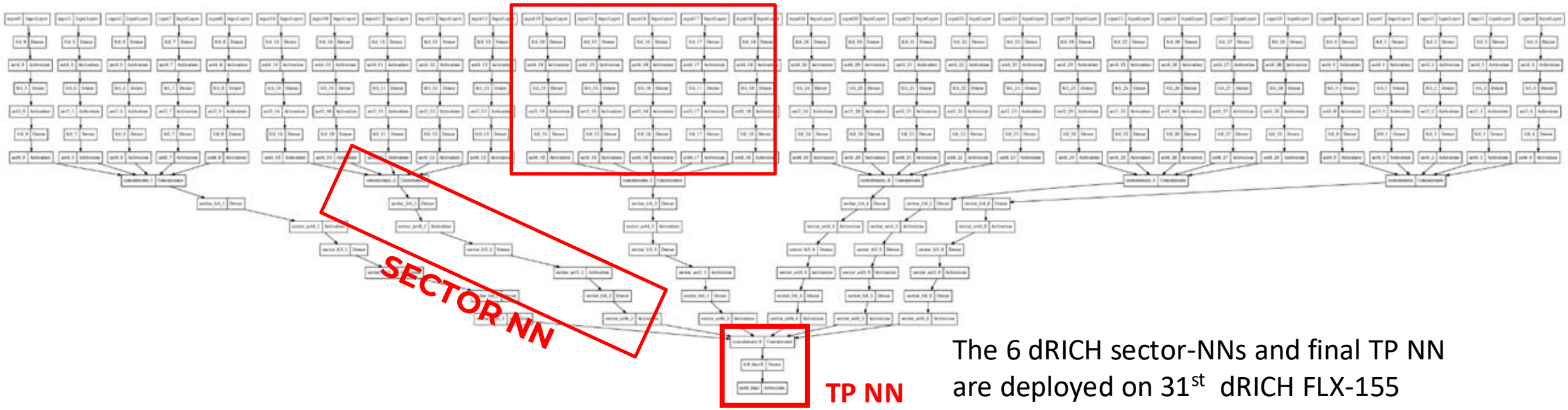


[ML for data reduction in DAMs](): C. Rossi @RICH2025

NN deployment model and DAMs

6 dRICH sectors – 5 DAMs/sectors





The 6 dRICH sector-NNs and final TP NN are deployed on 31st dRICH FLX-155

dRICH RDO requirements

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus towards FEBs
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- **opt. tranceiver** must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps