BTOF stavelet assembly plans

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On behalf of SCIPP and ePIC TOF

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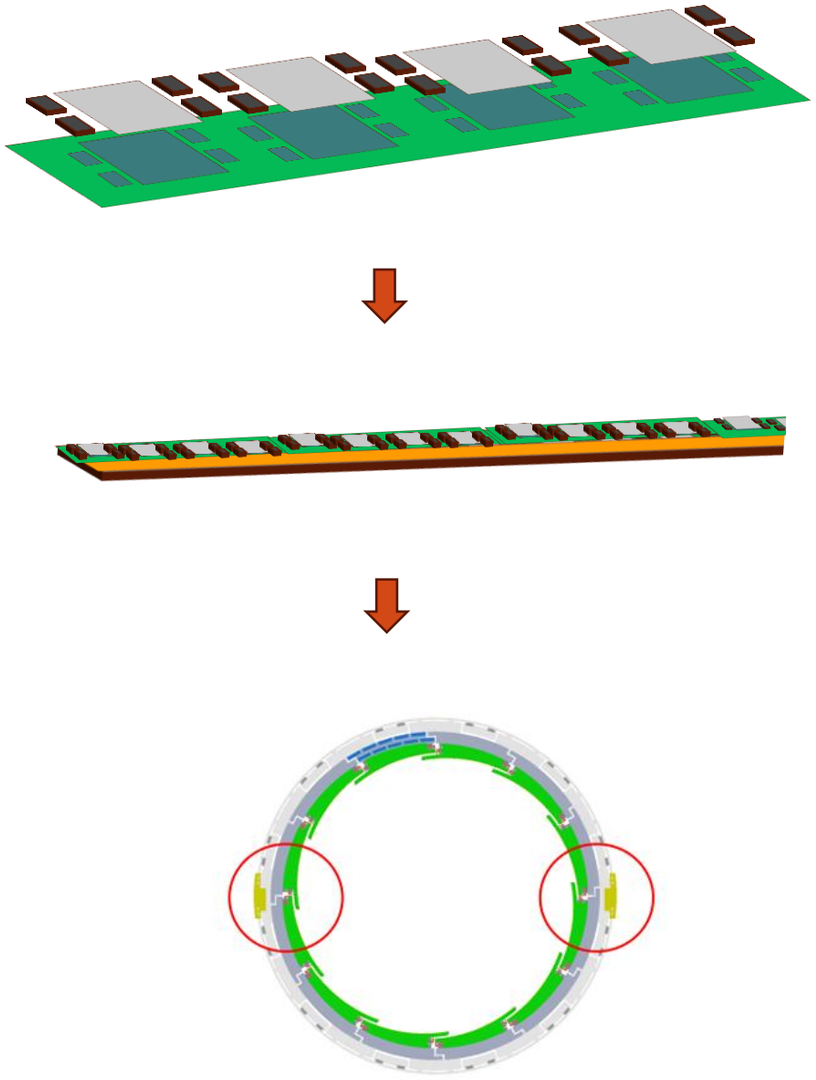
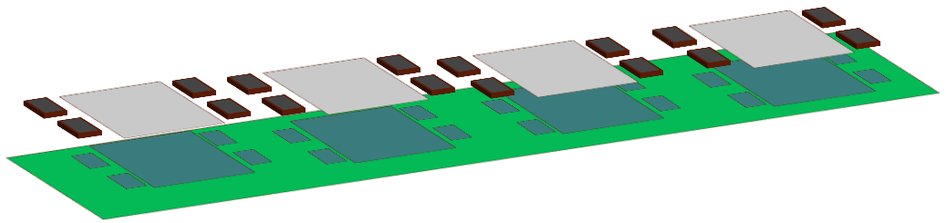
The assembly procedure and sites

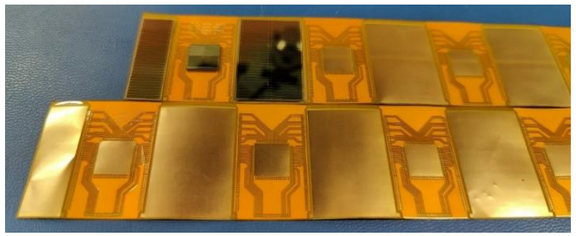
- The assembly is divided in modules (stavelets) assembly, stave assembly (stave) and final integration
  - Stavelets' assembly sites: UCSC, Hiroshima, Riken, Taiwan NCU
  - Staves' assembly sites: Purdue/BNL
  - Final integration: BNL
- Stavelets modular design was decided ~1.5 years ago for these reasons
  - Allow multiple sites which can assemble small (~3x16cm) components with complicated loading and wire-bonding using existing ATLAS/CMS equipment
  - Increase assembly yield with modular design
  - Ease of shipment to Staves assembly sites
- QA and QC is done at different levels
  - At sensor and ASIC single dies level, simple electrical (e.g. sensor IV)
  - FPC and interposer, trace impedance etc.
  - On assembled stavelet, electrical and telemetry
  - On assembled stave, electrical and telemetry

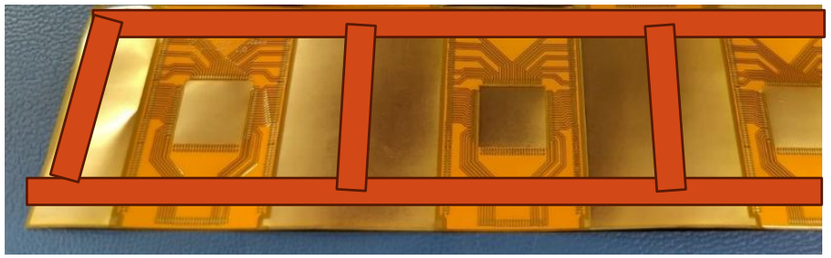


The stavelet

- The stavelet is a thin copper FPC (1-layer, might need 2-layers) to support the sensors and ASIC assembly
  - Large HV pads and return capacitors for the HV
  - Temperature sensors for monitoring
  - Traces to connect ASIC with FPC
- Can use stiffener on the perimeter to provide support and glue thickness
- Exploring other materials as well, e.g. thin ceramic (rigid, but higher material)
- 150um or better tolerance for sensors to ensure overlap



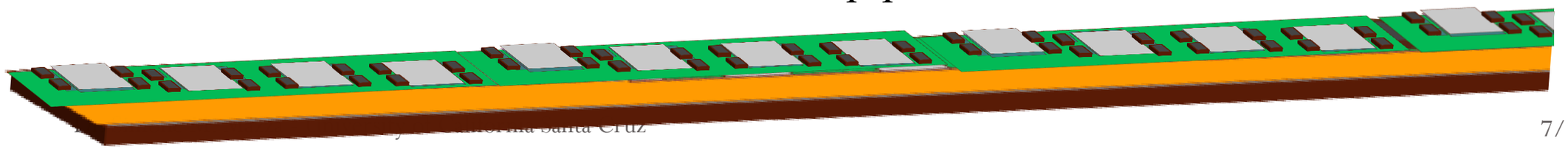




Stiffener (e.g. 50-100um Kapton)

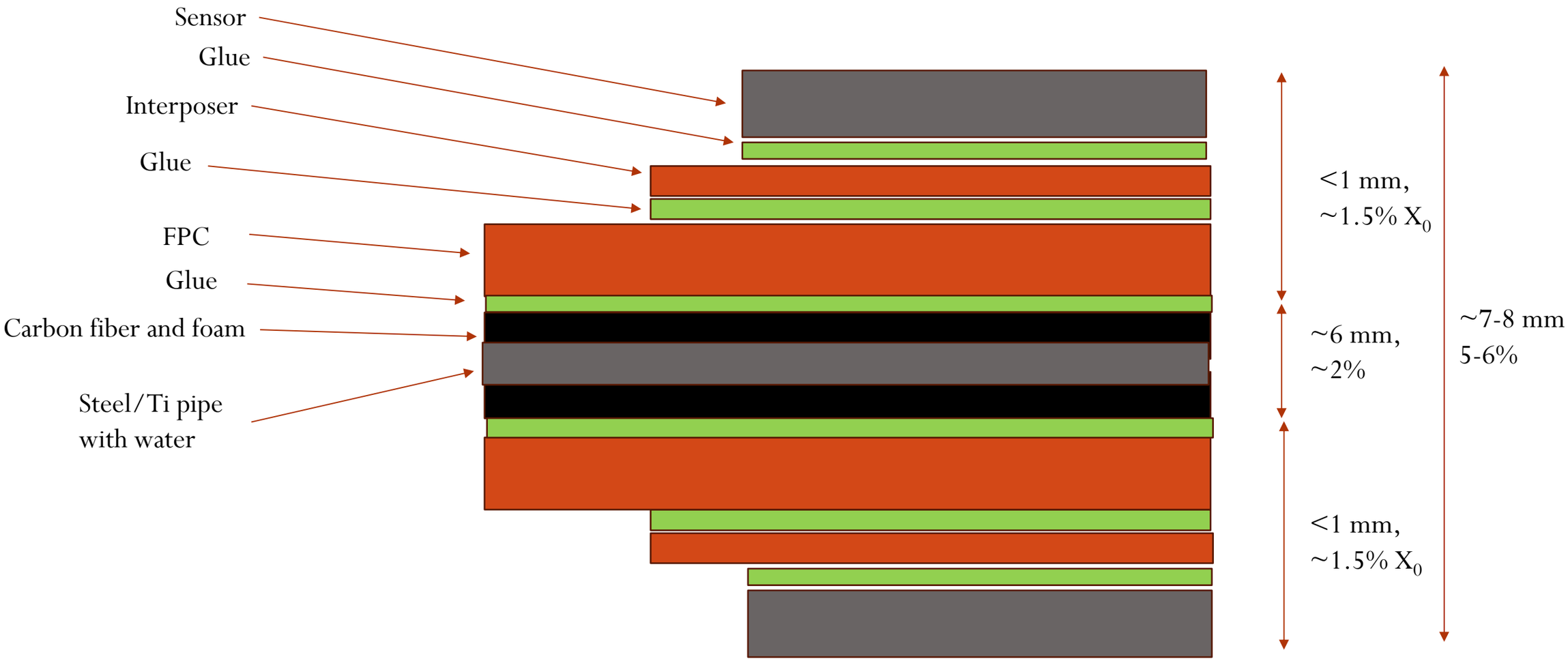
The stave

- The stave is double-sided (components on both faces) to have 100% coverage
  - Inner core is carbon honeycomb with cooling pipe slot
  - Steel pipes for cooling in-n-out on service's end with loop on the other side
  - Carbon plies and epoxy form the support for FPC which is co-cured or co-bonded on the hard support
  - Each side is fabricated and co-cured separately
- Stave composed by 7 stavelet and Service Hybrid on the service's end
- No change in stave design since December, except for stavelet design
- Sensors and ASICs are glued and wire bonded to interposer boards (green)
  - ASIC have an opening under it in the FPC to allow direct thermal connection with thermal paste
- Interposers boards are glued and wire bonded to FPC
- The two sides of the stave are sandwiched with pipe to fabricate final stave

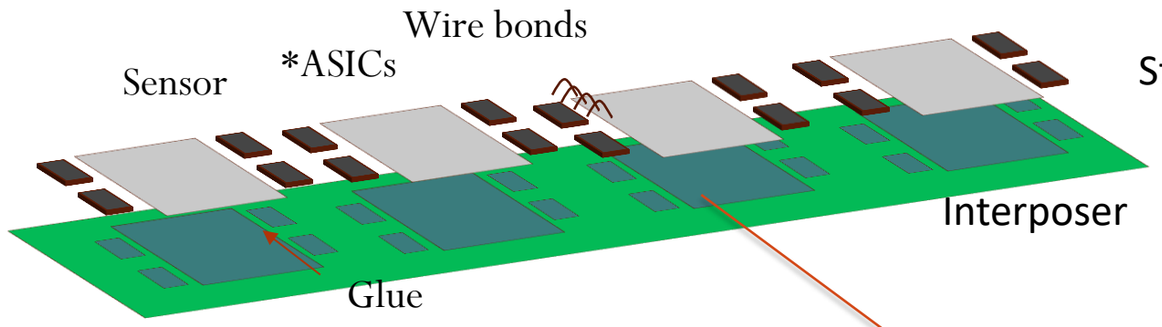


Cross section of assembled stave

- Thickness: 2*[(200um Si (sensor) + 50um glue) + (25um copper, 50um Kapton) + 50um glue + (72um copper, 225um Kapton) + 50um glue + (1500um Carbon fiber)] + 2000um pipe plus water = ~7-8 mm → averaging ~5-6% X_0
- Simulation results indicates ~6% X_0 for material budget is ok



Double-sided stave design



Service Hybrid

Stave Front

Glue

Half-stave

Co-cure

FPC

Carbon fiber

Co-bond

Cooling pipe and return (10-20C)

Co-bond

Carbon fiber

Co-cure

Service Hybrid

Glue

Stave Back

FPC

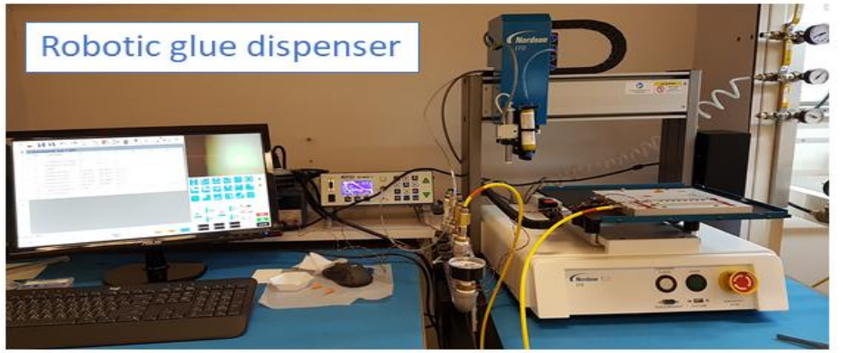
Half-stave

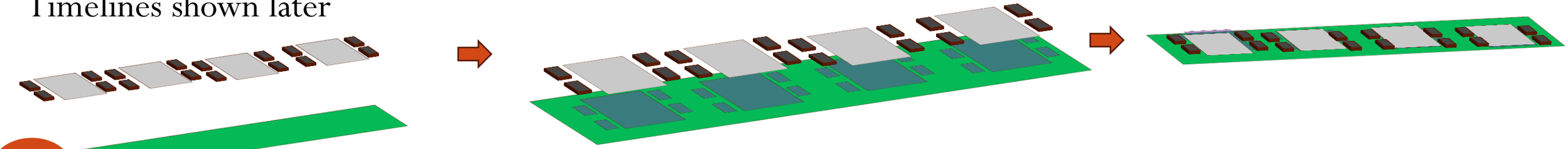
*ASICs placement is slightly different after update in baseline

Details of stavelet assembly

- Step 0: QC on components (e.g. sensor IV), might use 'certified components' from other sites
- Step 1: Glue deposition on the interposer is done with glue robot (gantry with precision deposition, same as ATLAS)
  - Glue: either UV or bi-component silver epoxy, TBD
- Step 2: Components (ASICs, sensors) are picked up with precision vacuum jigs and deposited on interposer, jigs close and set aside for curing
  - Hole under ASIC filled with thermal paste for better thermal connection
- Step 3: After curing, telemetry to verify components position
- Step 4: Sensors are ASICs are wire bonded to interposer, optional encapsulation or potting
- Step 5: QC testing station (sensor IV, ASIC, charge injection)
- Step 6: Ship to stave assembly site

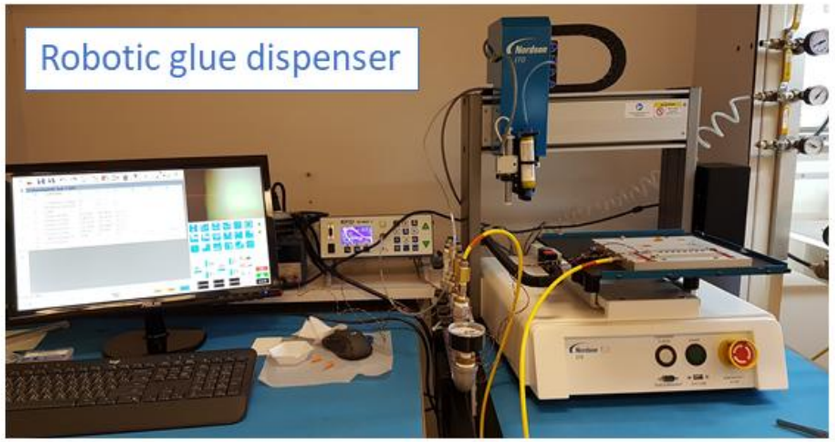
Timelines shown later

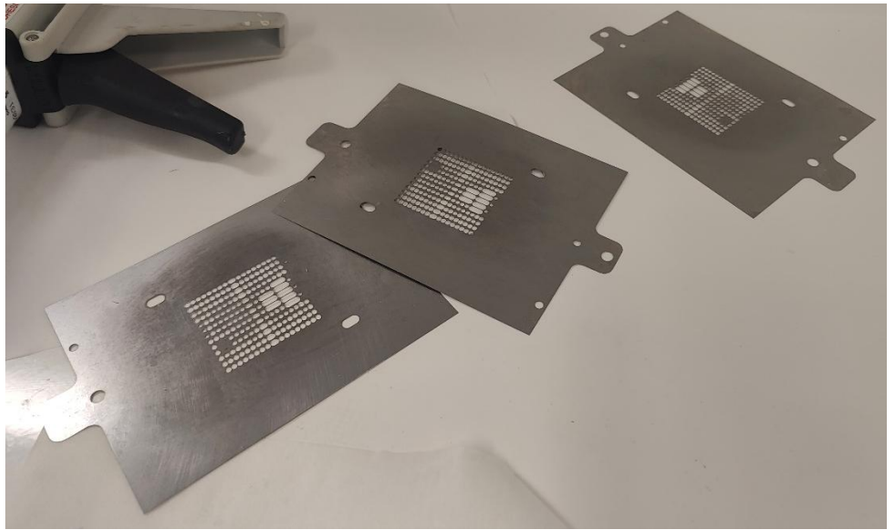


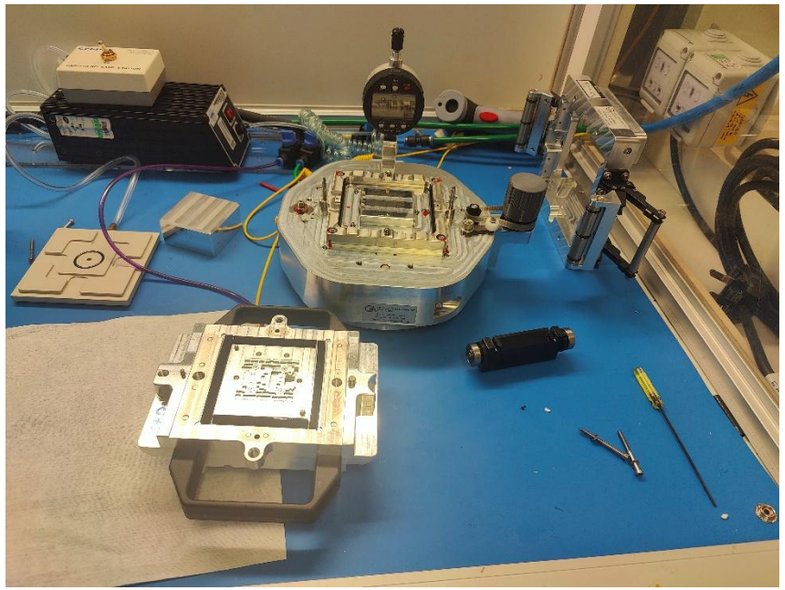


Glue deposition

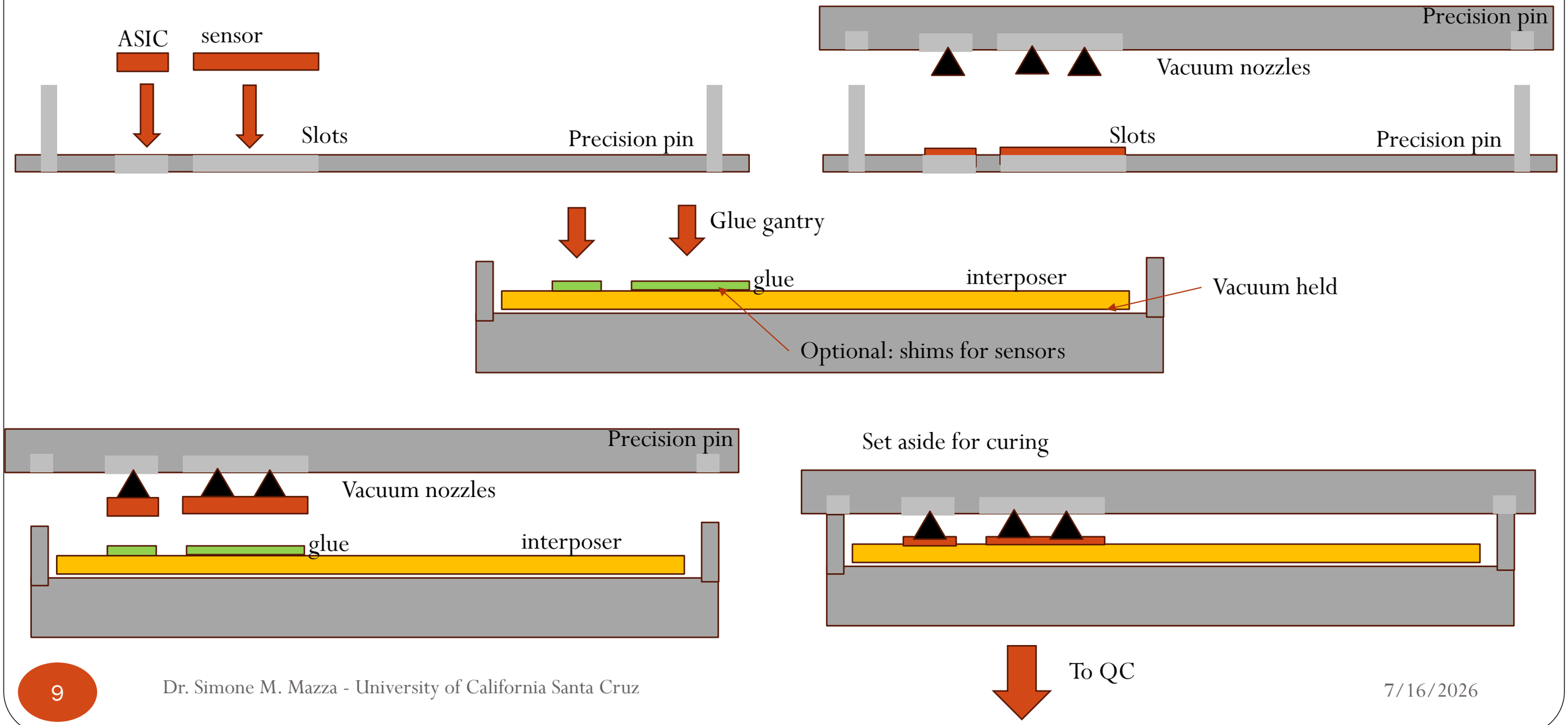
- Another option: glue panning (Itk pixels)







Stavelet jigs and equipment



Metrology and QC

- After curing the stavelet will be measured with SmartScope, metrology output goes to database
  - Component positioning with few um precision
- Stavelet is wire bonded
- Verify wire bonds pull, on stavelets at preproduction QA level and on samples at production QC

- Stavelet goes to QC 'box' for charge injection on all channels (to be designed and built)
- Needs simulation to determine impact of different scenarios. E.g. 1% dead channels (1 dead channel ~1mm x 1cm dead region) impact on overall performance

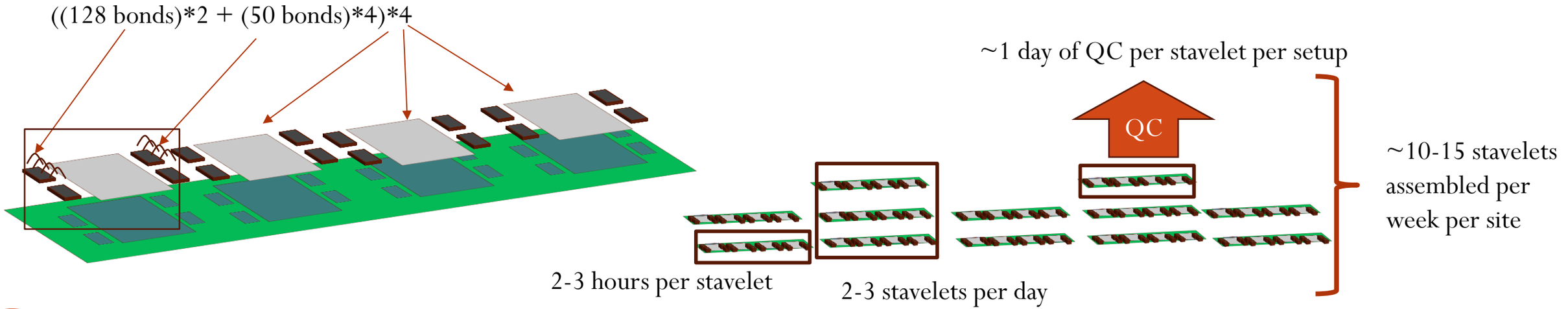
Assembly time of one stavelet

- Glue placement: 20 minutes
- Component placement: 20 minutes
- Glue cure: UV 5-10 minutes, bi-component 12h, thermal ~1h
- QC on glued component: 30 minutes (metrology)
- Wire bonding: 60 minutes
- Full time: ~2-3h per stavelet (minus long glue cure time)
- Can organize work with high parallelization (e.g. glue deposit on a jig with multiple stavelets)
  - 2-3 stavelet per day → possible

- **Likely QC will be most time consuming**
- Will design temporary service hybrid that clamps or connects to the stavelet
- QC on full stavelet: few hours, need to excite all channels with enough statistic
  - Assuming 1 stavelet QC per day, squeezed in 1.5 year, need 3-4x QC station per institute
  - Or could expedite with other institutes involved in stavelet QC

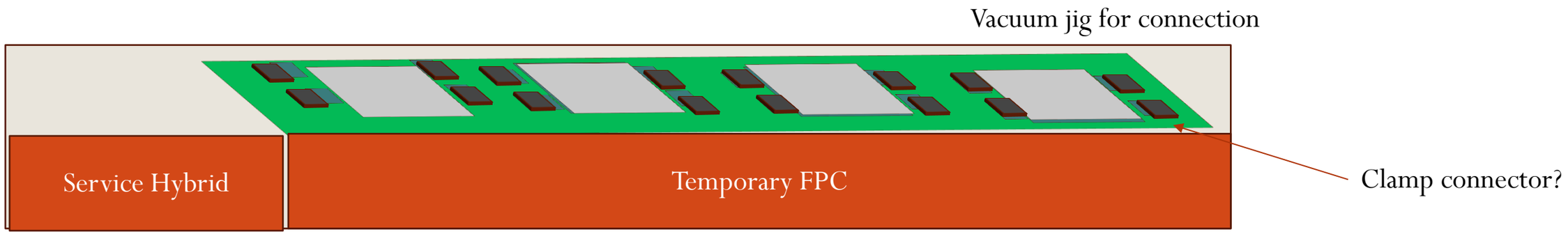
Stavelet production volume

- Volume: 144 staves, 288 half staves made of 14 stavelets (top and bottom)
  - Wirebonds per stavelet: (128x2 (sensors→ chip) + ~50(chip)x4)x4 → ~1500 bonds.
  - 4032 stavelets +10-20% yield adjustment, ~5000 to assembly in 2 years
  - Assuming 4 BTOF assembly sites: ~1250 stavelets per site in 2 years, ~2-3 stavelet per day → possible
- This is assuming production ramp up without issues
- <u>ATLAS ITk strip (similar size and complexity) has a rate of ~4 modules per day (20 per week)</u>

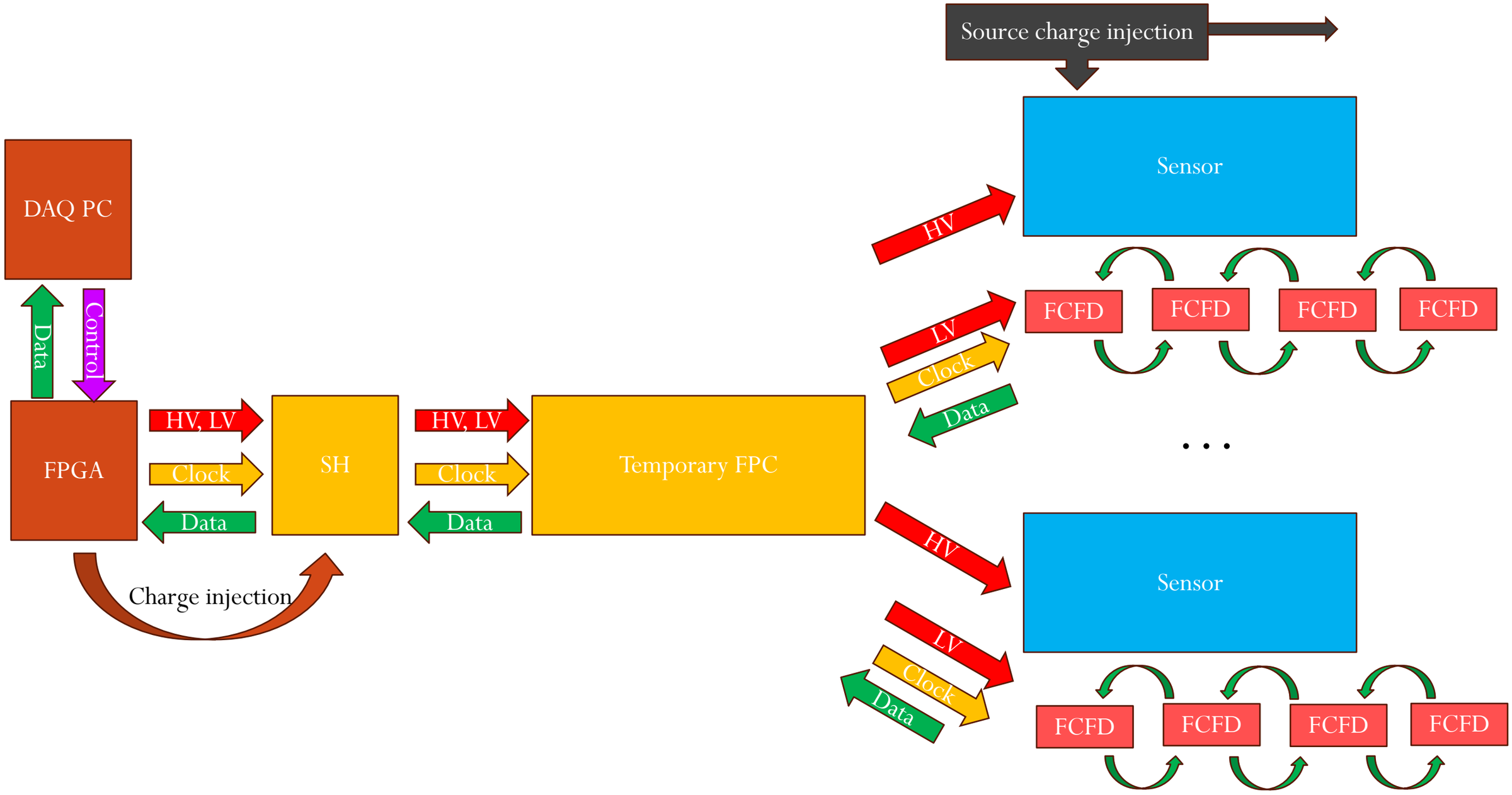


Stavelet QC station

- Developing SH ←→ stavelet direct connection for QC



Will look similar to demonstrator setup


Source charge injection
DAQ PC
Data
Control
FPGA
HV, LV
Clock
Data
SH
HV, LV
Clock
Data
Temporary FPC
Charge injection
Sensor
HV
LV
Clock
Data
FCFD
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Sensor
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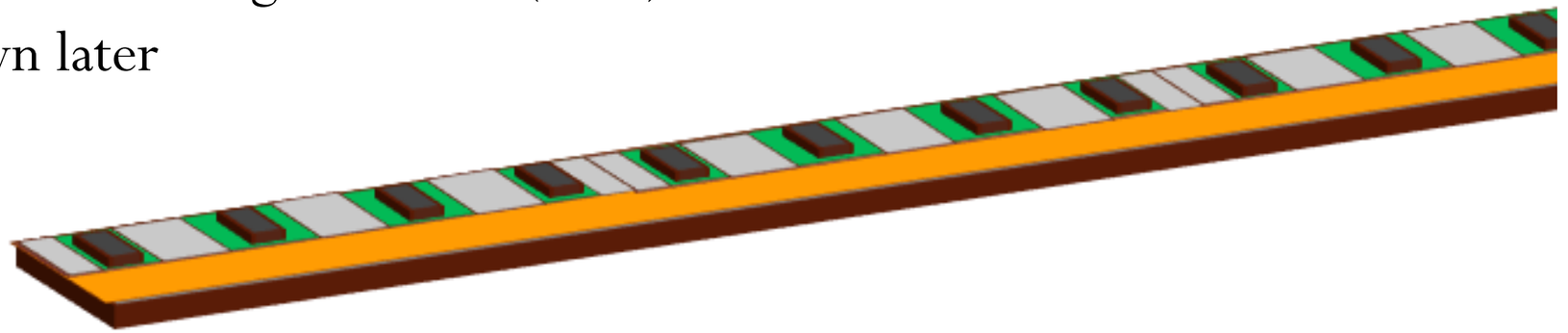
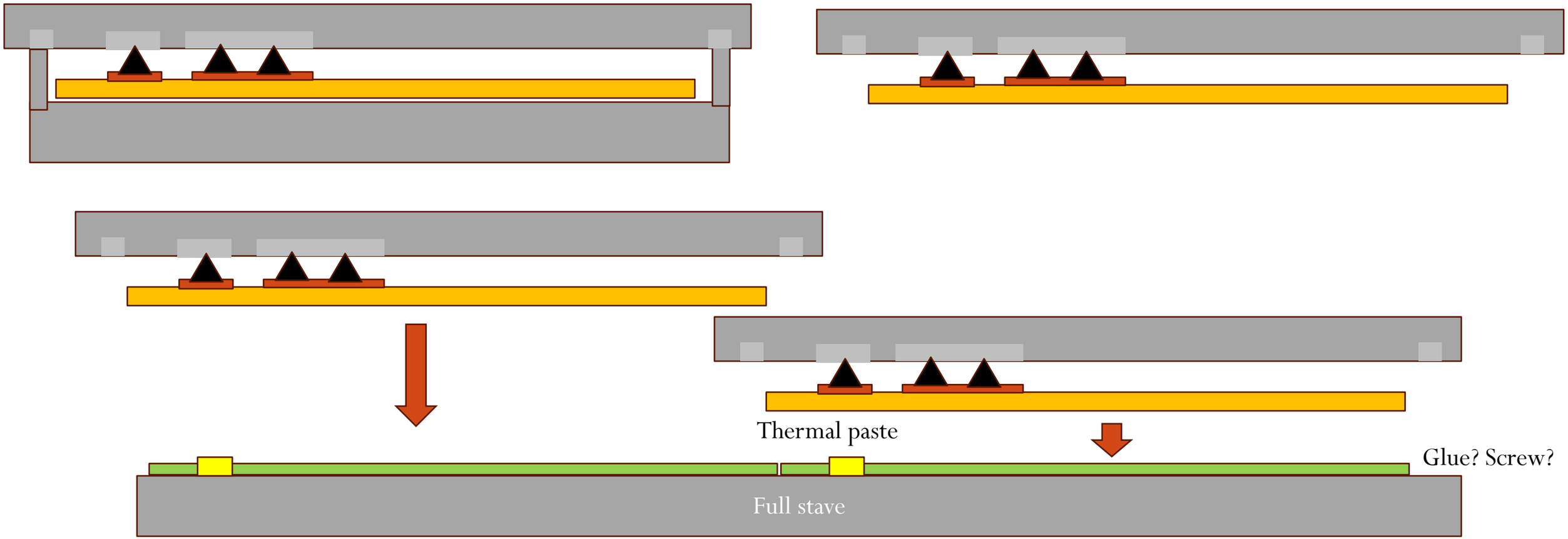
Details of stave assembly

- Step 0: prepare stave (co-cure or co-bond FPC with stave support), load Service Hybrid
- Step 1: received assembled stavelets
- Step 2: glue stavelets on half stave
- Step 3: final wire bonds (~20 per stavelet) (or using connector)
- Step 4: QC on half stave, telemetry, electrical → need custom telemetry for large objects (e.g. similar one was built at BNL for ATLAS)
- Step 5: sandwich stave
- Step 6: QC on full stave, telemetry, electrical
- Step 7: ship to final integration site (BNL)

Timelines shown later

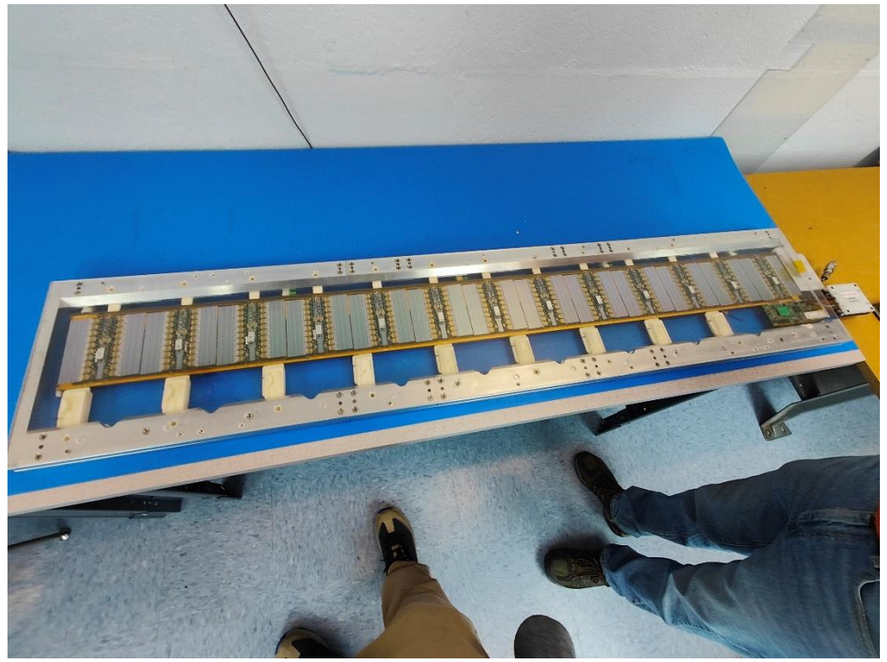


Stave jigs and equipment



Metrology and QC

- After assembly of stave will need to verify module placement and back-front alignment
- Need specialized QC station, object is too big for standard metrology stations
- Existing at BNL, developed for ATLAS ITk
- QC is with actual service hybrid on the stave

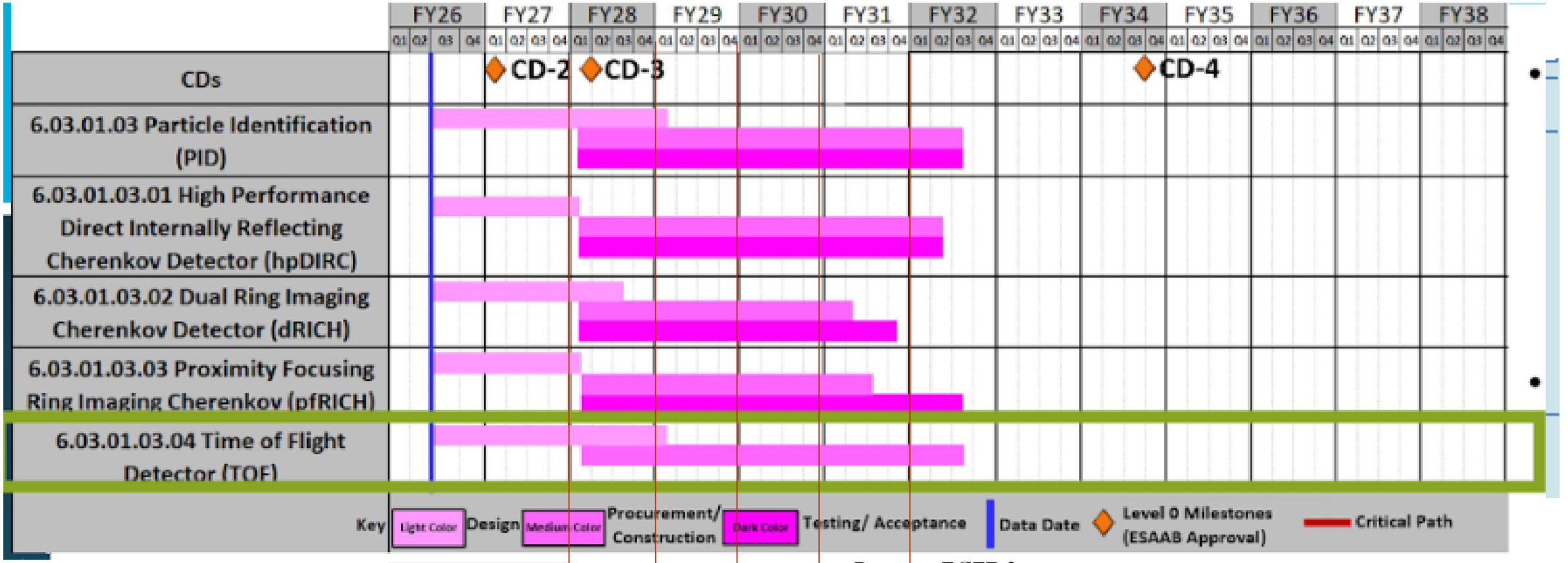


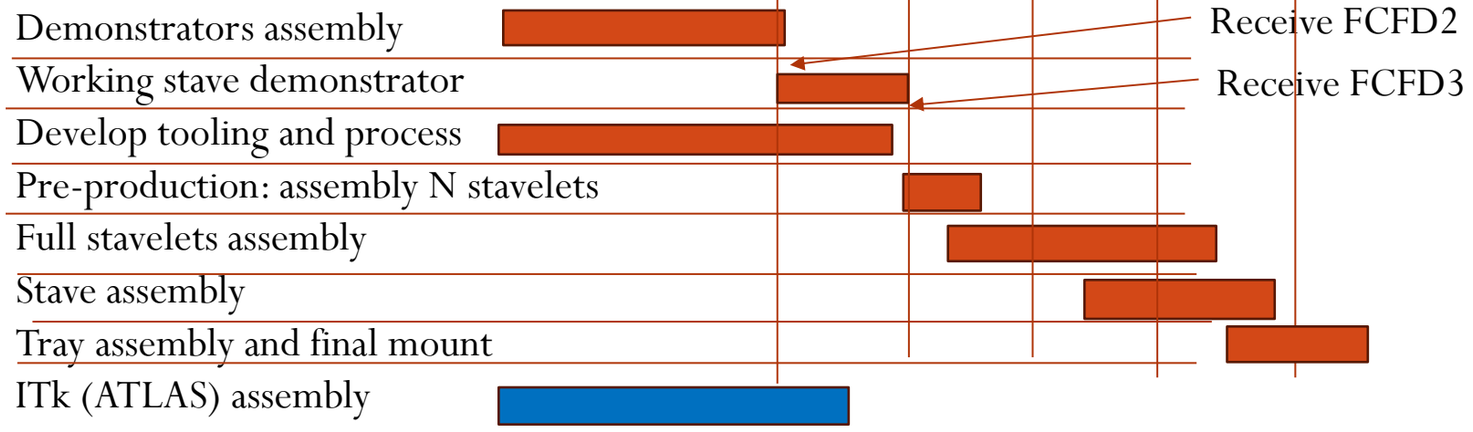
Assembly time of one stave

- Glue placement: 60 minutes
- Component placement: 30 minutes
- QC on glued component: 120 minutes (metrology)
- Wire bonding: 60 minutes
- Full time: ~4-5h per stave (minus long glue cure time), one per day?

- 144 staves (160 with yield) → ~1 year
- QC on full stave, verify ASIC response (quicker)
  - At pre-production QA do more extensive tests

BTOF road-to-assembly





Institutes involved and roles - assembly

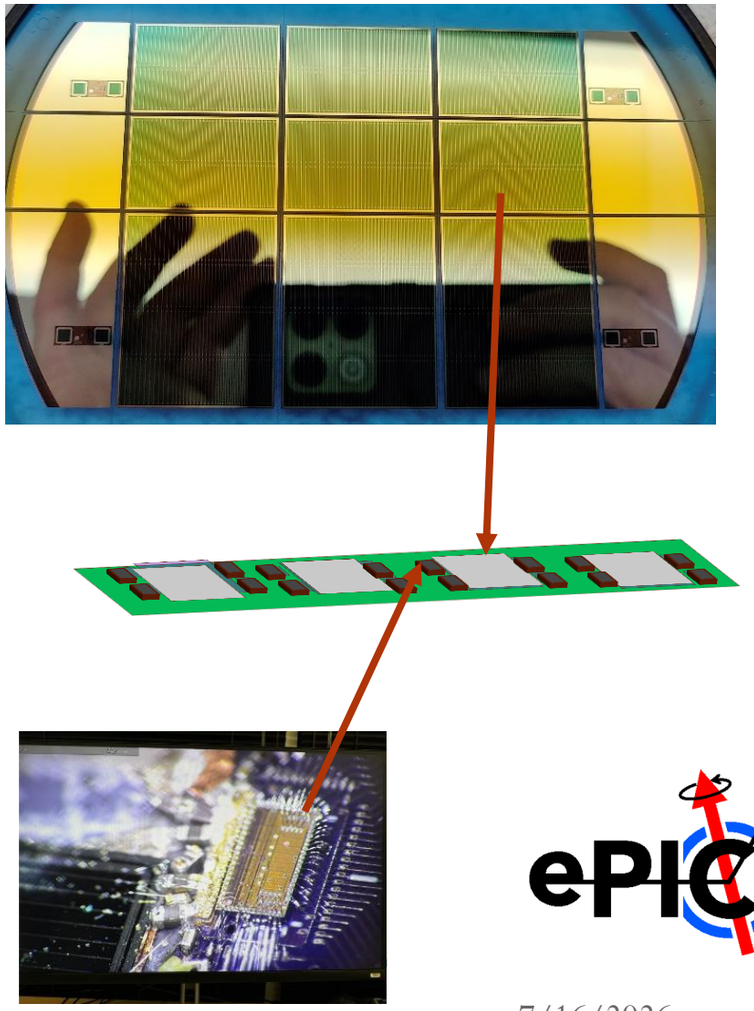
- Hiroshima – ASIC, sensor, FPC sample QC, stavelet assembly and QC
- Riken – ASIC, sensor, FPC sample QC, stavelet assembly and QC
- UCSC – ASIC, sensor, FPC sample QC, stavelet assembly and QC
- Taiwan NCU – ASIC, sensor, FPC sample QC, stavelet assembly and QC

- Purdue, BNL – Stave production, final stave assembly and double-side gluing
- Purdue, BNL – Stave QC

- BNL – Tray assembly and final BTOF assembly

Conclusions

- The loading procedure is outlined, and institutes roles are defined
  - Might need more institutes for the final assembly and QC
- ePIC BTOF module assembling is proceeding with multiple prototypes
  - Gluing trials
  - Jigs design
  - Assembly procedure tests
  - Thermal tests
- Expect a first ‘demonstrator’ soon and will repeat the process afterwards for multiple stavelets and a full stave
- Working on setting up the database



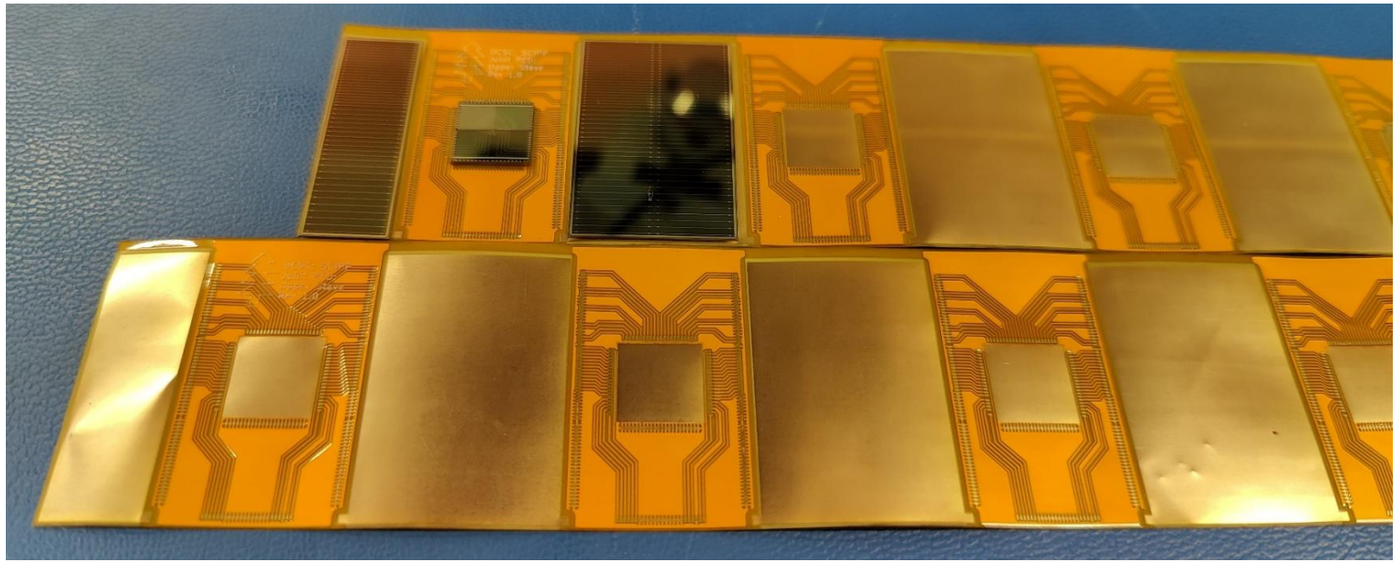
Backup

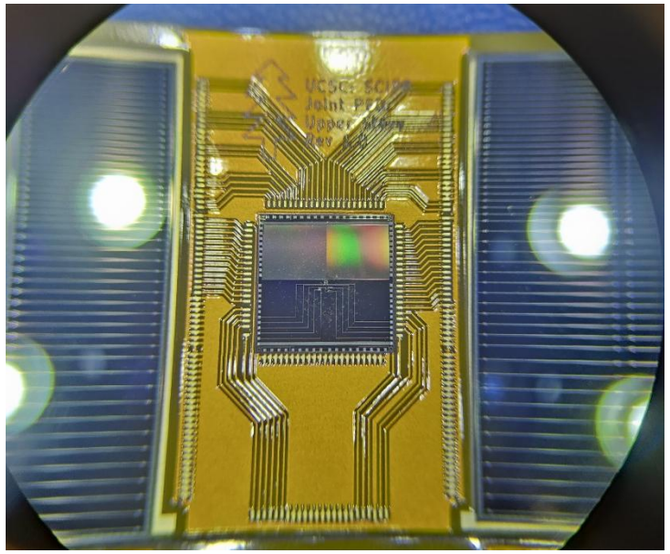
Prototyping status

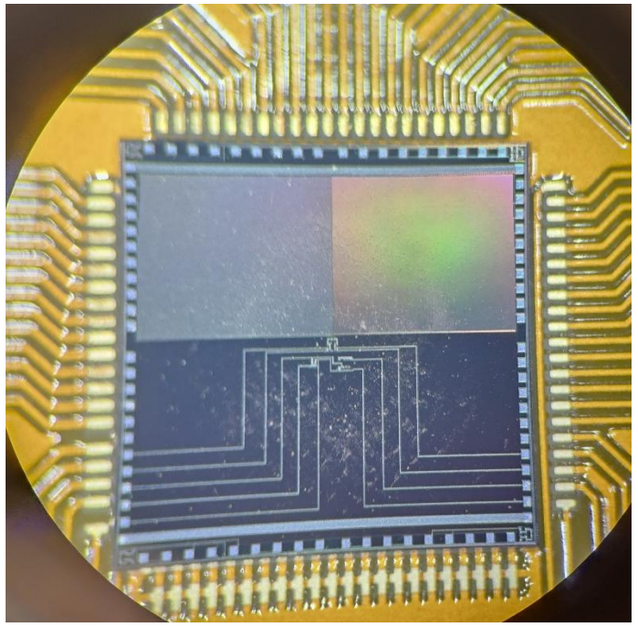
- Fabricated first interposer prototype ✓
- Fabricated first short FPC with connections ✓
- Co-cured and Co-bonded FPC prototype with carbon fiber ✓
- Fabricated first jigs for loading (3D printed) ✓
- Identified a few glues and performed gluing trials ✓
- Loaded first interposer with few components and mockup ASIC, thermal tests ✓
- Simulated long FPC ✓

Stavelet demonstrator

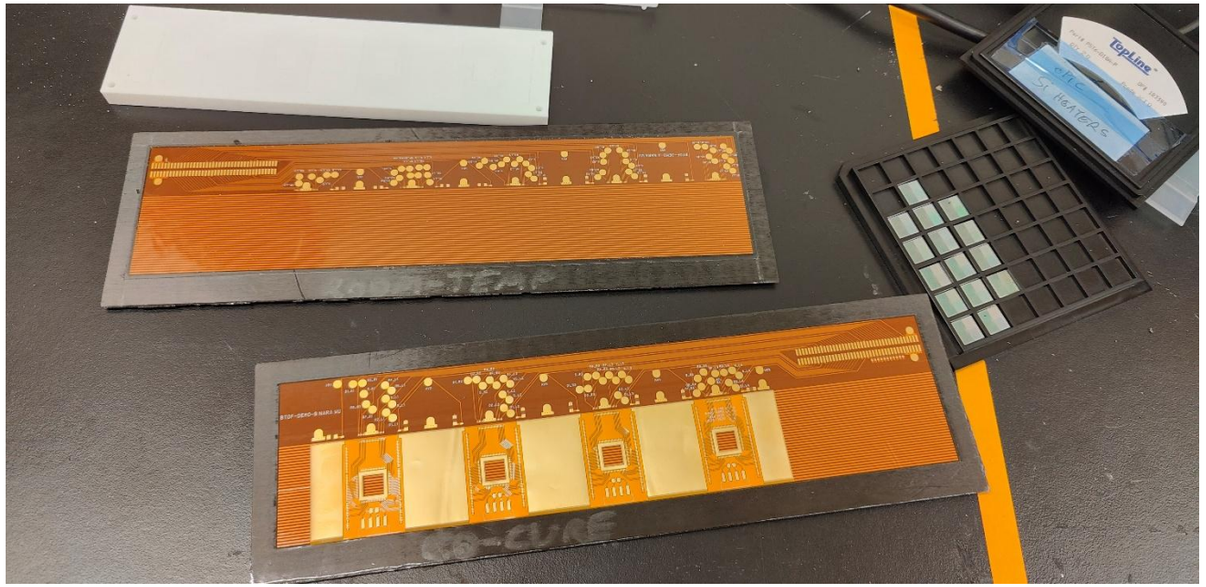
- First prototype of interposer board produced
  - Using non-working detectors from the HPK production
  - Si heaters to simulate ASIC
- Goal: fully load a double-sided stavelet with active pipe cooling and check thermal dissipation in prototype
  - Perform telemetry on the stavelet

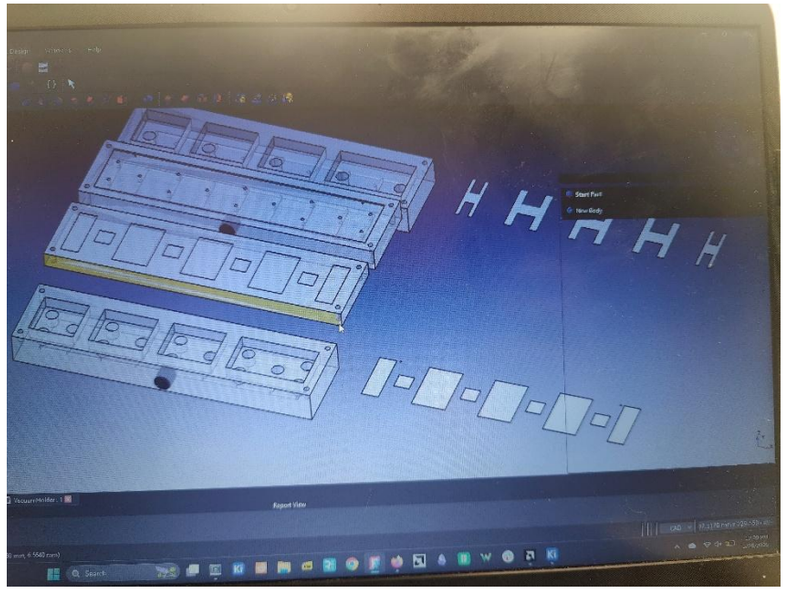






Loading jigs and co-cured FPC and stave

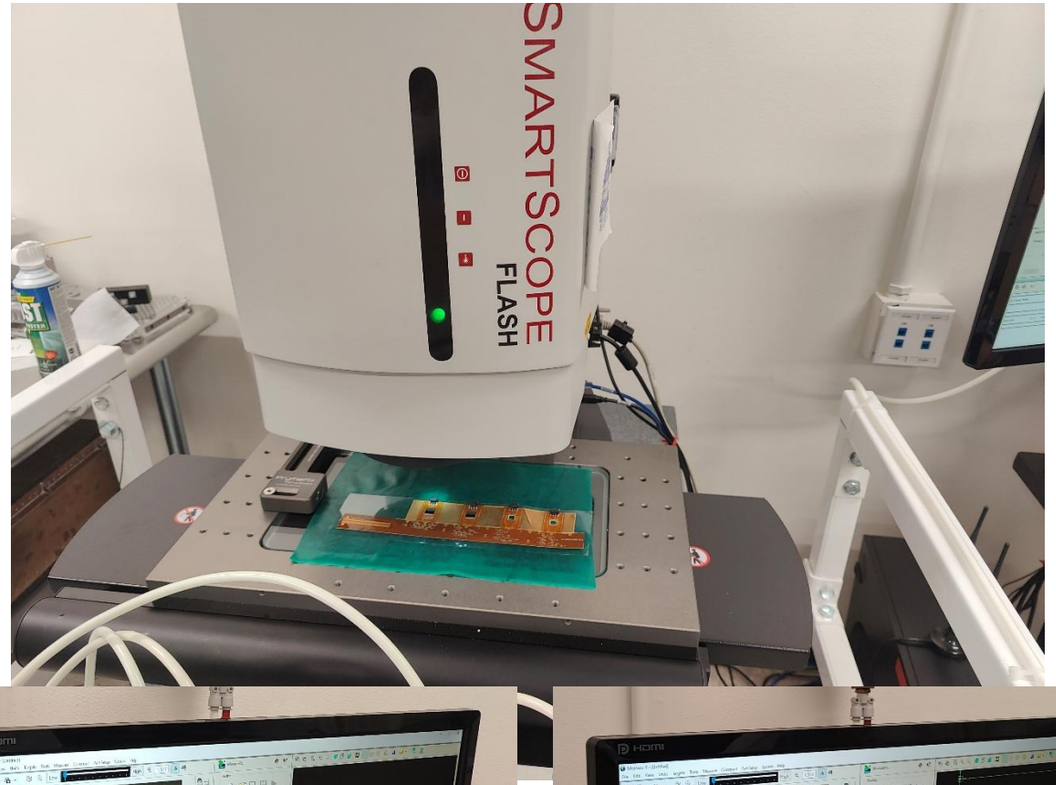


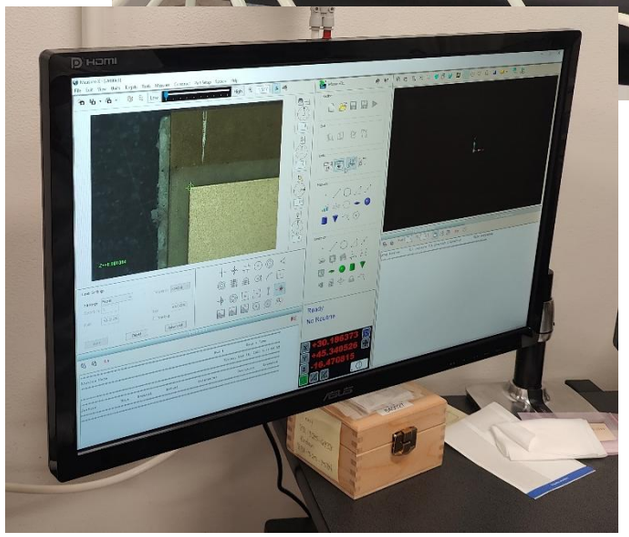


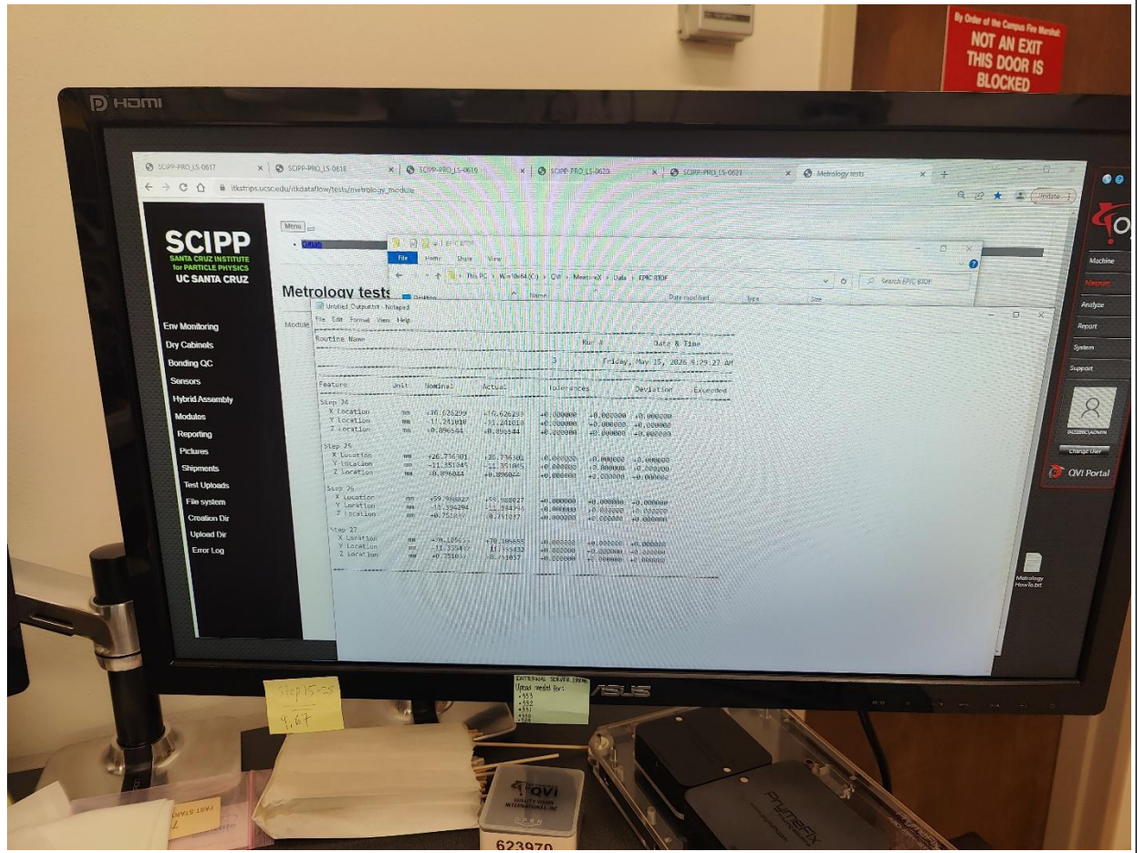
Shim loader and shims
Interposer holder
ASIC and sensor holder
ASIC and sensor loader

Metrology tests

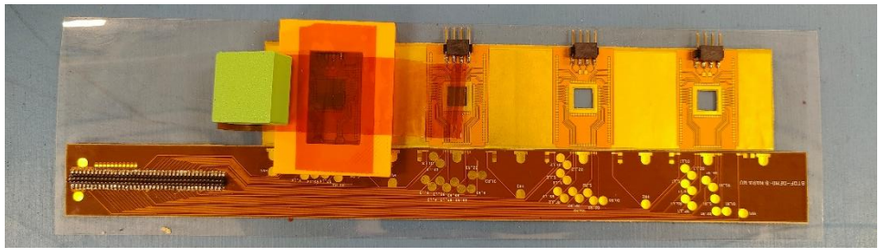
Metrology on ePIC BTOF demonstrator stavelets
Can measure with ~1um precision features on the board
Automatic program can measure all components in 10-20 minutes
Output is a table of position measurements in respect of the reference system

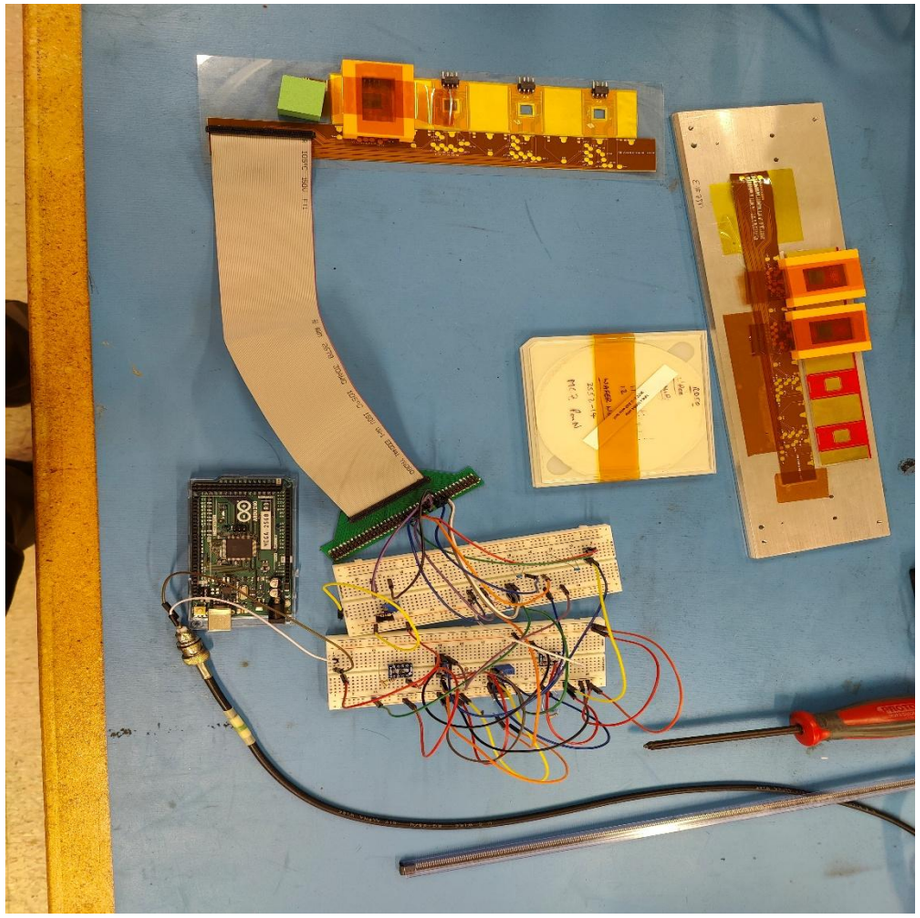


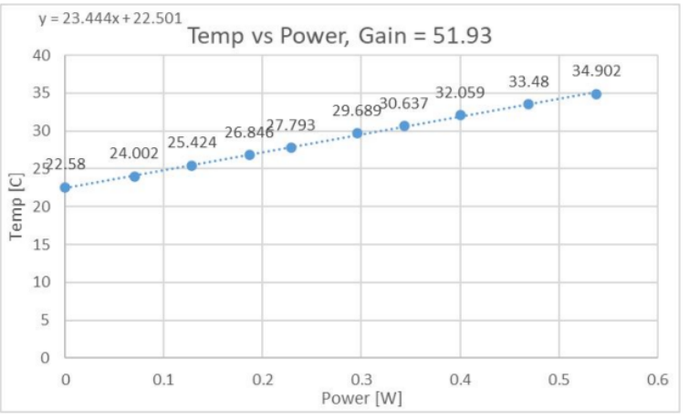


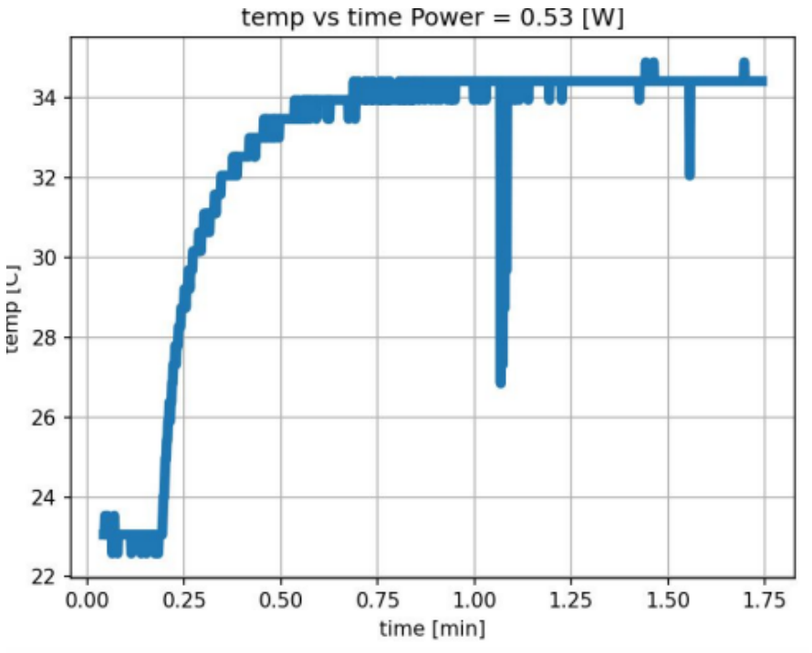


Thermal tests with mock-up ASIC



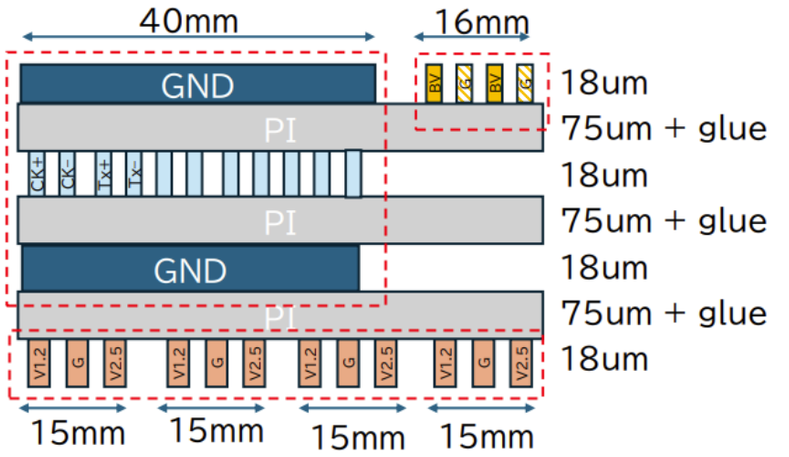


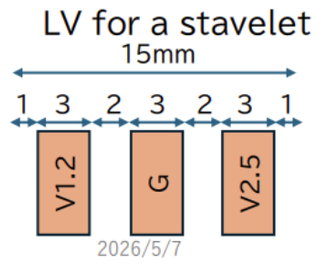


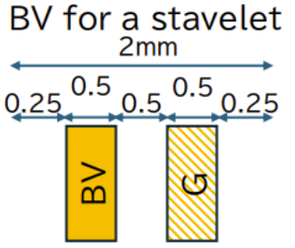


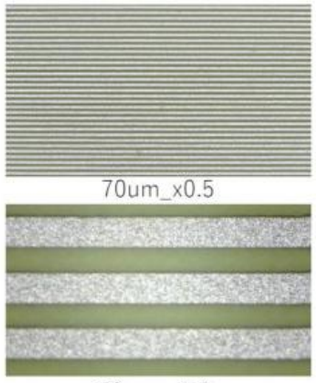
FPC simulations

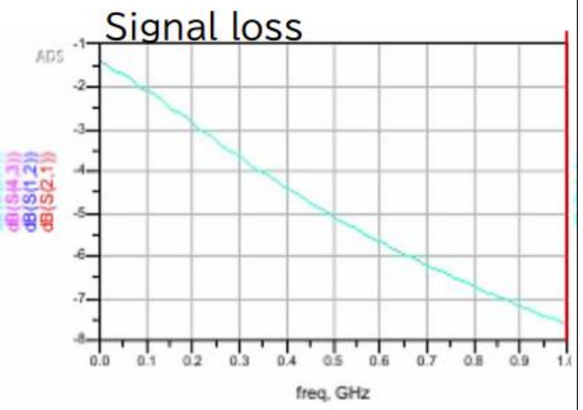
- Mechanical test for Long FPC: 70um line/space is feasible
- LV distribution from edge power board divided in 4 lines with adjusted voltage
  - This keeps LV for FCFD within 5% variation
  - Power consumption 4.8W per line (2 stavelets)
- 8 HV lines (one for each stavelet)
- Simulated on full FPC at 1GHz (clock is 320MHz) signal loss (42%), reflection (4%) and cross talk (6%)







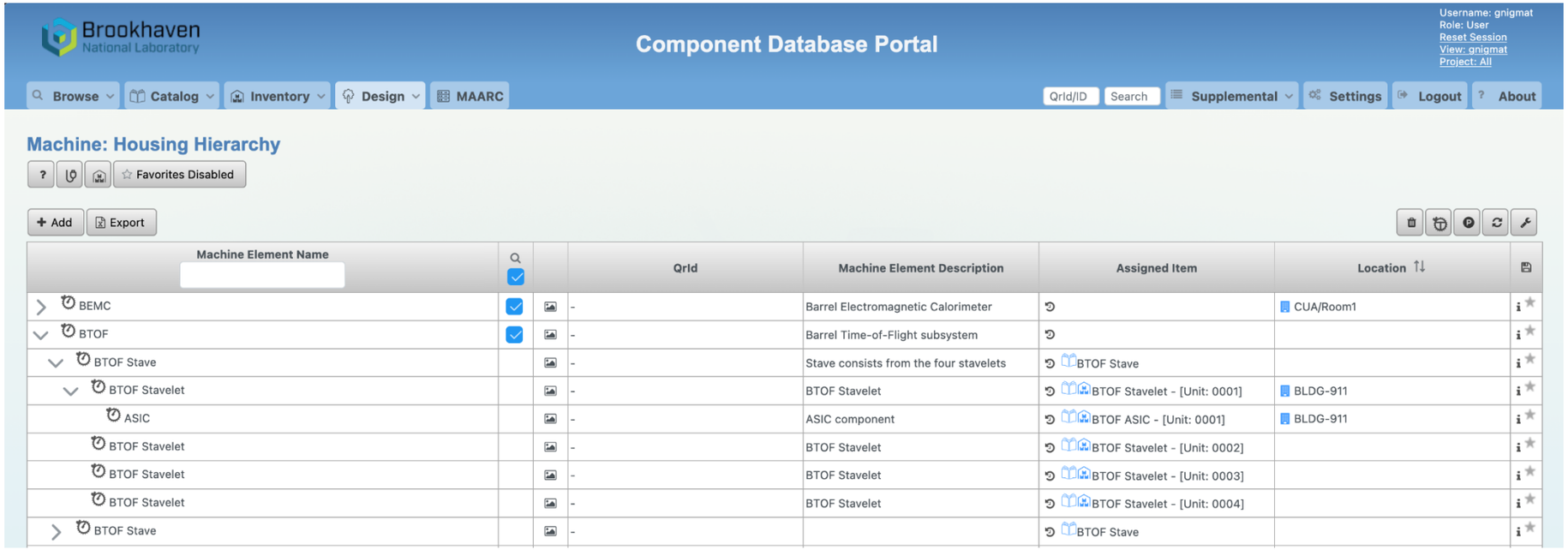




See: https://indico.bnl.gov/event/32810/contributions/124298/attachments/69955/119912/20260506_hachiya_FPCDesignSimulation.pdf

Database and stored information

- Database being configured with central ePIC database, each assembled stavelet will have an entry with:
  - Sensor IV
  - ASIC electrical tests (e.g. power draw)
  - Telemetry results (crucial for final alignment)
  - Pictures of assembly and components
  - Results of QC on assembled stavelet



UCSC ePIC room

Japanese assembly site

- Hiroshima University and RIKEN are building clean rooms for stave assembly
  - ~100 m^2 and ~ 50 m^2 for HU and RIKEN, respectively

- Several equipment have been installed into the institutes
  - Very powerful microscope and large desiccator were installed
  - Manual wire-bonding machines, and high-spec oscilloscope just installed

Subsystem challenges

- Sensors yield low: low risk, several productions with high yield done by HPK. FBK production of ePIC prototypes almost completed to have second vendor.
- Need ASIC by Q1 2028, but ASIC design issues: high risk, but can have 6 months delay in production (enough for another ASIC production)
- Sensor QC done at vendor's level and verified in samples
- ASIC QC can be outsourced to a company

- FPC-stave assembly issues: medium risk, need to test co-curing long FPC soon.
- Assembly yield issues: 10-20% extra production currently planned for.
- Stavelet issues after assembly: medium risk, re-design and production is quick. Can be caught at demonstrator level. Assembly tests ongoing.
- Stave issue after assembly: high risk, longer re-design and production for FPC. Plan to have full stave demonstrator next year.

Charge direct response

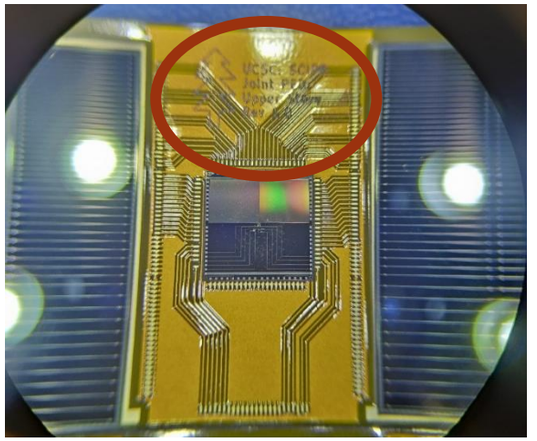
- **Are the technical performance requirements appropriately defined and complete for this stage of the project?**
  - Yes, a lot of the production process is inspired to ATLAS/CMS production and sufficient expertise and equipment exists in institutes
- **Are the plans for the various sub-systems appropriately documented and complete for this stage of the project?**
  - Several discussion and slides are in the indico agenda, still need to work on a centralized share point for results.
- **Are the current plans for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?**
  - Cost increase is low risk, but assembly schedule depends heavily on ATLAS/CMS activities of the involved institutions. Technical problems should be identified at demonstrator level.
- **Are the schedule assumptions for the fabrication of the various sub-systems and assembly plans reasonable and consistent with the overall detector schedule?**
  - Yes if production continues as schedules or with a 6month delay
- **Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?**
  - As indicated by the slides, a QA/QC procedure has been outlined for components and assemblies.

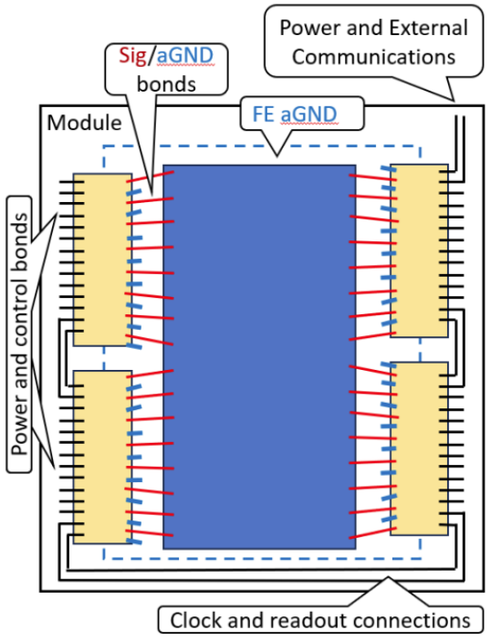
- **Inclusion of additional simulation work on PCB design for transmission lines to define the technical performance and in particular for the resistivity on the BTOF**
  - Full FPC was simulated, the work is ongoing
- **A clearer power budget estimation and cooling design strategy**
  - We now have precise power budget for each LV line from FCFD developers
- **An estimate of the manpower needed and the one available with a trend for the future phases of the project**
  - The stavelet production volume was estimated. It requires 2 Techs (maybe junior and senior) per institute plus several students for loading and QC.

Disclaimer: update on FCFD design

- Issue: current design interposer fan-in lines can be an issue for the chip readout, degrade the signal and introduce extra capacitance
- Solution: use 4 chips per 2 half-sensors, long and narrow with same pitch as sensor
  - Direct wire bond to sensor
- 4 chips will be condensed in only one set of lines, no increase in FPC lines (already at limit)
- Potential idea of 8 chip to 1 to reduce FPC lines
- Finalization of the approval ongoing

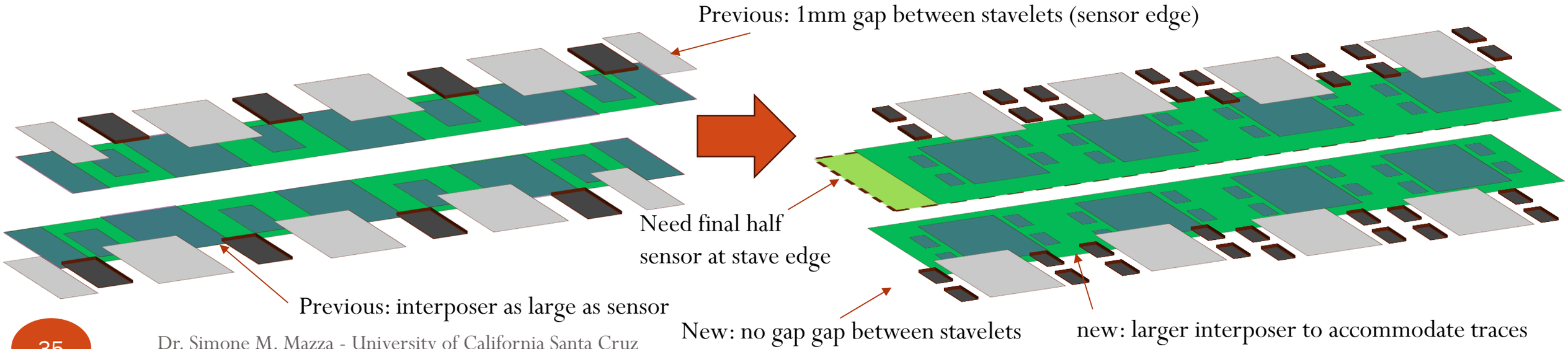
- See: https://indico.bnl.gov/event/32008/



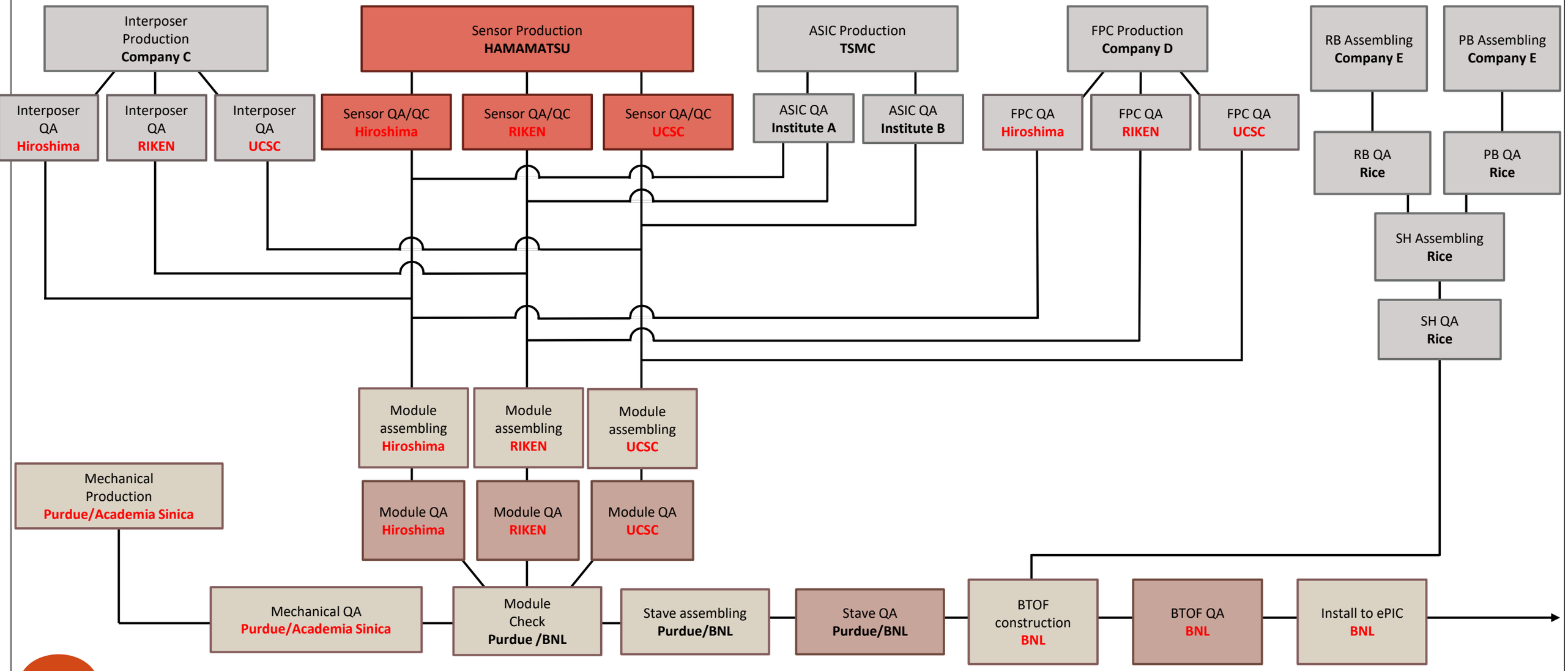


FCFD design change on stavelet since December

- FCFD change will affect the stavelet composition
  - Can split stavelet on the ASIC side, no gap between stavelets
  - Interposer a bit larger to accommodate traces between ASICs
  - No change in assembly precision tolerances
- Still need a Half Sensor at the very edge of the stave to avoid a ~5-10mm gap
  - Edge interposer (1 or 2 per stave) with slightly different design, ending with half (1 column) sensor
- Assembly procedure remains identical, need updated interposer and jigs
  - Next slides: still old design, will be updated once FCFD change is finalized



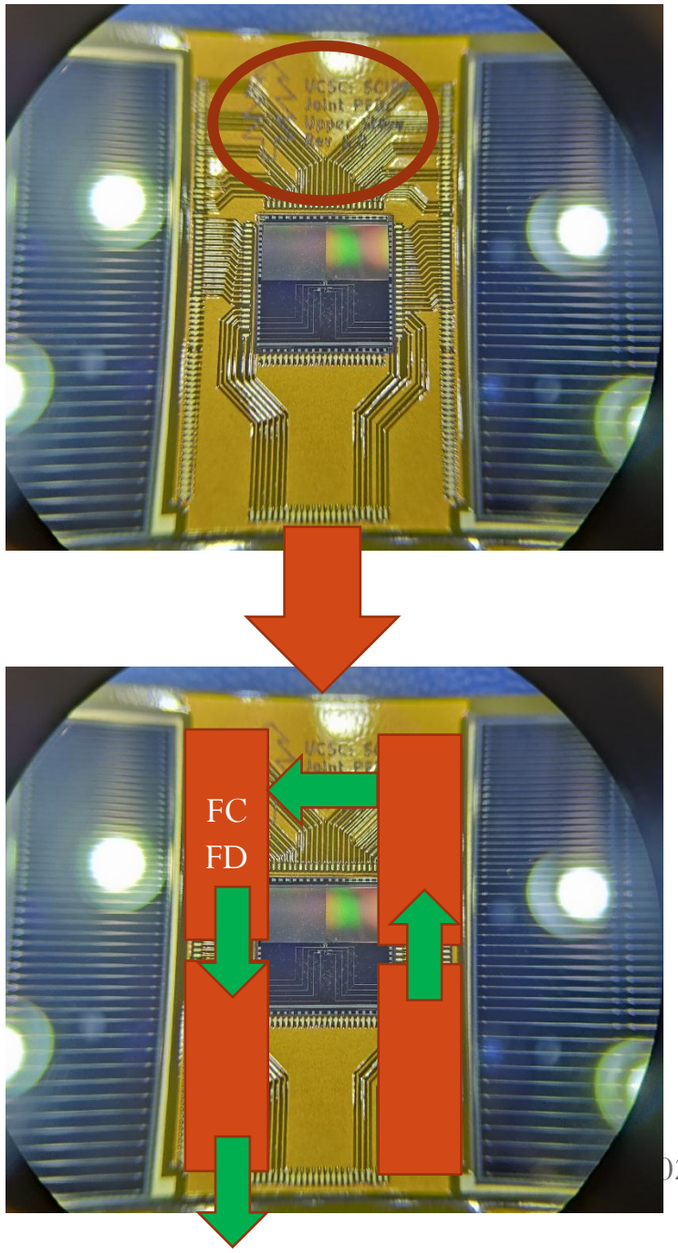
Detector Assembling Workflow



Discussion with FCFD developers

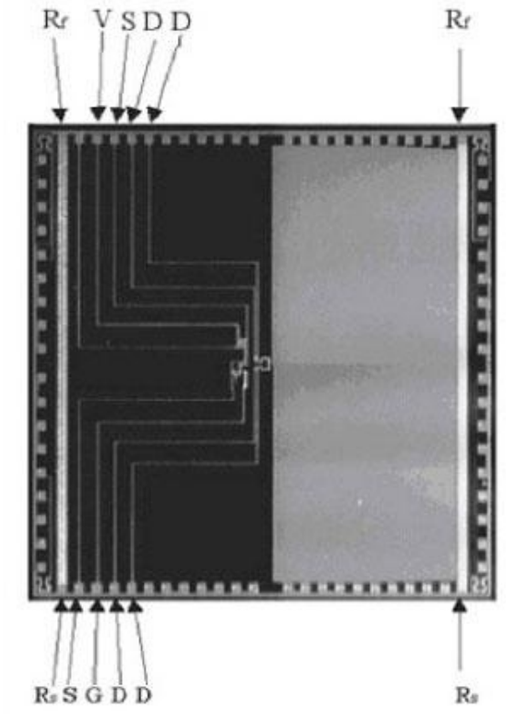
- Fan-in lines can be an issue for the chip readout, degrade the signal and introduce extra capacitance
- Solution: use 4 chips per 2 half-sensors, long and narrow with same pitch as sensor
  - Direct connection to sensor
- 4 chips will be condensed in only one set of lines, no increase in connections

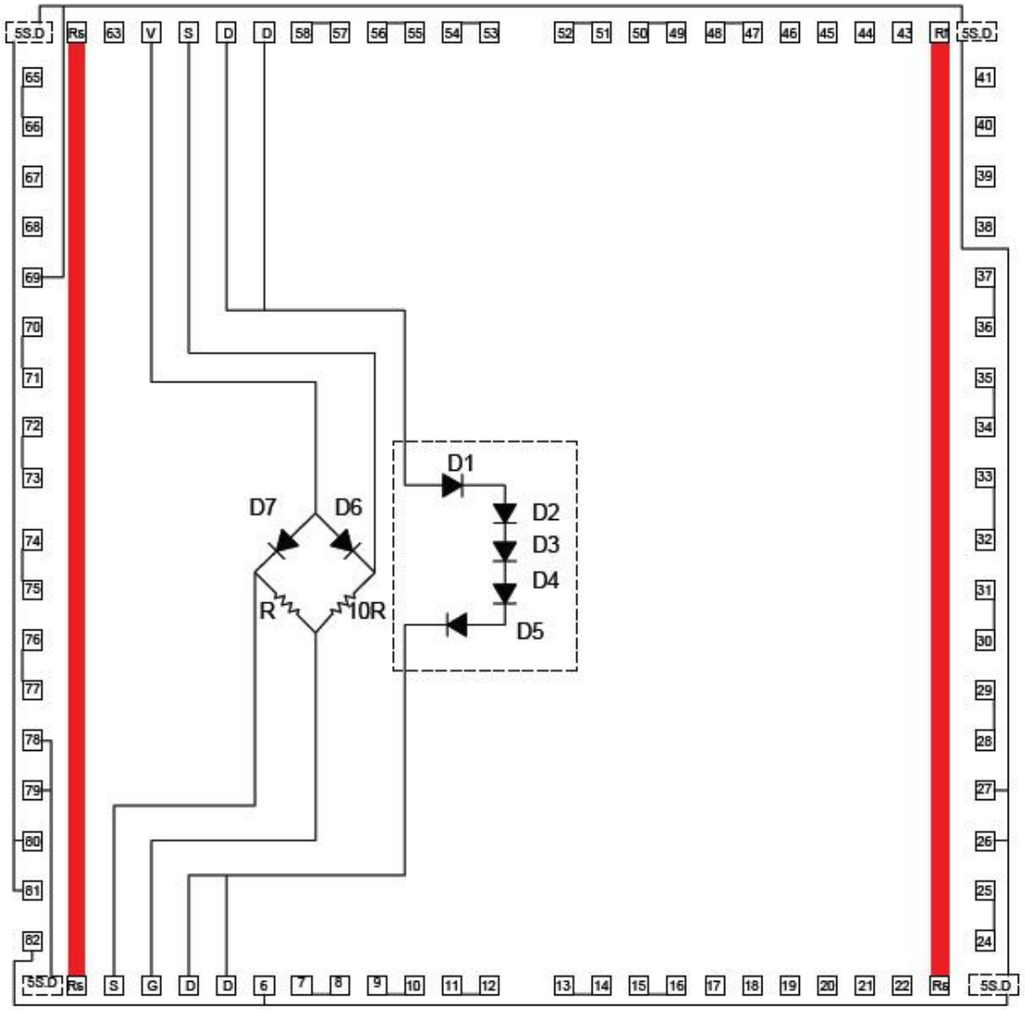
- Stavelet design remains the same, we can't split in the middle the interposer (need lines between chips)



Test Si heater

- 1x1 cm size, 20 in SC right now
- 9 needed for the design
- Each one need 1 line for heaters and 5 (?) for sensors
- Has 2 sensors, one for absolute (less precise) and one for relative (more precise)

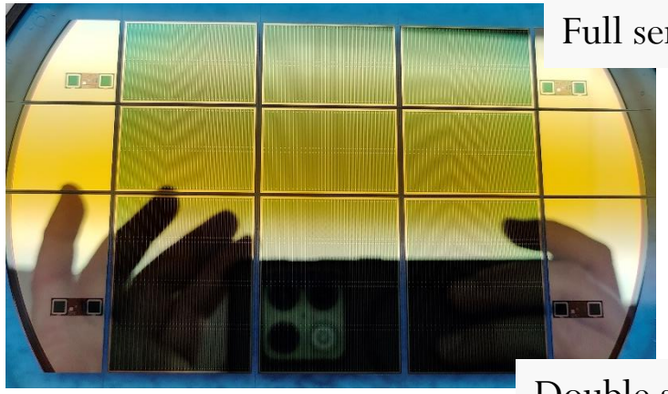




HPK AC-LGAD strip production

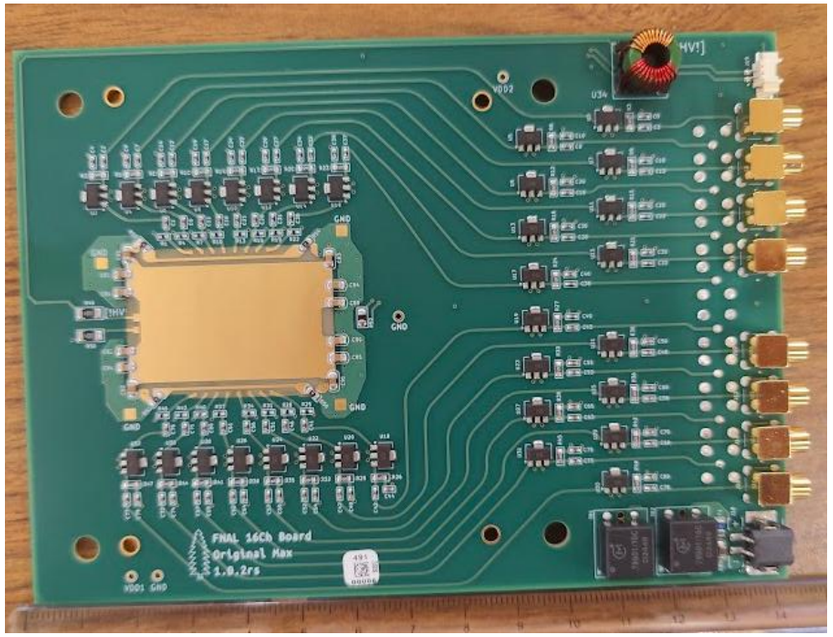
- ePIC full-size production of HPK strip AC-LGADs with devices up to 3.2x4.2 cm
  - Nominal size 3.2x2.2 cm with 1cm strip ‘segments’
  - Strip width: 40-50um, strip pitch 500, 750, 1000 um
- 8 wafers in hand, four 50um thick and four 30um thick

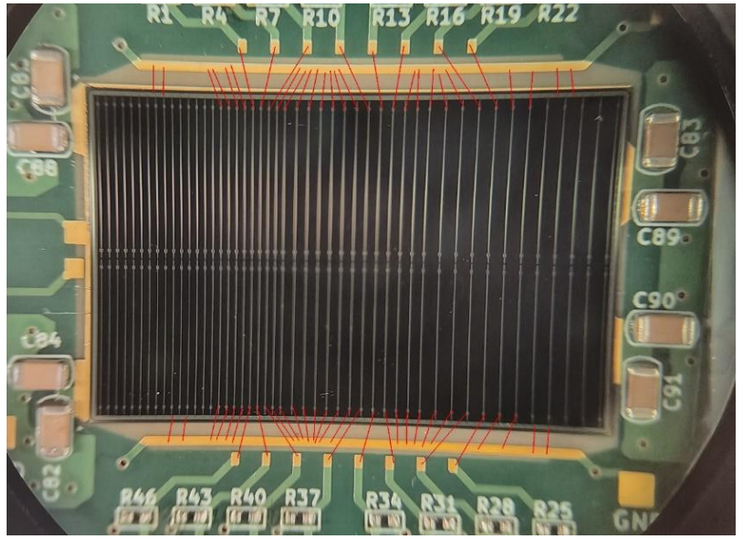
Half sensors

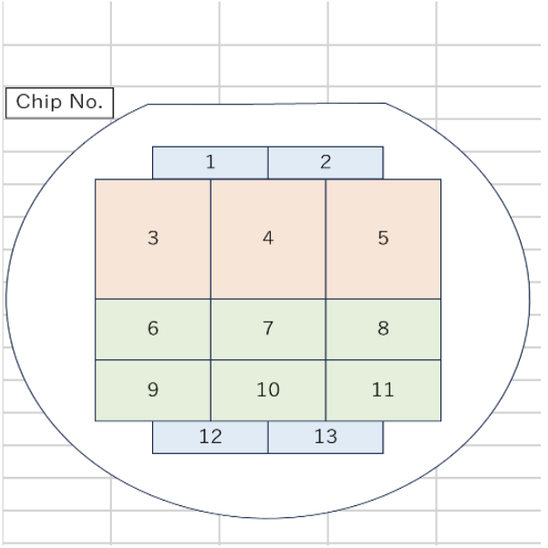


Full sensors

Double sensors

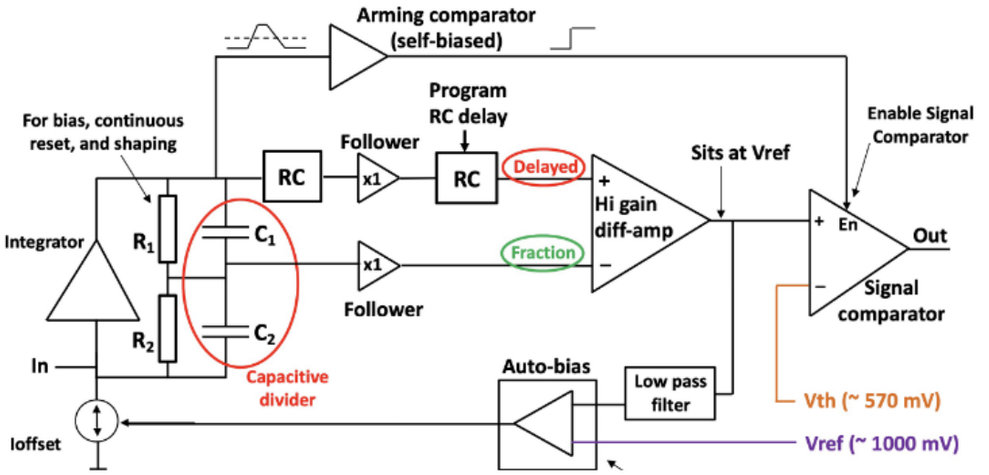


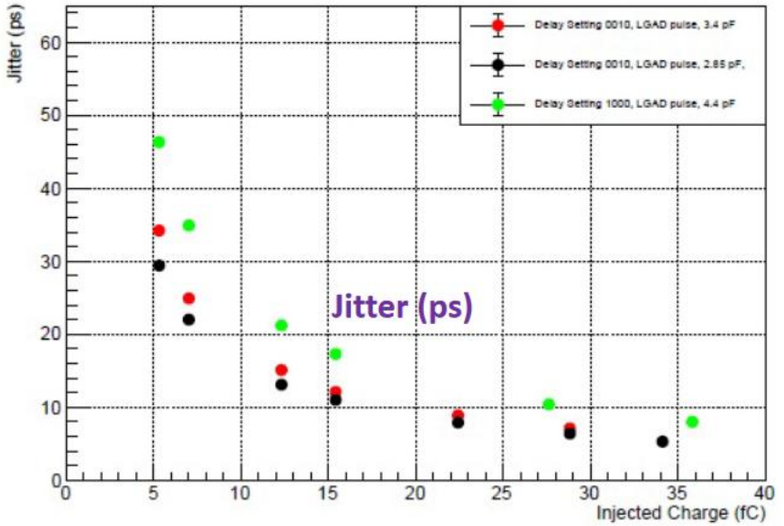




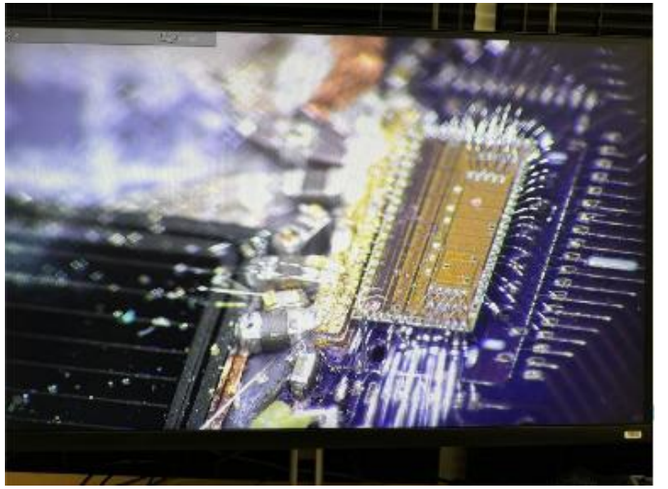
AC-LGAD strip readout – FCFD (FNAL)

- AC-LGAD strip readout developed at Fermilab
  - Can accept high input capacitance o(10pF)
  - Target Jitter <10ps
- FCFDv1 – 6 channel received Jan 2024.
  - Tested at FNAL in May/June 2024, AC & DC-LGAD (1 mm):
- DC-LGAD @ 50 ps; AC-LGAD @ 52 ps
- AC-LGAD should get ~35 ps with improved comparator.
- **FCFDv1.1 –TSMC May 2025; DESY tests in July 2025.**





- 128 ch strip readout
- 65 nm CMOS
- Constant Fraction Discriminator
- Plus TDC, ADC, interfaces
- Cdin: <15 pF
- Dynamic Range: 5-40 fC
- Timing: 10-30 ps
- Links: ~Gbps, multiple
- Radiation tolerant.

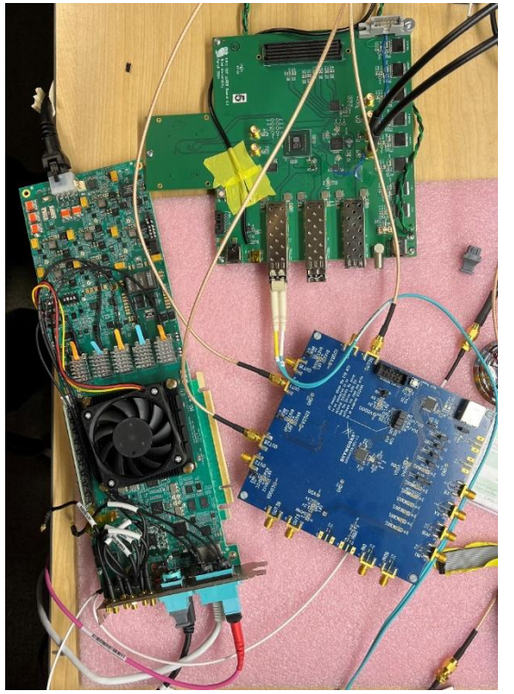


High Precision Clock Distribution

- ppRDO – pre-prototype Readout Board:
  - Generalized to allow readout from various ASICs – FMC connector
  - Xilinx Artix+ FPGA (low cost, CERN TCLink compatible)
  - Clock Jitter cleaner – 5 ps
  - Clock recovery on Rx of SFP or direct clock on dedicated fiber
  - Establish procedures to readout ePIC's ASICs prototype PCBs
  - Develop common streaming readout scheme with DAQ's protocols
  - Platform for radiation tests (SEU measurement and handling)

- Produced and tested 6 PCBs.
  - Jitter measured at 3 ps (Ref clock – FLX182 Tx serializer – ppRDO)

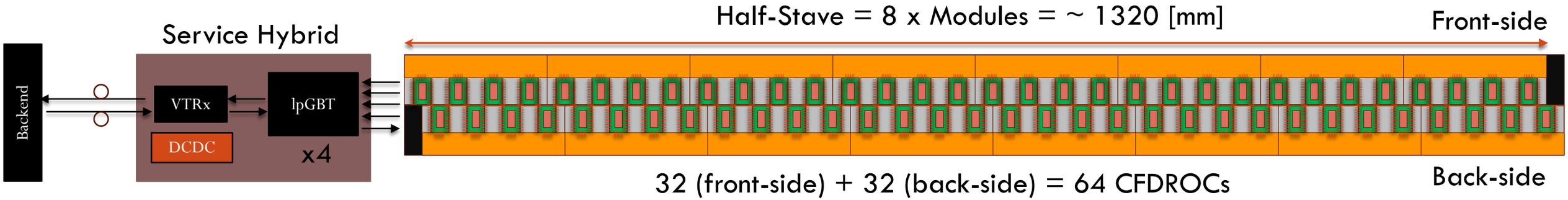
ppRDO
(ADCLK944)

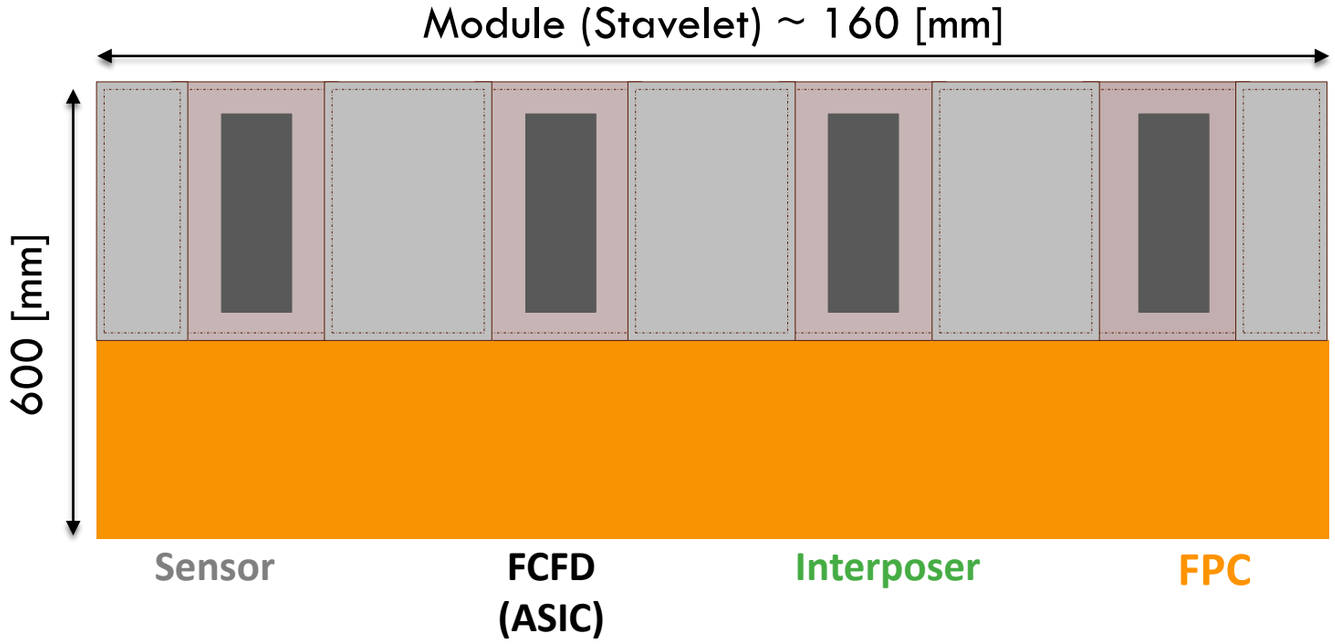


Si5344H
(ref Clock)

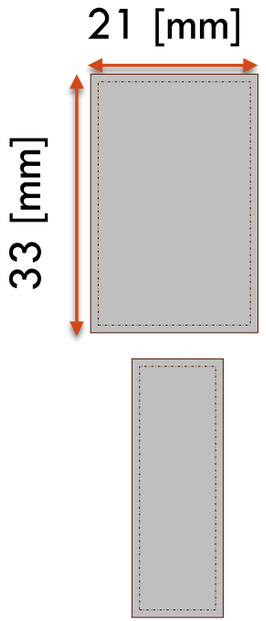
FLX182

Data Transmission





8 x 2 x 288
=4608

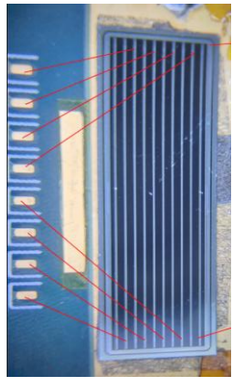


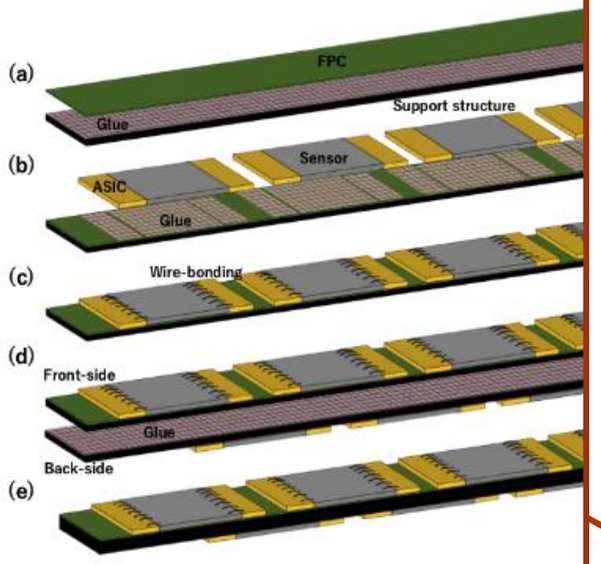
3 x 8 x 2 x 288
=13824

2 x 8 x 2 x 288
=4608

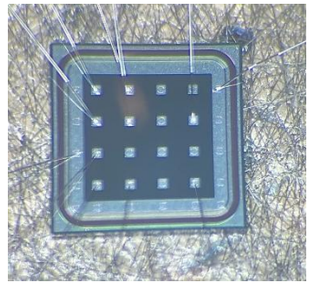
$X/X_0 < 3\%$ (including support structure)

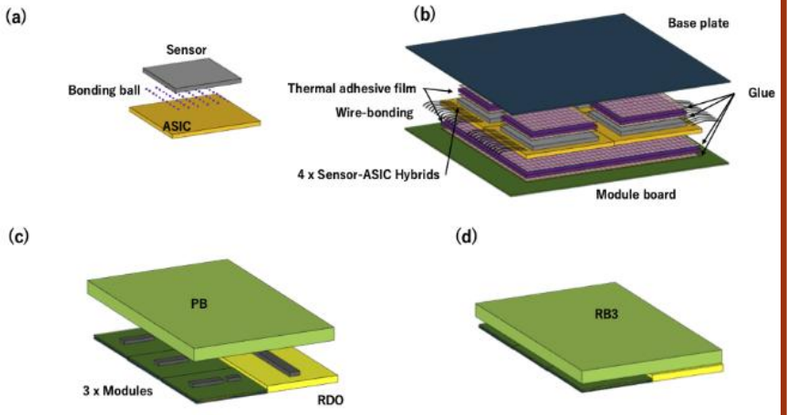
TOF layout in ePIC





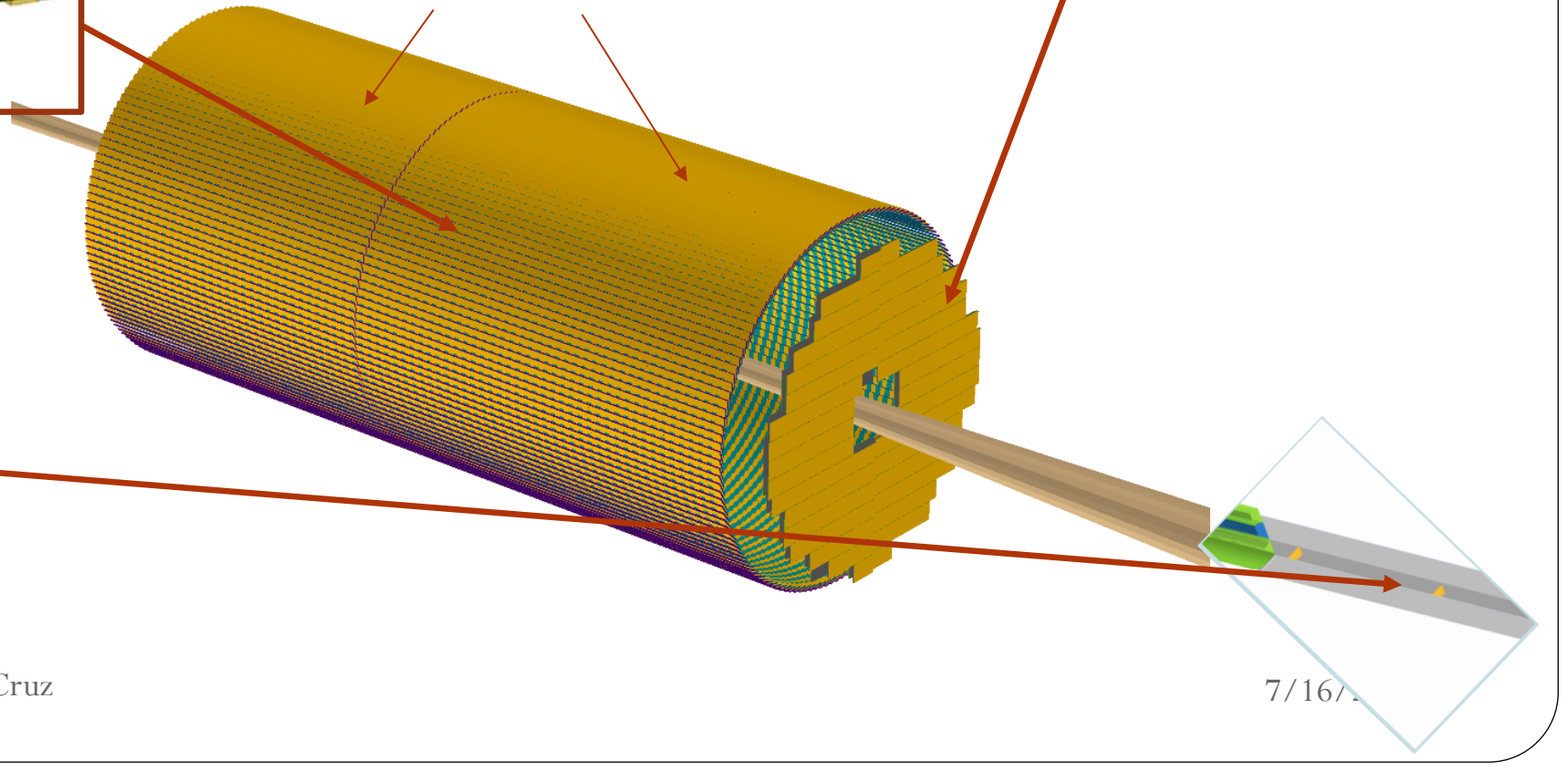
Sensors: strips
Readout: FCFD

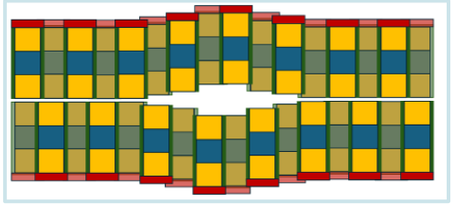




Sensors: pixels
Readout: EICROC

Divided in two halves



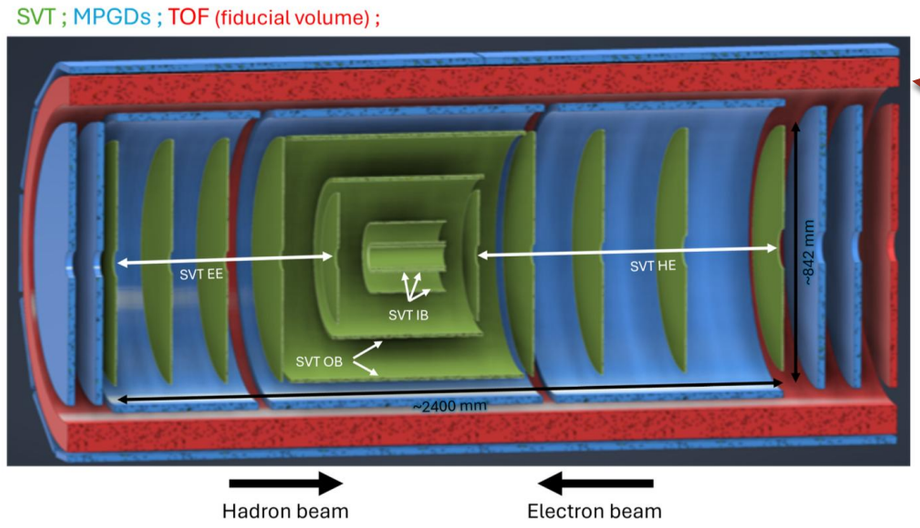


Sensors: pixels
Readout: EICROC

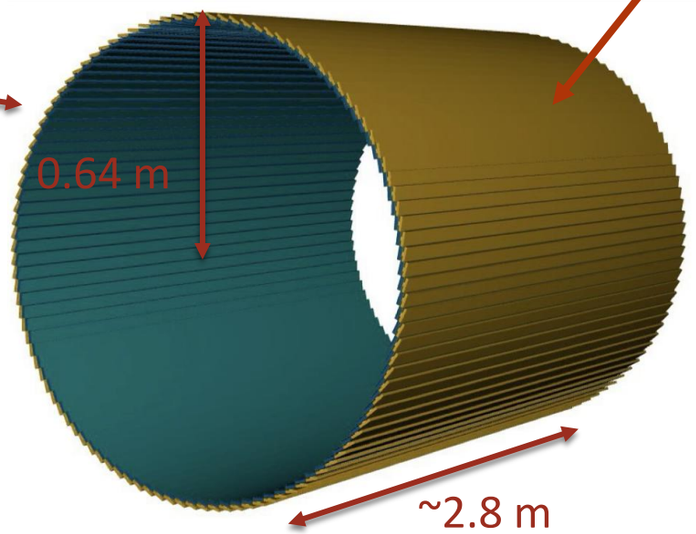
Off-Momentum Detectors (OMD)

Barrel-**TOF**

Staves mounted in 'trays' that can be removed for servicing

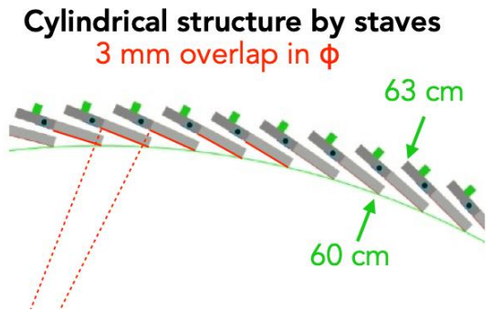


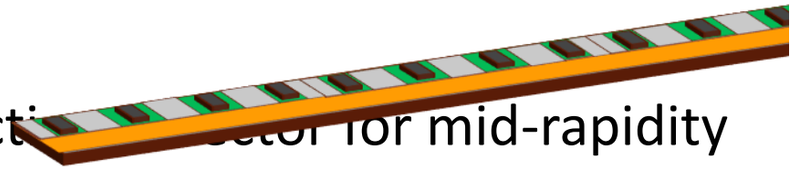
Barrel-TOF (BTOF)



-1.33<η<1.74

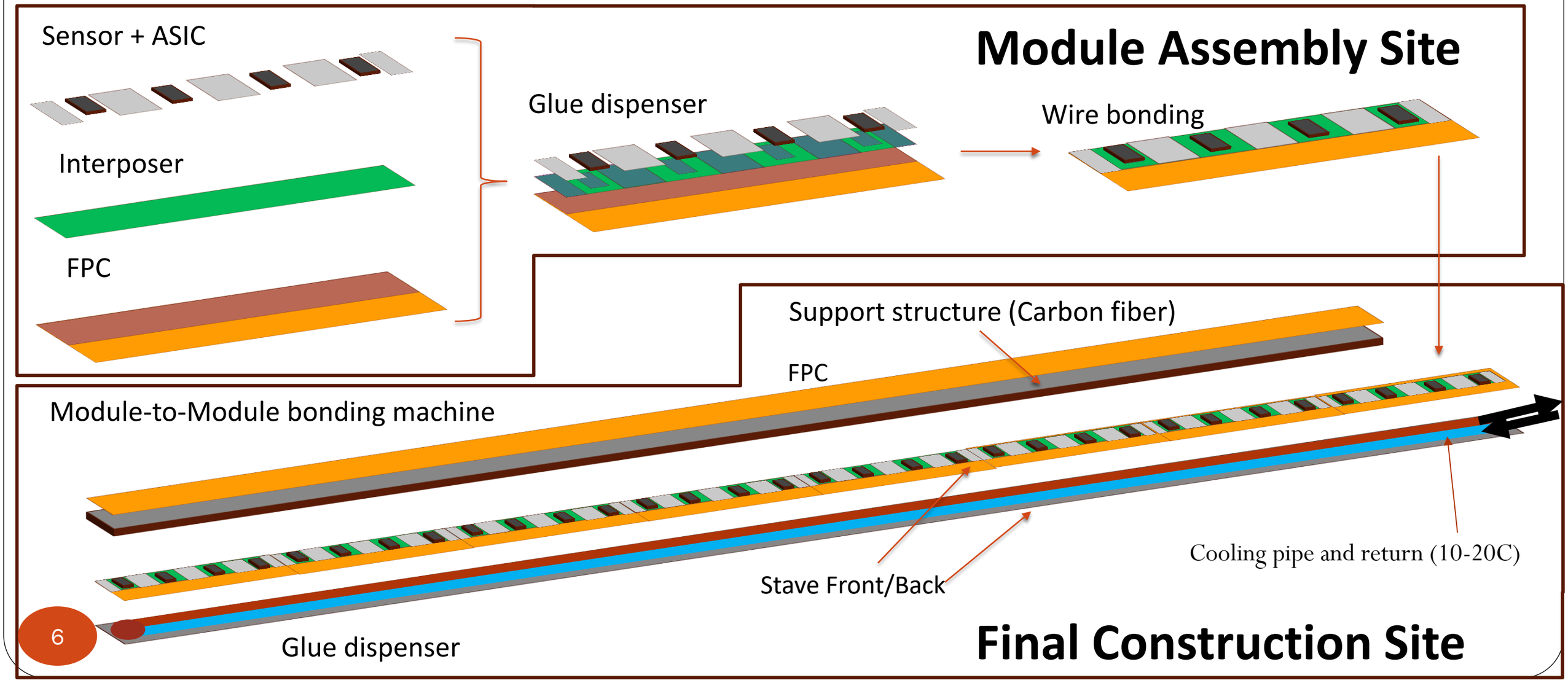
144 x Staves



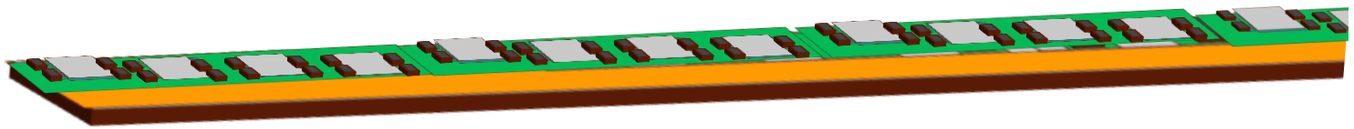


- The ePIC AC-LGAD TOF is PID, tracking and background rejecti… …sector for mid-rapidity (BTOF: -1.33<η<1.74)
- Cylindrical shape is composed of 144 tilted staves (288 half-staves)
- Strip-type AC-LGAD sensor is used to meet the requirement of ~35 ps and ~30 um timing and spatial resolution respectively

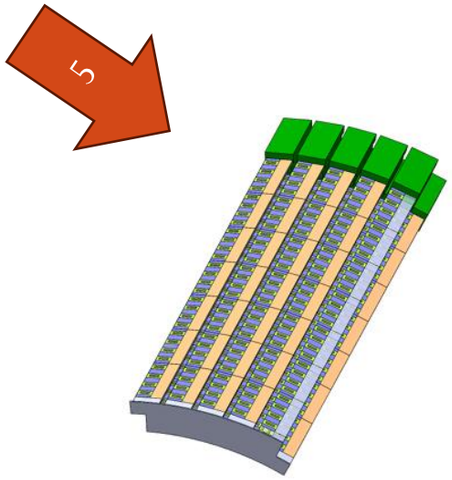
Stave Assembling Steps (Opt1)

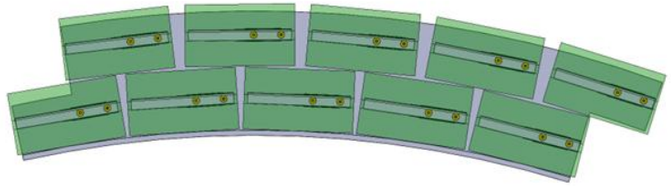


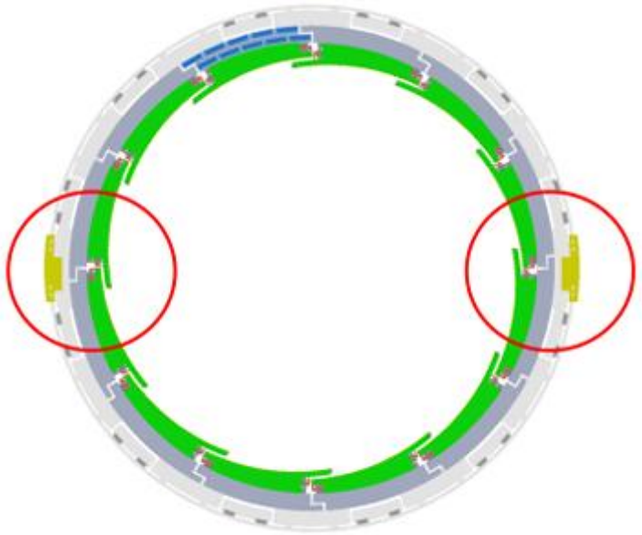
Assembly steps



Step 5: assemble staves in trays
Step 6: assemble BTOF







Crucial activities for the next year or two

- Interposer board finalized design, to do when FCFD is available
- Interposer board simulation in HFSS to understand transient signal effects
- Identification of correct glue (UV or bi-component), viscosity, thermal conductivity
  - It might be necessary to use two different types of glue: thermally conductive glue for ASIC, electrically conductive for sensor
  - If UV glue, design of UV curing box. If bi-component glue, glue robot calibration vs viscosity. If thermal cure, check effects on components
- Identification of glue robot configuration or glue panning with jigs
- Define QC procedure before assembly
- Define QC during assembly (metrology)
- Define QC procedure after assembly (DAQ?) and testing PCB
- Design jigs for stavelet assembly, movement and shipping
- Define wire bond encapsulation needs and procedure
- Define and build database
- To identify the correct components, it might be useful to go to fairs, like Semiconductor West

Plans

Thermo mechanical test – 2025

- Ongoing with PED funds 2025, production of a simple 1 stavelet demonstrator front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers.

Assembly R&D - 2026

- Define glue and first version of Jigs. Define assembly procedure and QC procedure before assembly

Prototype 1 – 2026

- Production of a full stave demonstrator front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers.

Assembly R&D – 2027

- Shipping tests, finalize assembly and identify assembly machines, finalize jigs. QC procedure before-after assembly. Build first QC test station for stavelet

Prototype 2 – 2027

- Production of a full stave rack demonstrator (4 staves) front and back mounted on a carbon fiber support with cooling pipe. ASICs are mimicked with Si heathers. Production of a stavelet with working ASIC and development of PCB for stavelet testing.

Pre-production – 2028

- 10% of production, 500 stavelets

Production – 2028-2030

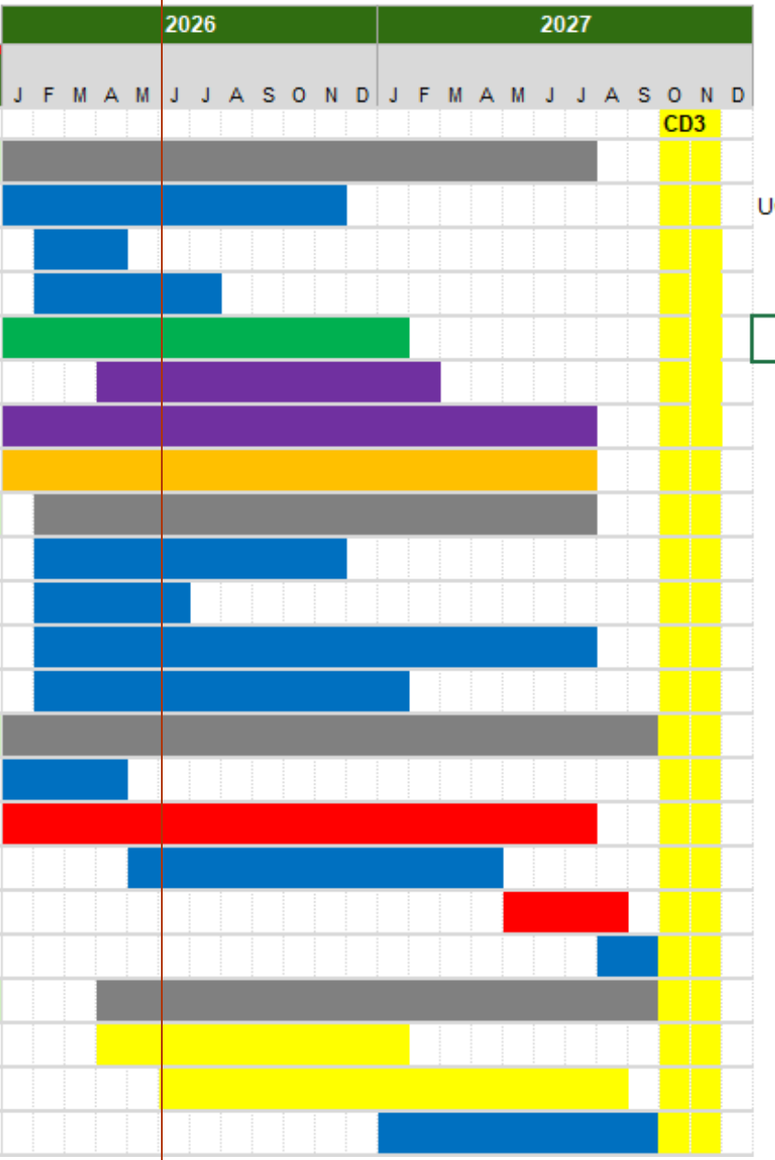
- Remaining 90% of production, 5000 stavelets

Path to CD3

ePIC BTOF fabrication

UCSC, Purdue, UIC, Japan, Rice, FNAL, Not specified

TASK DESCRIPTION	PLAN START	PLAN END	TYPE
DEL1: Components qualification	1/1/2026	7/1/2027	
Qualify final sensor production	1/1/2026	11/1/2026	B
Identify and qualify glue and gluing process	2/1/2026	4/1/2026	B
Finalize interposer design and identity material	2/1/2026	7/1/2026	B
Jigs design and fabrication	1/1/2026	1/1/2027	G
Power board design	4/1/2026	2/1/2027	P
FCFD design and qualification	1/1/2026	7/1/2027	P
FPC design and qualification	1/1/2026	7/1/2027	O
WP2: Assembly sites preparation	2/1/2026	7/1/2027	
Acquiring equipment for the assembly	2/1/2026	11/1/2026	B
Identify the laboratory space for the assembly	2/1/2026	6/1/2026	B
Define QA criteria for components and assembly	2/1/2026	7/1/2027	B
Build stavelet QA station	2/1/2026	1/1/2027	B
WP3: Demonstrator assemblies	1/1/2026	9/1/2027	
Finalize Demonstrator stavelet assembly	1/1/2026	4/1/2026	B
Stave-FPC assembly procedure	1/1/2026	7/1/2027	R
Assembly of 10 stavelets	5/1/2026	4/1/2027	B
Assembly of one mock-up half stave with some instrumented sections	5/1/2027	8/1/2027	R
Demonstrate 90% completion	8/1/2027	9/1/2027	B
WP4: Database set up	4/1/2026	9/1/2027	
Set up online database for QA	4/1/2026	1/1/2027	Y
Set up multi-institution communication protocol	6/1/2026	8/1/2027	Y
Identify QA criteria and information to put in database	1/1/2027	9/1/2027	B



UCSC, Japan

Institutes involved and roles – pre-assembly

- Hiroshima – define FPC QC/QA, define interposer QC/QA. Wirebond and assembly tests
- Riken – design FPC, define FPC QC/QA. Wirebond and assembly tests
- UCSC – Identify glue, define needed machines (glue robot, storage), design interposer. Wirebond and assembly tests, stavelet QA development
- UIC – holding jigs, shipping jigs, gluing jigs, database set up
- FNAL – design FCFD, test FCFD
- Rice - SH
- Purdue – Test stave production, test assembly, mechanical integration