# Toward Long FPC

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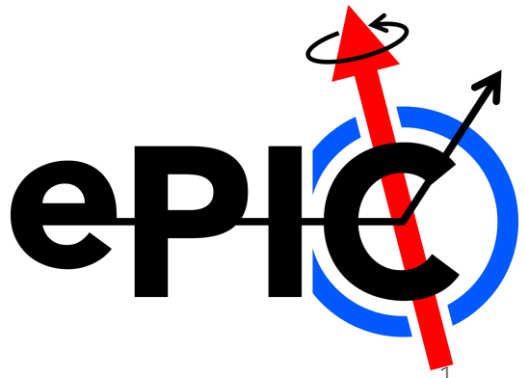


# Current Status and Remaining Challenges

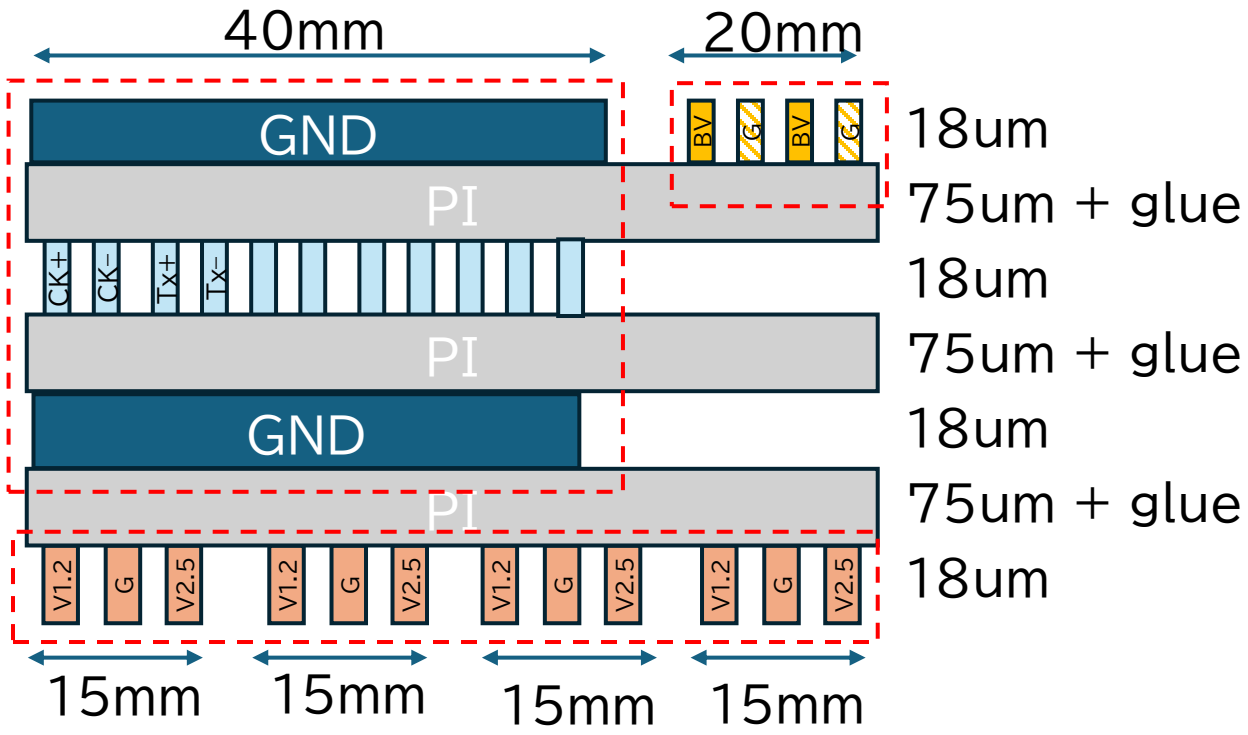
- Goal: Develop a 130cm long FPC for the ePIC BTOF detector.

- **Current Status**
  - FPC design is under development.
  - Layer structure and signal routing are being optimized.
  - Power distribution scheme under consideration.
  - Interfaces to the Service Hybrid and stavelets need to be designed.
- **Remaining Technical Challenges**
  - Routing ~200 signal lines over 130 cm with uniform line width / space
  - Maintaining clock quality
    - 320 MHz
    - <10 ps jitter
  - Archiving reliable 320 Mbps data transmission.
  - Minimizing voltage drop.

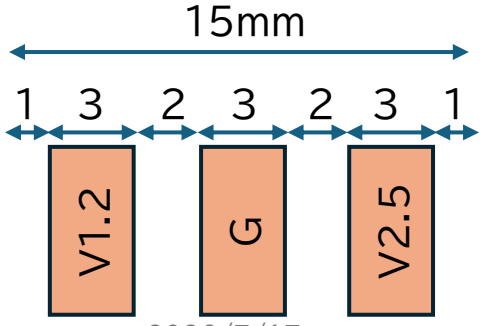
- **Newly Identified Challenge**
  - Thermal management of the high-power FCFD.

- These requirements are compiled in the DOC below:
  - https://docs.google.com/document/d/1gJO5AsvFQypVvU2cHV11WHy5QTBQ1Opm3aAoIuFGR0E/edit?usp=sharing

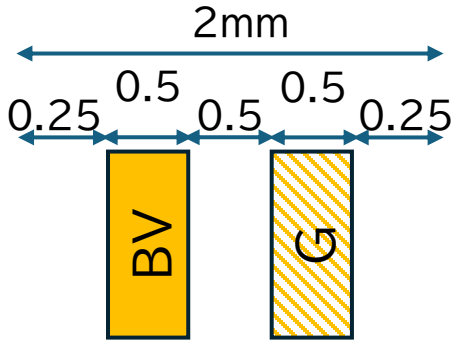
# Layer Structure



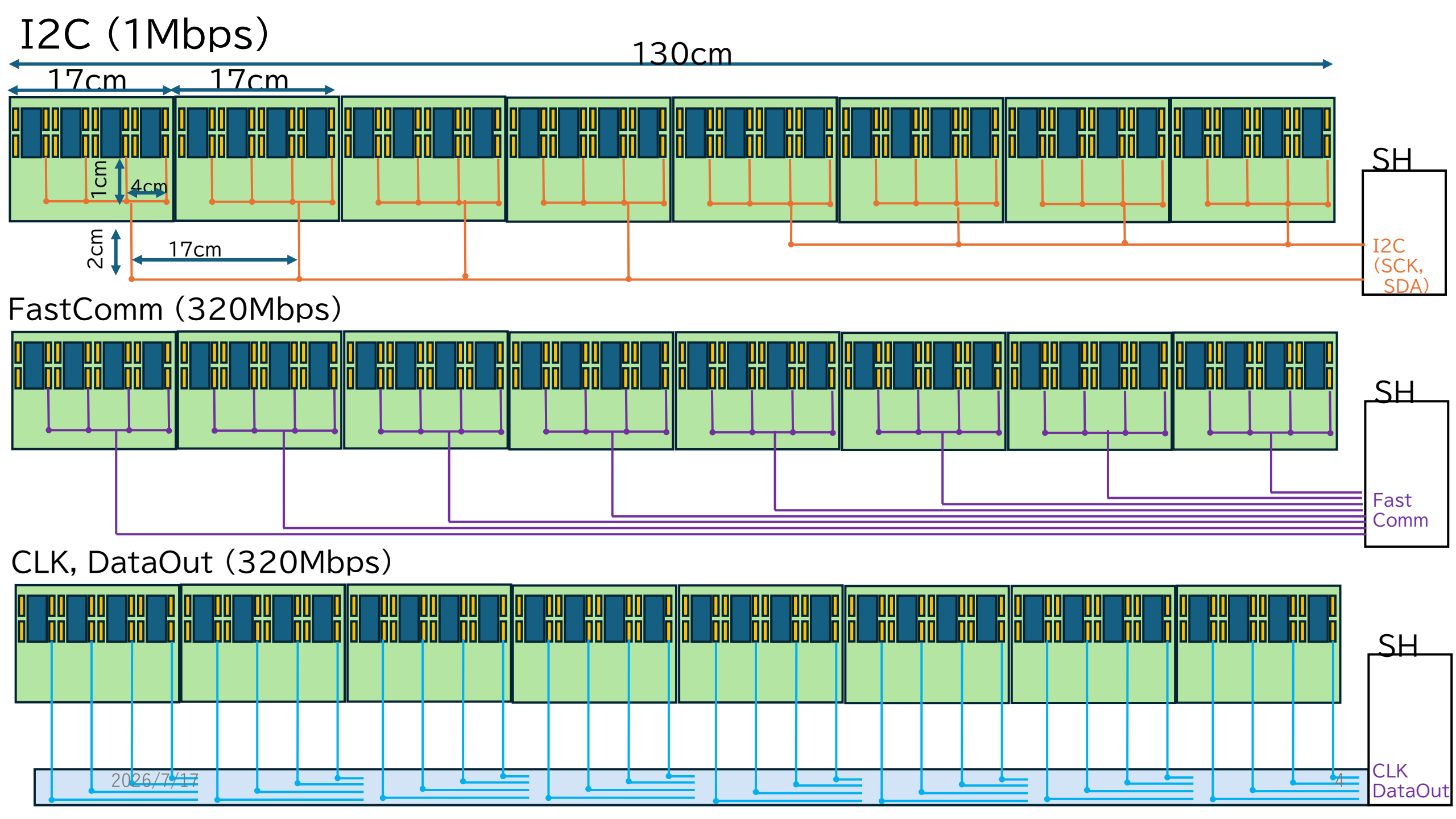

LV for a stavelet




BV for a stavelet




- **Design Concept**
  - Four-layer FPC structure optimized for signal integrity and power delivery.
  - Stripline configuration adopted to achieve controlled impedance and low crosstalk.
- Four-layer FPC
  - Layer 1 : GND + HV(+GND)
  - layer 2 : Signal,
  - layer 3 : Signal GND
  - layer 4 : LV Power (1.2V and 2.5V)
- Design parameters:
  - Signal Cu thickness :18um
  - Power Cu thickness :18um (default), 30um (consideration) to reduce voltage drop
  - Single Line & Space : 70&70 um
  - HV trace width: 0.5 mm
  - LV power width: 3 mm


I2C (1Mbps)
130cm
17cm
17cm
1cm
4cm
2cm
17cm
SH
I2C
(SCK,
SDA)
FastComm (320Mbps)
SH
Fast
Comm
CLK, DataOut (320Mbps)
SH
CLK
DataOut

# Simulation and Prototype Development

Simulation and prototype development are carried out in parallel to reduce technical risks.

- **FPC Simulation**
- **Step 1: Completed**
  - Simple Circuit simulation
    - Goal : Impedance
- **Step 2: Completed**
  - Simple but EM-field simulation
  - Goad: expected electronical performance
    - Clock Jitter / signal integrity
- Step 3: In progress
  - EM-field simulation w/ realistic line routing
  - Goad: expected electronical performance
    - Clock Jitter / signal integrity

- **FPC Prototype fabrication**
- **Step 1 : Completed**
  - Prototype signal layer using the INTT design
  - Objective
    - Verify fabrication of 70 $\mu$m line/space over a 130 cm FPC.
    - Compare with the INTT design (130-$\mu$m line width).
  - Material : Cu: 12 $\mu$m, PI: 20 $\mu$m
- **Step 2 : Completed**
  - Prototype using the baseline materials
  - Objective
    - Verify manufacturability using the target materials.
  - Material : Cu: 18 $\mu$m , PI: 75 $\mu$m
- **Step 3 : In Progress**
  - 130 cm prototype with the INTT routing
  - Goals : electronical performance
    - Clock jitter / Signal integrity
    - Characteristic impedance (50 Ω)

+

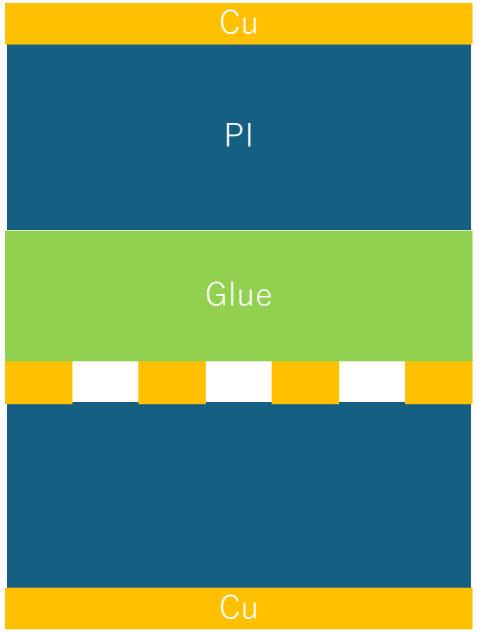
Other performance
- Thermal
- Peel strength
- Aging

- Step 4 Next
  - 130 cm prototype with the BTOF routing
  - Goals
    - Validate the final routing, Verify clock and data transmission performance.

# Signal Integrity Simulation for the Long FPC

- Signal integrity is critical for achieving the required BTOF timing performance.
- **Objective**
  - Verify that the long FPC satisfies the BTOF requirements of Clock jitter and signal transmission.
  - Evaluate signal integrity before prototype fabrication.
- **Simulation Items**
  - Characteristic impedance
    - 70-$\mu$m line width / 70-$\mu$m spacing
    - Target: **50 Ω (single-ended), 100 Ω (differential)**
  - Eye diagram
  - Clock jitter
  - S-parameters
    - Insertion loss
    - Reflection
    - Crosstalk
- **Expected Output**
  - The simulation predicts the electrical performance of the baseline design and identifies potential issues before fabrication.

Strip line structure
(Covered by top and bottom




R-F755： PI:75um， Cu: 18um
PI er = 3.2

Glue sheet：YBL-000-OL、50um
er=2.5

R-F755： PI:75um， Cu: 18um

Line width：70um, space btw lines：70um

# Signal Integrity Simulation Results

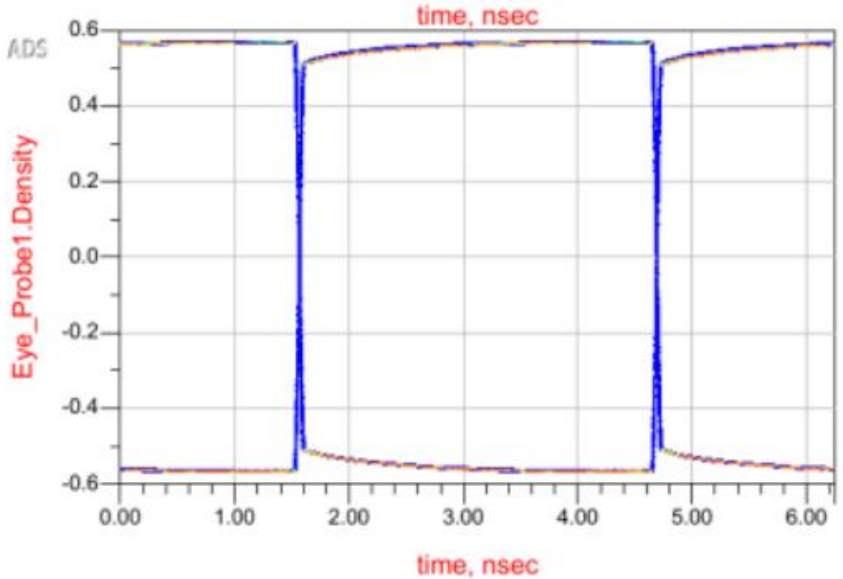
- **Simulation Conditions**
  - Full-wave 3D electromagnetic simulation
  - Input signal:
    - 320 Mbps data stream
    - 20 ps rise time
  - Clock pattern and random data pattern evaluated separately

## Results

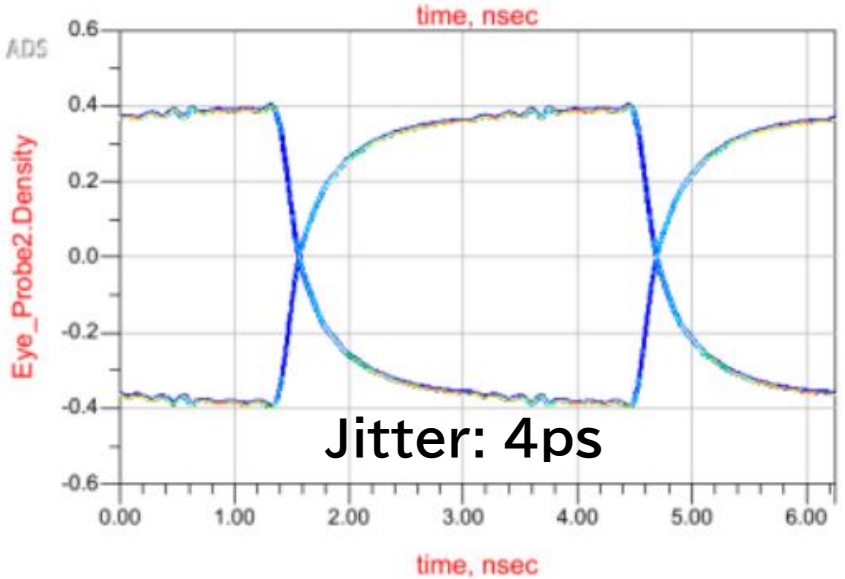
| | |
|---|---|
| Clock jitter | **4 ps** |
| Data jitter | **40 ps** |
| Eye diagram | **Widely open** |

- The baseline long-FPC design satisfies the signal integrity requirements for the BTOF detector.

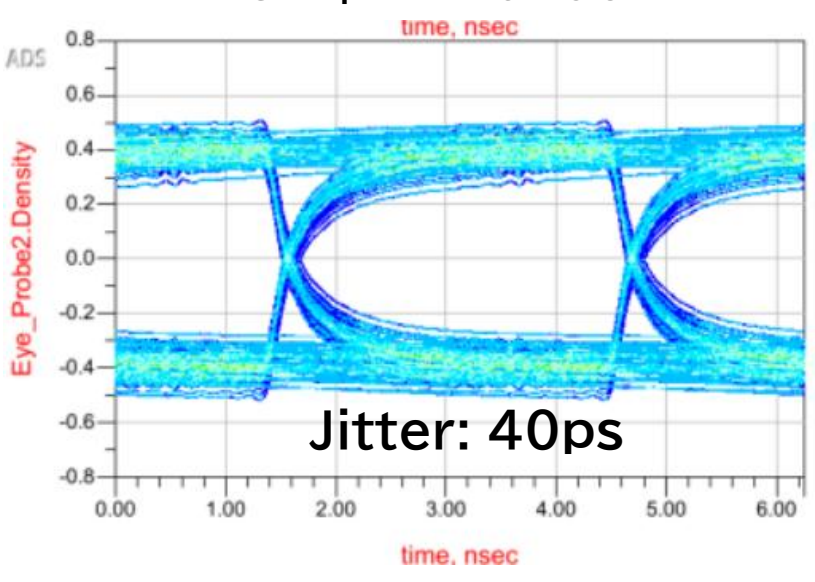
Input




Output: Clock

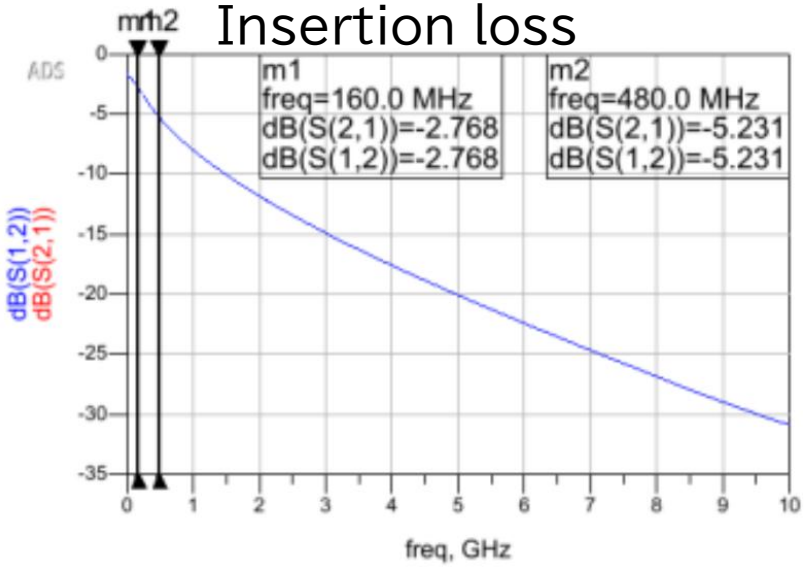



Output: Random

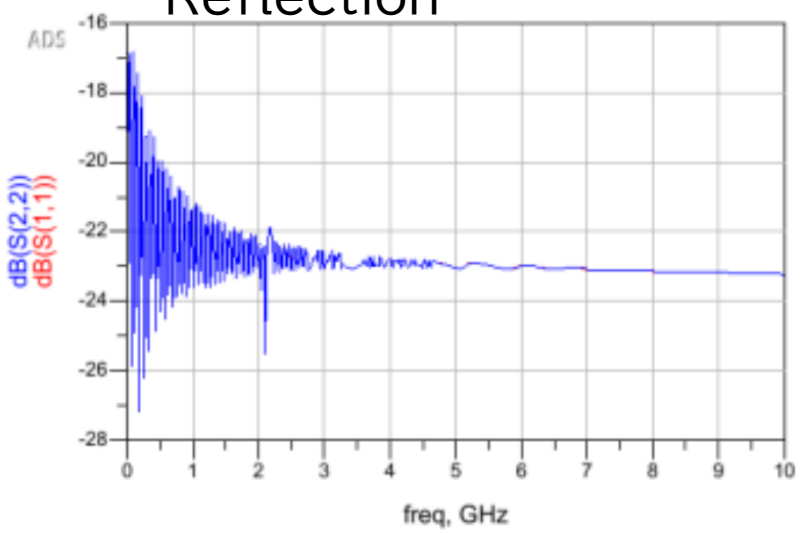


# Signal Transmission Performance

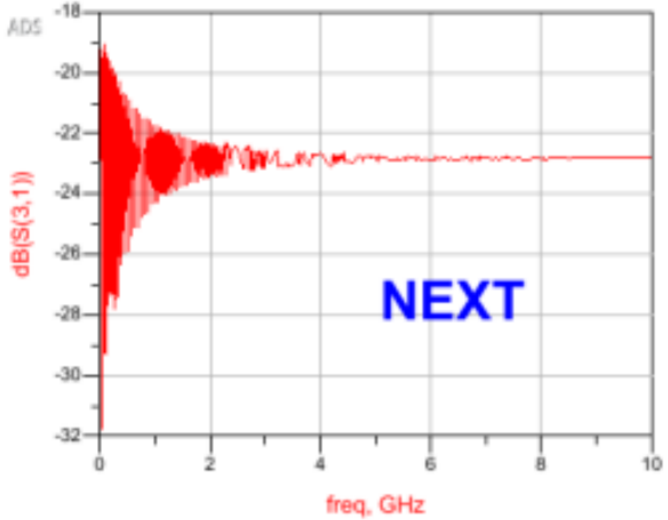
Insertion loss




Reflection




Cross Talk




- Evaluate the distortion at 0.8~1GHz (2.5 x reference freq. (320MHz))
  - Insertion loss : -7.5 dB = 42%
  - Reflection : -23 dB = 7%
  - Crosstalk : -23 dB = 7%

Comparable to the sPHENIX INTT FPC, which has been successfully operated.

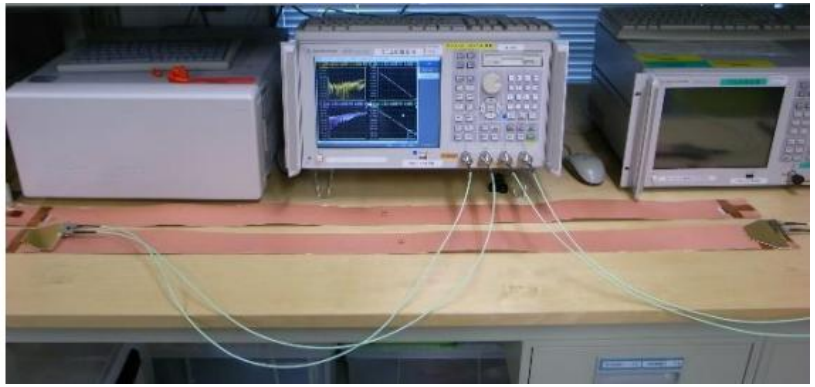
- These results satisfy the current BTOF requirements.
  - This simulation assumes an ideal straight routing. A realistic routing model is under development.
  - The simulation currently assumes the lpGBT driver. The model will be updated once the FCFD output characteristics become available.

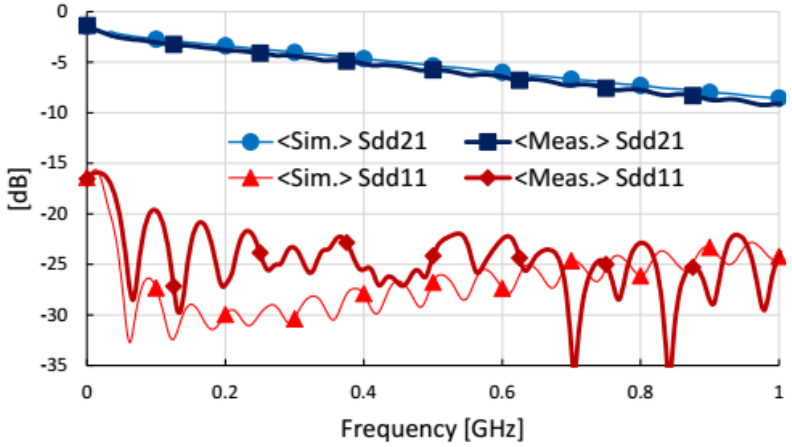
# Preparation for Signal Transmission Measurements

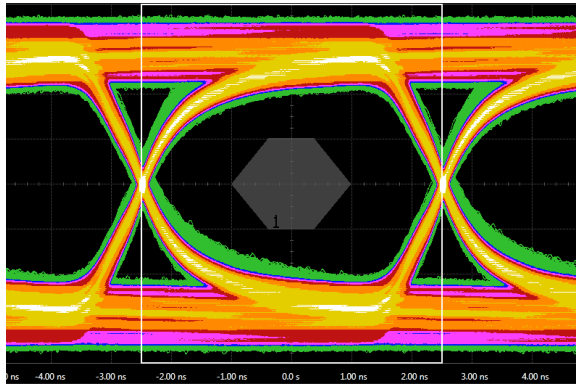
- **Current Status**
  - VNA has been purchased:
  - The measurement environment is being prepared.
  - The measurements will be performed w/ the engineer.
- **Measurement Plan**
  - Evaluate signal transmission characteristics of the prototype FPC.
  - Compare the measurement results with the simulation.

Keysight VNA : 4ch, 20GHz


- Previous measurement for sPHENIX-INTT

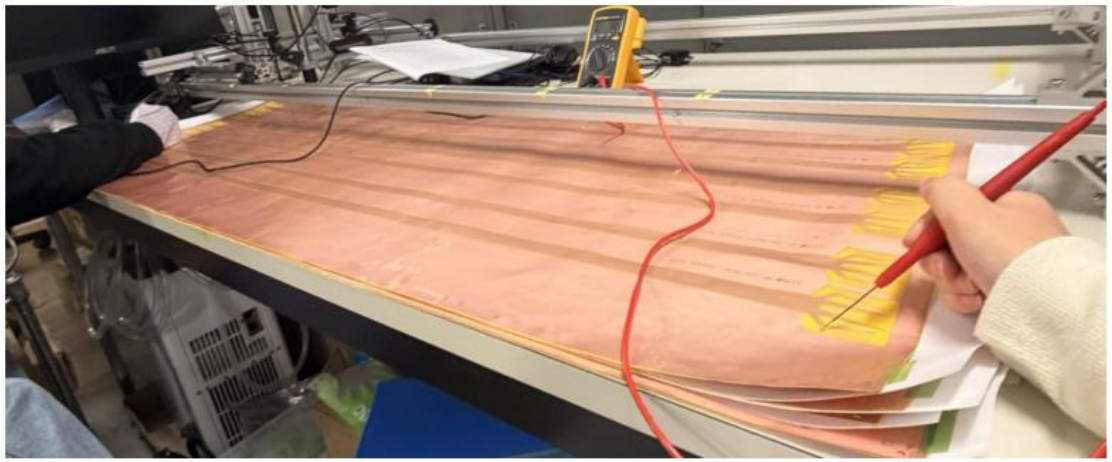




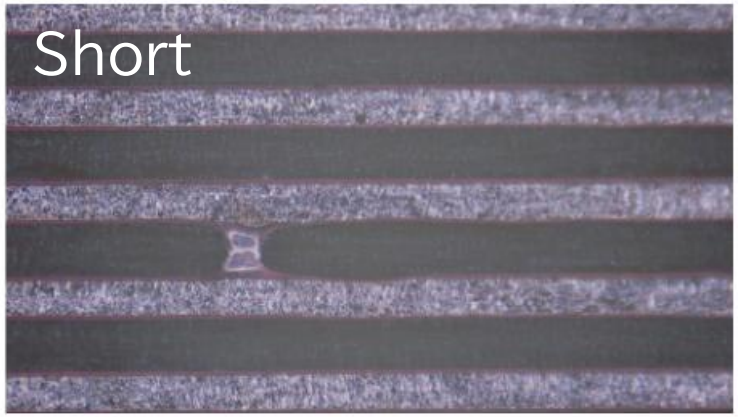



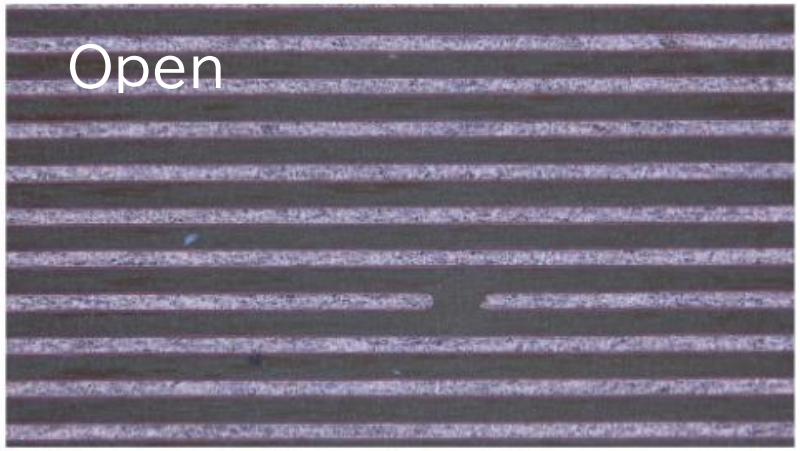
# Prototype Fabrication Results

- Electrical Continuity Test
- **Two prototypes** fabricated.
  - Cu thickness: **12 $\mu$m** + 20um PI (Step1)
  - Cu thickness: **18 $\mu$m** + 75um PI (Step2)
- **Electrical Inspection**
  - Open/short test by resistance measurement
  - Most signal lines were fabricated successfully.
  - 98.6% of the signal lines passed the continuity test (710/720).
- **Results**
  - **The first prototype demonstrated good manufacturability.**
  - The identified defects will be addressed in the next fabrication

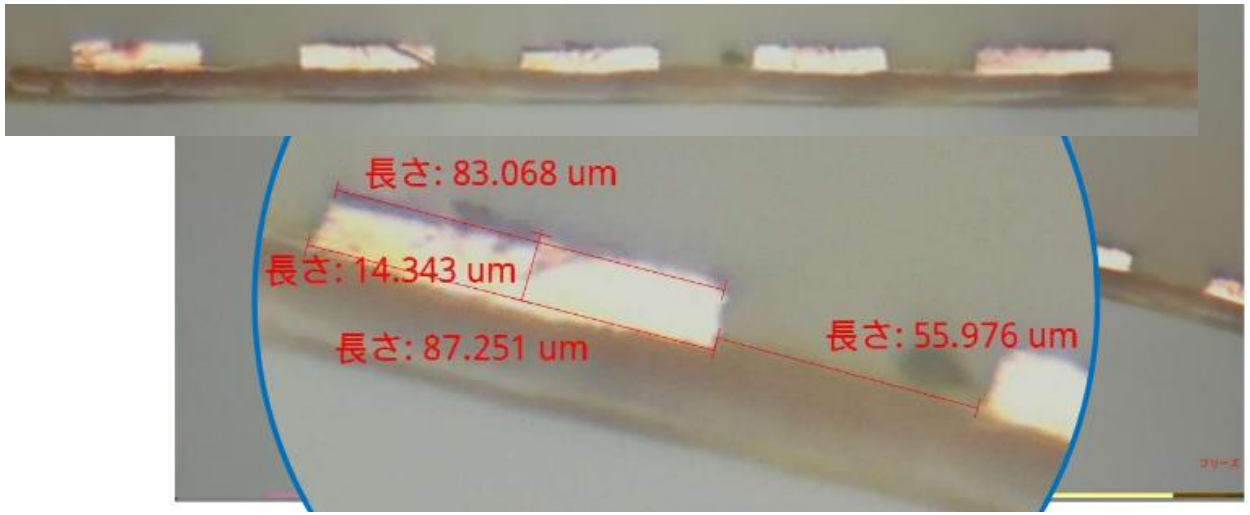


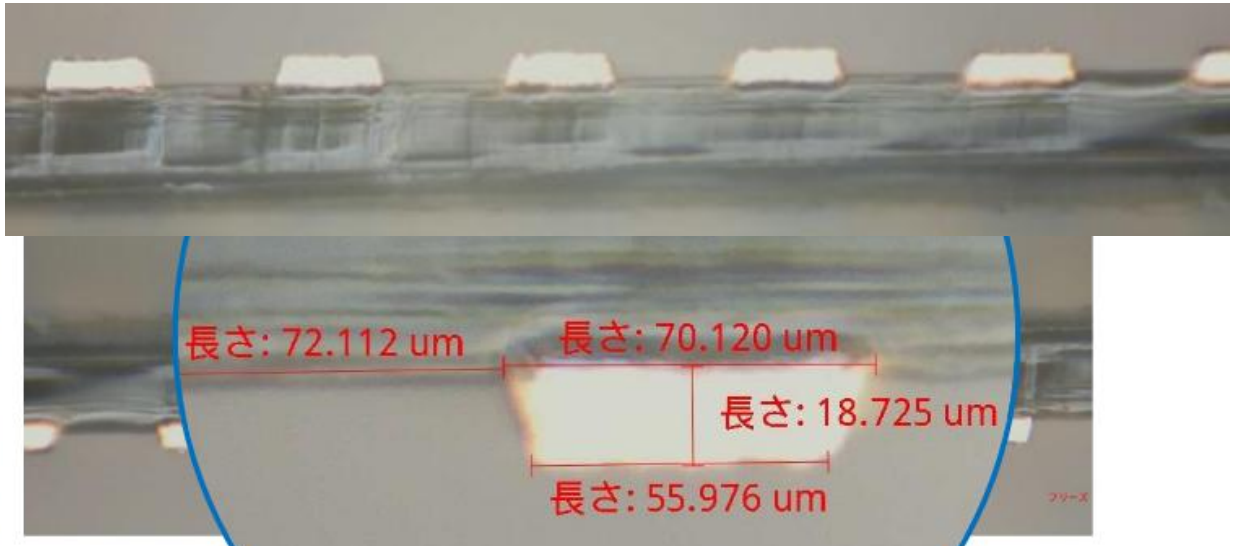
| | 18um_1 | 18um_2 | 18um_3 | 18um_4 | 18um_5 | 18um_6 |
|---|---|---|---|---|---|---|
| disconnect wire points | 28 | 0 | 2 | 1 | 0 | 3 |
| Short section<br>* Number of short shots<br>(number of locations) | 0 | 0 | 2(1) | 2(1) | 0 | 0 |




# Cross-sectional Analysis

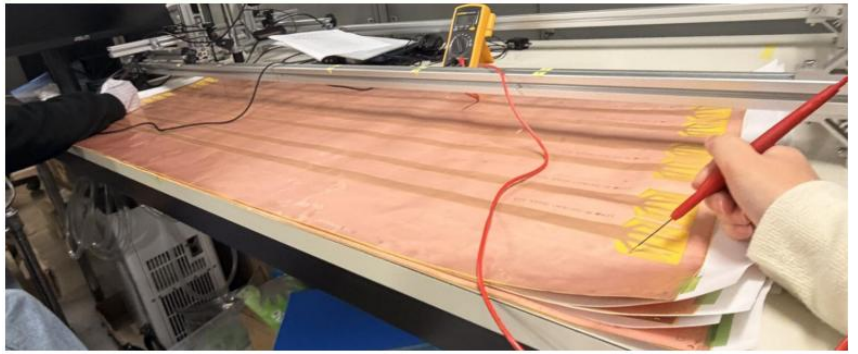



Slight over-etching observed

- **Result**
  - Cross sections of both **12-$\mu$m** and **18-$\mu$m** copper traces were measured.
  - The **12-$\mu$m Cu** traces have an approximately rectangular profile.
  - The **18-$\mu$m Cu** traces exhibit a trapezoidal profile.
- **Interpretation**
  - The 18-$\mu$m copper process is newly introduced for this project.
  - Further optimization of the fabrication process is required.
  - The measured conductor cross sections are close to the design values.
- The measured cross-sectional areas are comparable with the designed value.
  - 12um → 1021um$^2$,  18um → 1134um$^2$

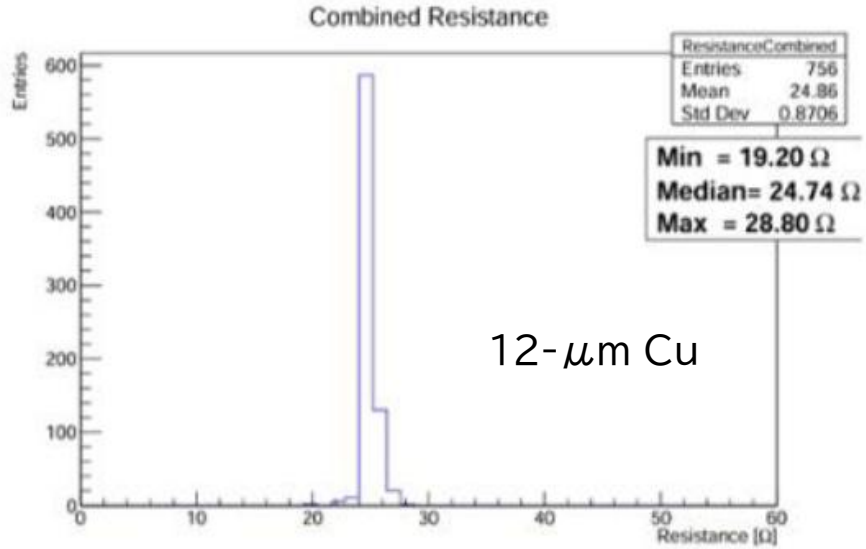
# Electrical Resistance Measurement

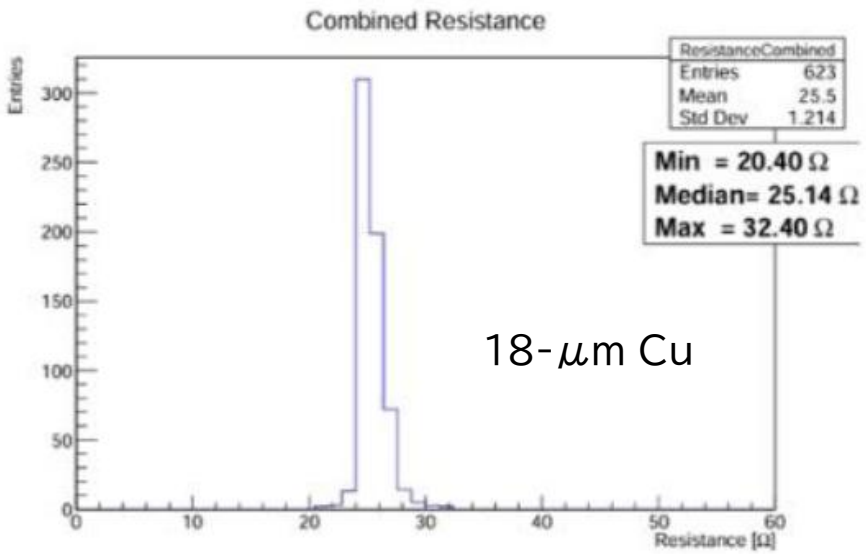


- Results
  - The measured resistances agree well with the design expectations.
  - The 18-$\mu$m Cu traces show electrical performance comparable to the 12-$\mu$m Cu traces.
  - No significant degradation due to the thicker copper was observed.

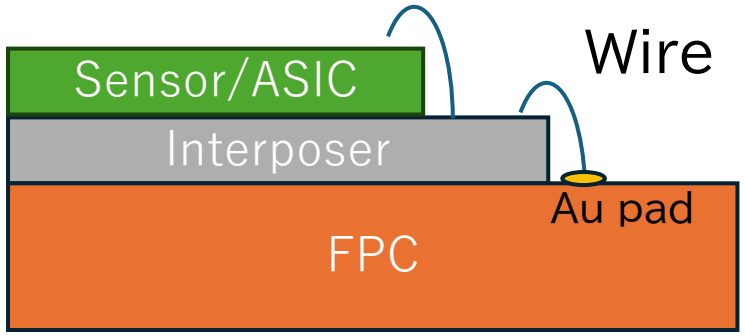
$$R = \rho_{Cu}\frac{L}{S}, \qquad \rho = 1.69 \times 10^{-8}\ \Omega \cdot m, \qquad L = 130\ m,$$
$$S_{12um} = 1021um^2, S_{18um} = 1134um^2,$$

- Ongoing Study
  - Evaluation of line-width uniformity is in progress.
- The results demonstrate the feasibility of using 18-$\mu$m Cu for the baseline design.



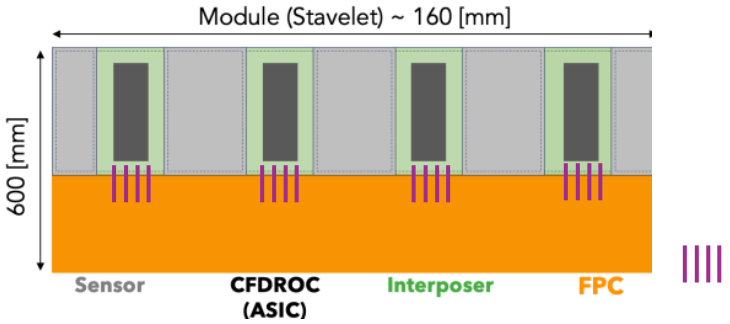



# FPC–Stavelet Integration

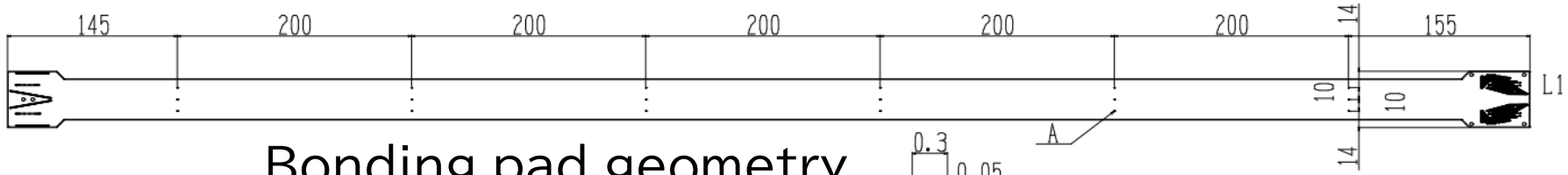



- Prepare the long FPC for integration with the BTOF stavelet.

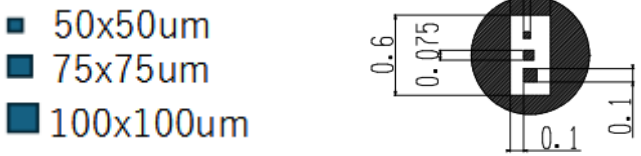
- **Wire Bonding Interface**
  - Gold plating (Ni-Pd-Au) is required on the bonding pads.
  - Test fabrication of gold-plated pads is planned for the next long-FPC prototype.
  - Three bonding-pad geometries will be evaluated.
  - Eight bonding-pad sets will be prepared, corresponding to one stavelet.




- **Industrial Collaboration**
  - Prototype fabrication is being carried out in collaboration with **two PCB manufacturers in Japan and Korea.**




Bonding pad geometry



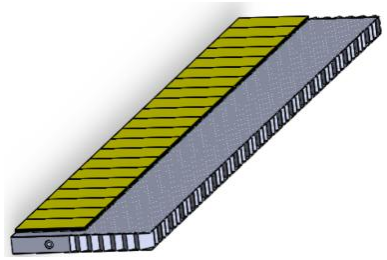

Next milestone: Wire-bond validation

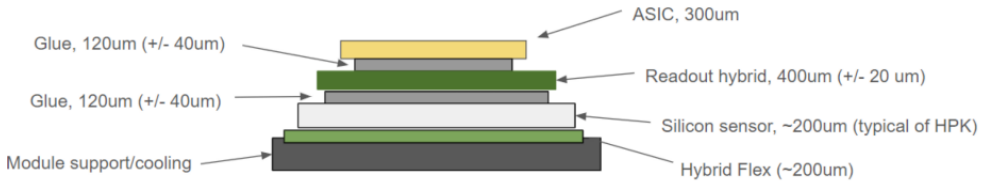
# Thermal Management of the FCFD

The **FCFD** dissipates significant power, making efficient heat removal essential for stable detector operation (~ 10x higher power dissipation than sPHENIX-INTT)

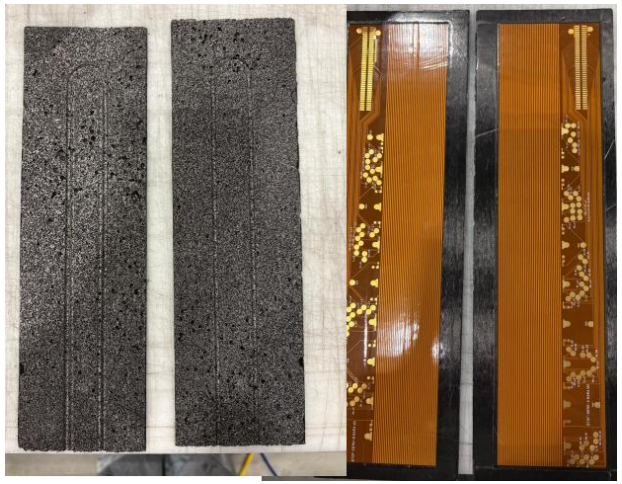
| | Unit power(mW) (32-ch) | Units in FCFD32 | FCFD32_Power(mW) |
|---|---|---|---|
| analog_front (2.5V) | 2 | 32 | 64 |
| analog_front (1.2V) | 1.6 | 32 | 51.2 |
| TDC | 0.2 | 32 | 6.4 |
| eRx | 1 | 2 | 2 |
| eTx | 2 | 1 | 2 |
| Readout16 | 30 | 2 | 60 |
| Serializer | 3 | 1 | 3 |
| fc_decoder | 5 | 1 | 5 |
| data_aligner | 2 | 1 | 2 |
| I2C | 2 | 1 | 2 |
| Total (mW) | | | 197.6 |
| Total (mW) for 2.5V | | | 64 |
| Total (mW) for 1.2V | | | 133.6 |

800mW / 128 ch





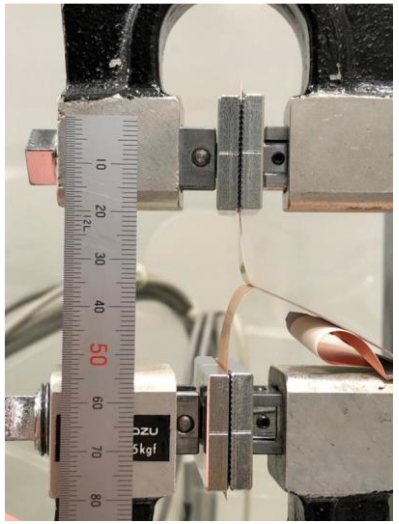

From Review slide



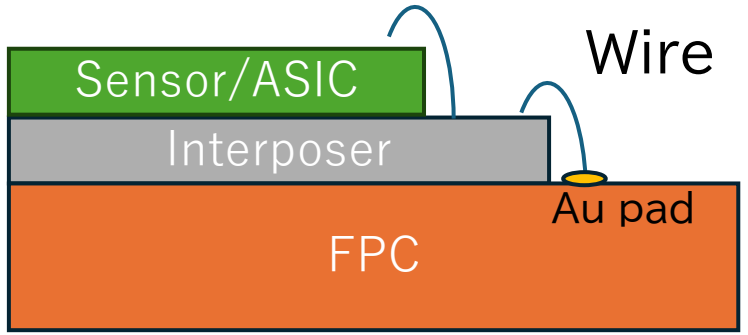
- FEA analysis was done with the previous ASIC and FPC (Thermal Demonstrator)
  - More from Andy's talk
- **Prototype Setup**
  - Use the upcoming **4-layer long FPC** + **Dummy interposer** + **heat source**
  - Measure temperature distribution and heat dissipation.
- Joint study with Purdue,  RIKEN, BNL and Nara WU

# Mechanical Qualification Plan

- **Planned Mechanical Tests**
  - **Peel-strength test** for bonded interfaces
  - **Aging test** for long-term reliability
    - Thermal Sheck test (Low to High temp)
  - **Radiation tolerance test**

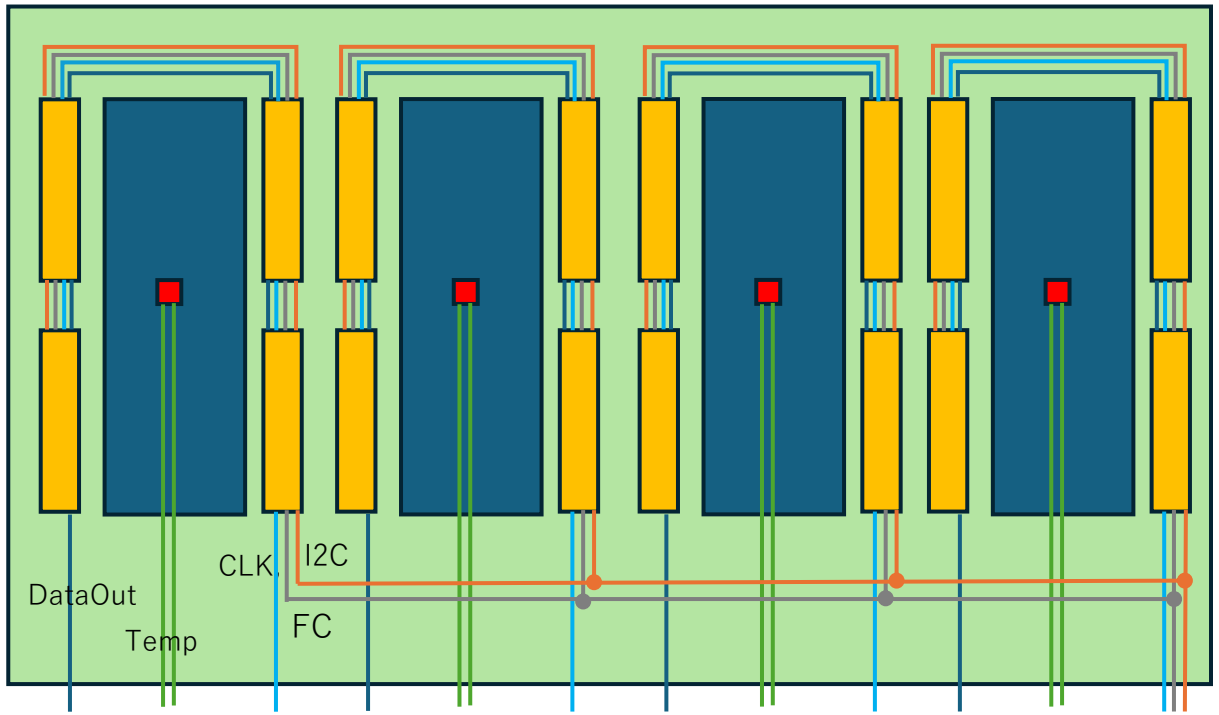


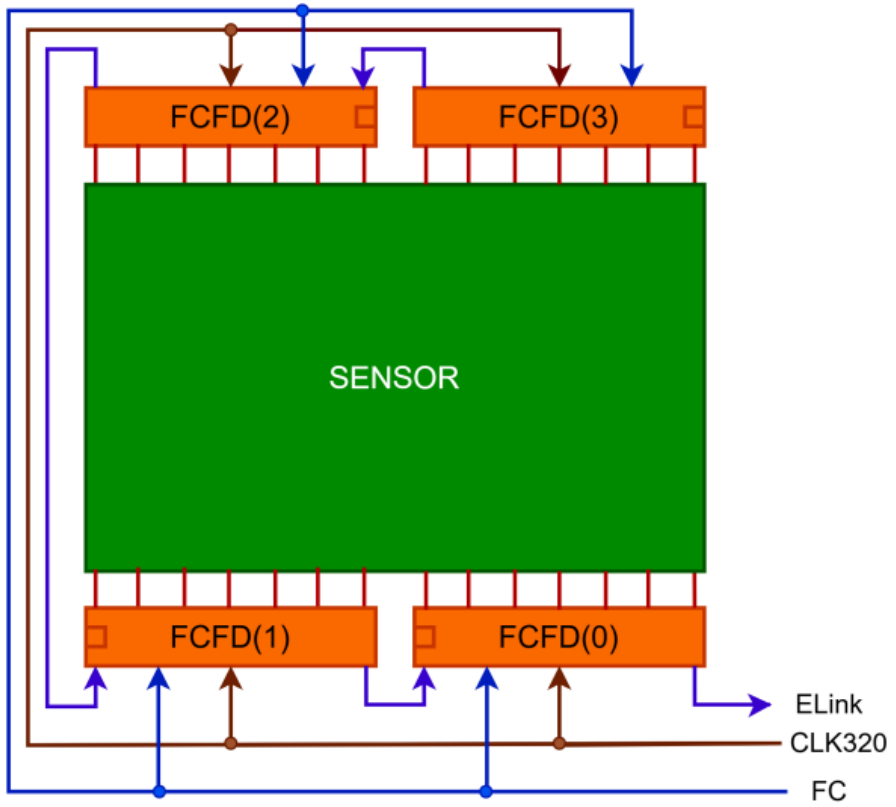
- **Mechanical Challenge**
  - Define the flatness requirement for the long FPC.
  - Establish measurement and acceptance criteria.
  - Optimize the carbon-frame fabrication.
    - The flatness specification for the full-length (260-cm) carbon frame must be defined based on realistic manufacturing capabilities.
    - The mechanical design and fabrication strategy will be developed with reference to the **ATLAS detector experience**.



# Thought on interposer design

From Artur’s slide




- **To be clarified:** Define which signals are buffered inside the ASIC and which are directly routed through the interposer.
- Concepts
  - Only wire bonding pads + passive devices (such as bypass capacitors and termination registers)
  - No active device is mounted on interposer
    - No buffer, no fanout, no LDO to reduce extra parts and materials
  - Two-layer FPC?

# Summary

✓ **Design**

- The baseline **4-layer long-FPC design** has been made for the ePIC BTOF detector.

✓ **Simulation**

- Signal integrity simulations demonstrate that the baseline design satisfies the BTOF requirements.
- The simulated transmission performance is comparable to the successfully operated **sPHENIX INTT FPC.**

✓ **Prototype**

- The first long-FPC prototypes were successfully fabricated.
- Electrical continuity and resistance measurements demonstrate the feasibility of the proposed design (Cu=18um).

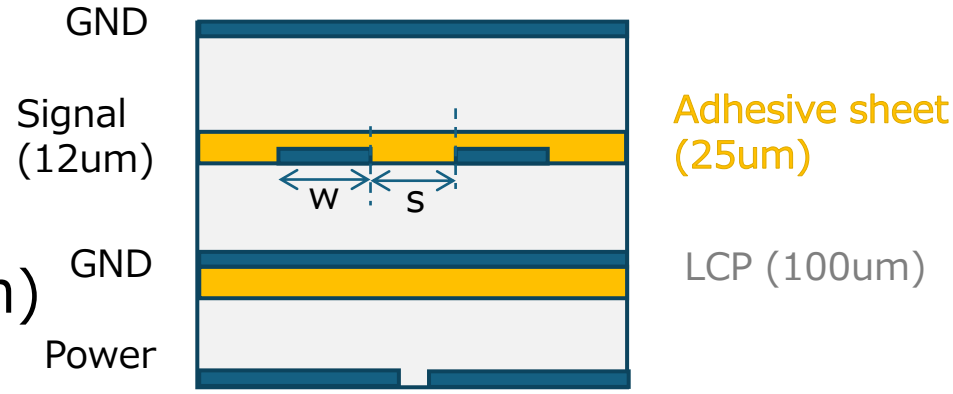
▸ **Next Steps**

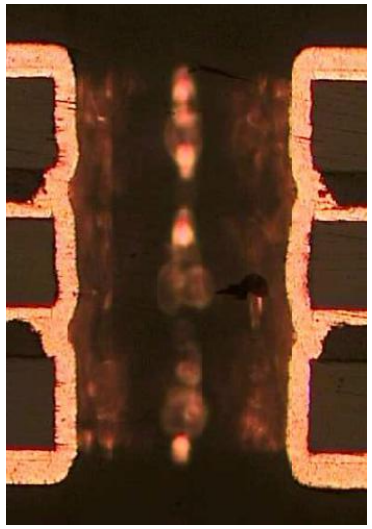
- Fabricate the first **130 cm 4-layer prototype.**
- Validate **signal integrity** using the full-length FPC.
- Demonstrate **wire-bond integration** with the stavelet.
- Evaluate the **thermal performance** of the FCFD/FPC assembly.
- Mechanical qualification of the long FPC.

# BEX

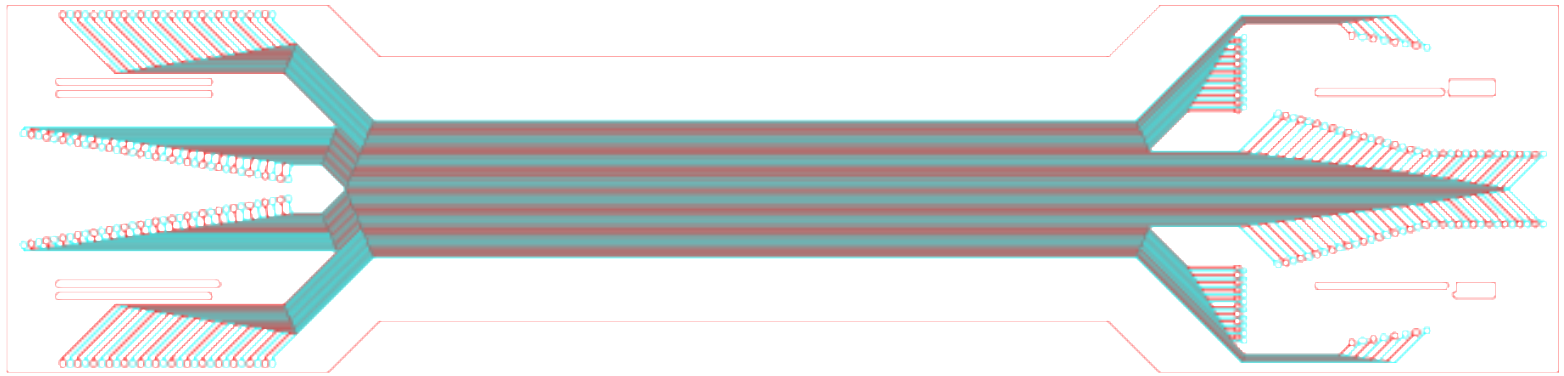
- Cable design (prototype)
  - Dimension (L x W): 120 x 5 $cm^2$
  - 4 layers (signal , 2xGND, PWR):  X = 0.8% $X_0$
    - Cu : 12um thick per layer + 30 um Cu plating on surface
  - Lines : 124 lines (Line and space : 130 & 130 um)
  - $Z_{diff}$ : 100Ω by strip line structure
    - Signal layer is sandwiched by GND layers
  - Liquid Crystal Polymer (LCP) as substrate
    - Less signal loss due to low di-electric constant & tan(δ)
    - Thick LCP available for $Z_{diff}$ : 100um

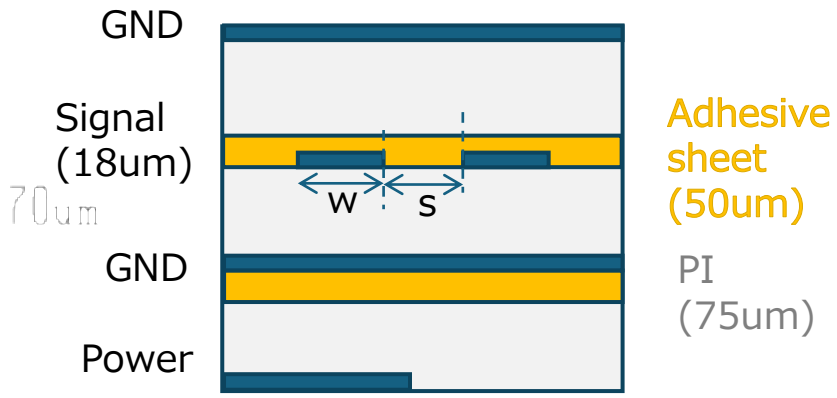
4 layers laminated by the adhesive sheet

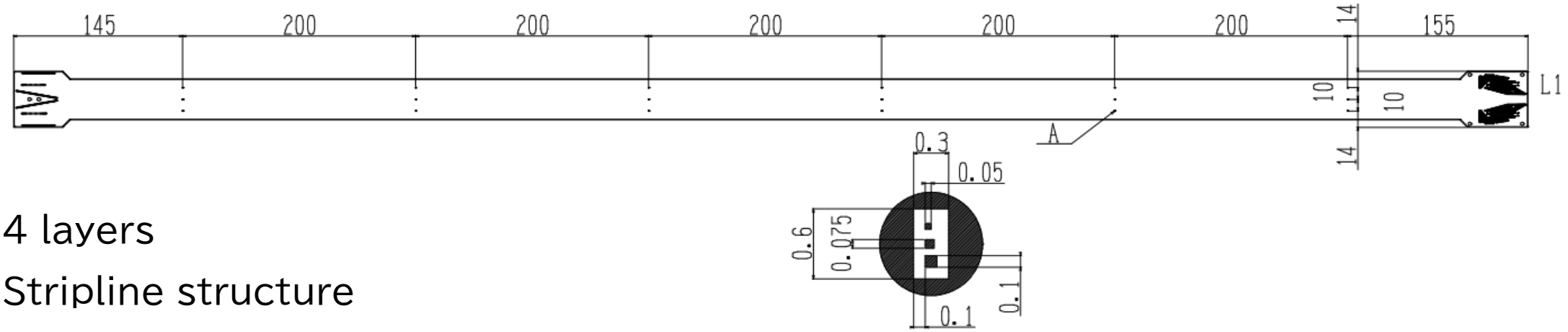


# 130cm 4-layer prototype w/ INTT design

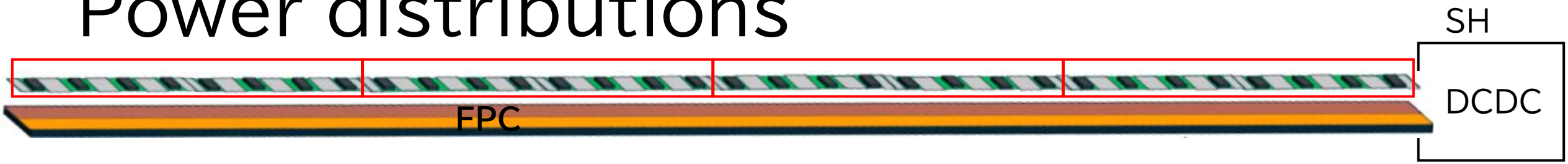


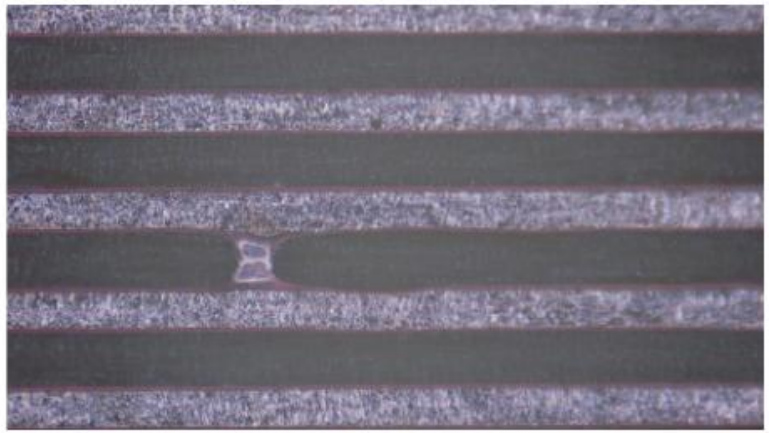
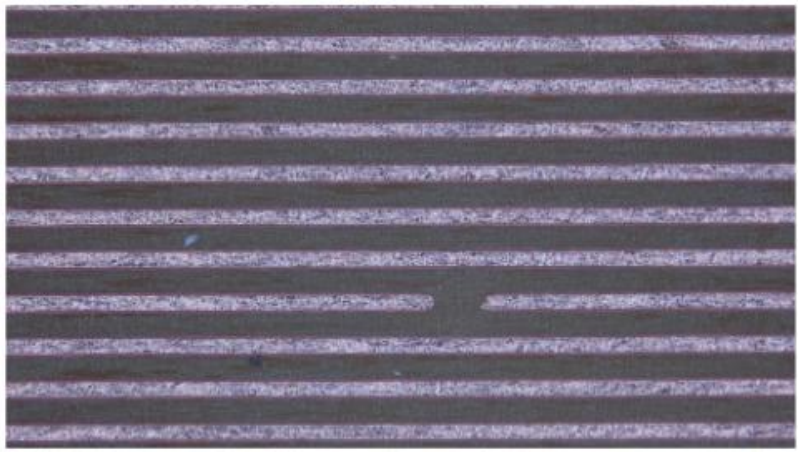
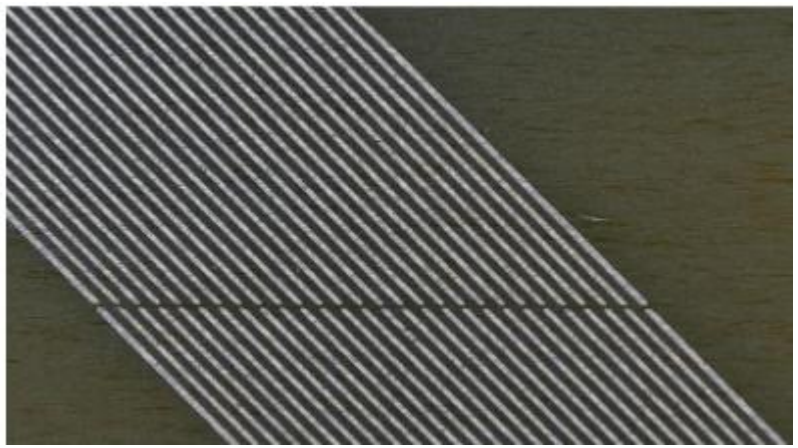



- 4 layers
- Stripline structure
- Cu: 18um, PI: 75um
- Au plating test for wire bonding
- Cover PI

# Power distributions



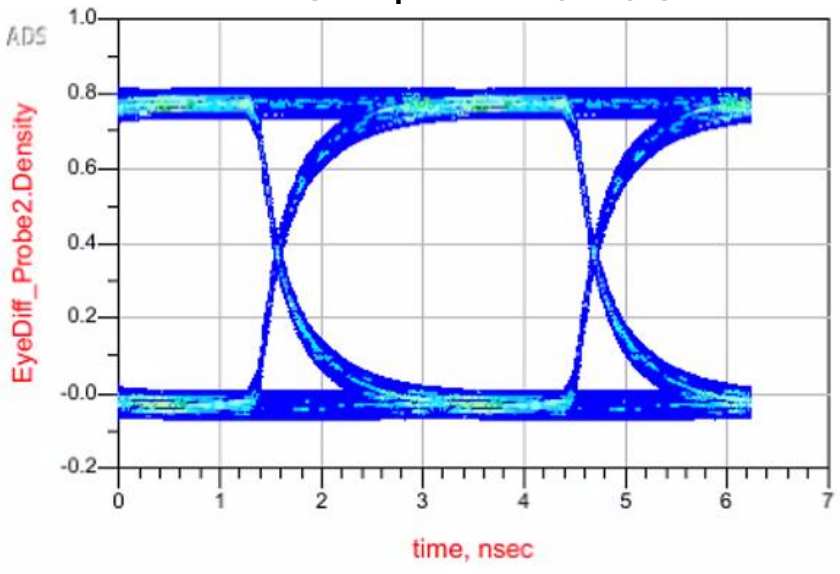




# Simulation results

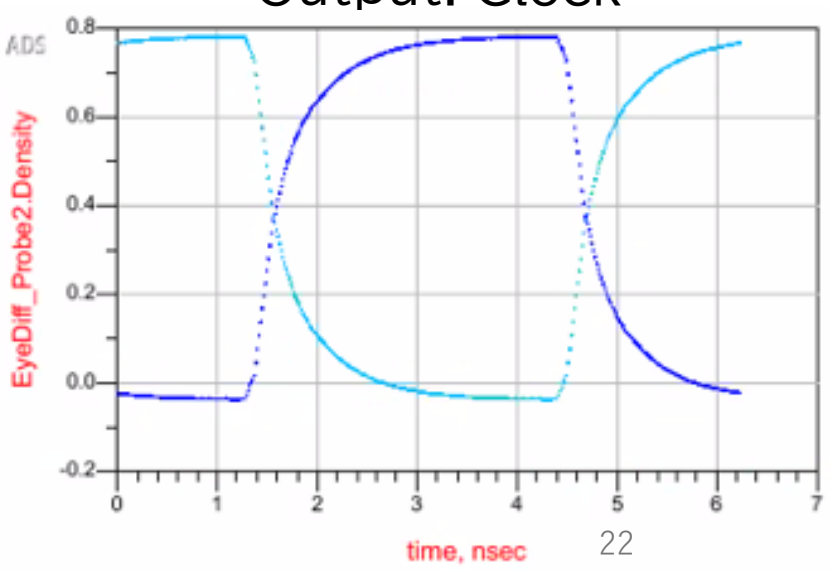
- 1st version SIM done with very simple assumption
  - EM simulation of FPC
- Input: Left
  - 3.125ns pulse (= 320Mbps) with 20ps rise time
  - Random pattern and Clock pattern tested
- Output :
  - Middle:  Random bit pattern
  - Right　: Clock pattern
- Jitter (right)
  - Jitter is width at the crossing of the pulse
  - Looks small for the clock pattern.
  - Extracting the jitter quantitatively

Input


Output: Random

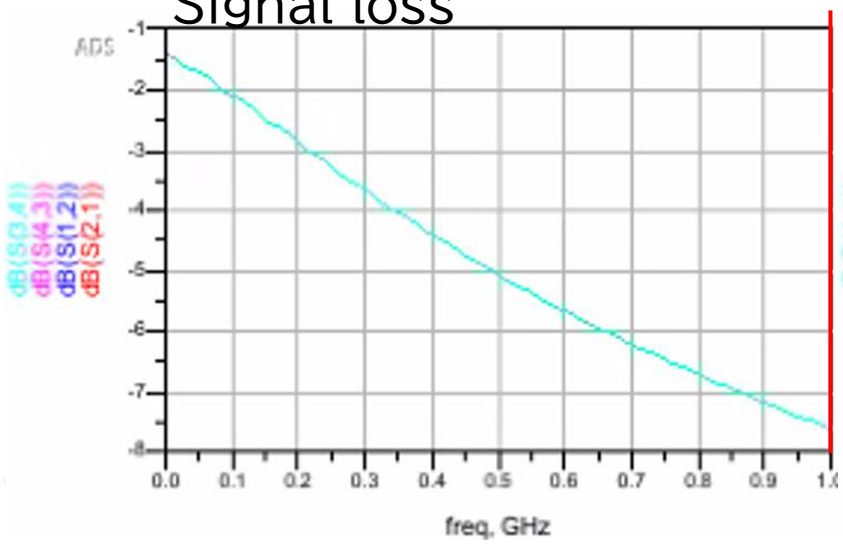



Output: Clock

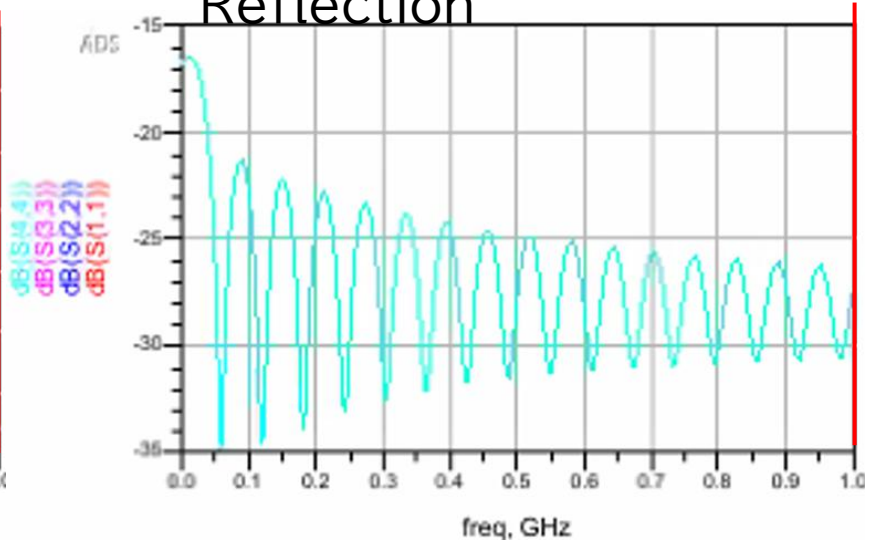


# Signal loss and reflection

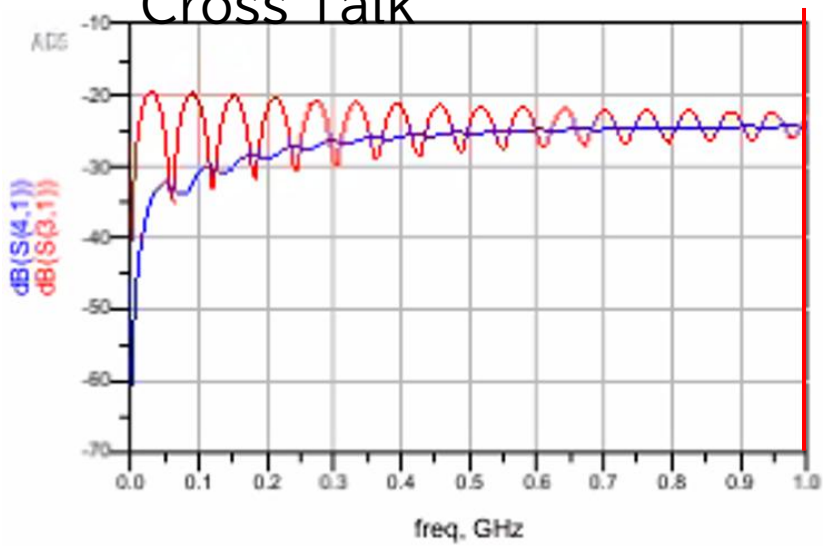
Signal loss




Reflection




Cross Talk




- Evaluate the distortion at 0.8~1GHz (2.5 x reference freq. (320MHz))
  - Signal loss : -7.5 dB = 42%
  - Reflection : -28 dB = 4%
  - CrossTalk : -25 dB = 6%
- These values are good enough for 320MHz clock
  - This is ideal case (simple straight line), redo with the realistic condition
  - lpGBT can use “pre-emphasis” which help the pulse shape
  - Need the driver characteristics of the FCFD driver

Pre-emphasis of lpGBT

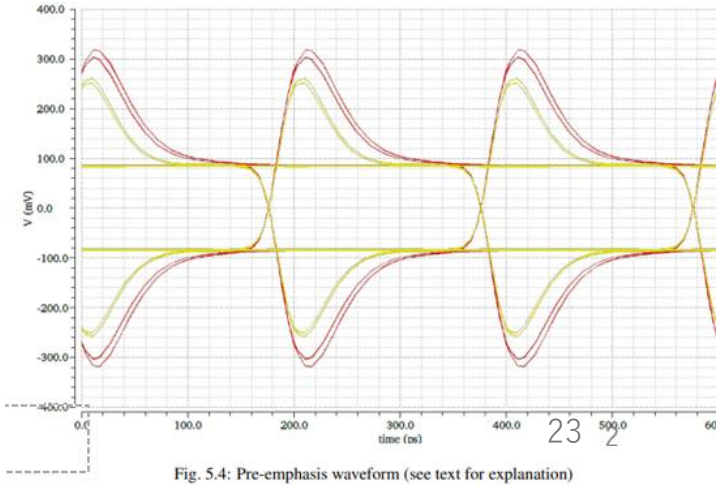



Fig. 5.4: Pre-emphasis waveform (see text for explanation)