LGAD and ASIC QA/QC

added: bTOF QA/QC

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Disclaimer, To Note

- **Objective of QA/QC: ensure functionality of components and production units before they are being installed in the detector**
  - Including mechanical, thermal, electrical performance

QA = quality assurance, measures taken during production
- *can include probing on a small subset of samples*

QC = quality control, to monitor quality of a product or intermediate

Disclaimer, To Note

- **Objective of QA/QC: ensure functionality of components and production units before they are being installed in the detector**
  - Including mechanical, thermal, electrical performance

- *Drawing from experiences – and also personal perception – in LGAD R&D, ATLAS pixel QC*
- *Focusing on electrical and related QA/QC: similar considerations naturally for mechanical and metrological measurements*
- *ASIC-specific details need to be developed further with the respective designers/experts*
- *All the following is targeting the production phase: assuming that signal sharing physics in sensor, analog FE, TDC and ADC path, and their interplay, are ~understood at that point*

Practices

- **Conduct similar measurement protocol in sensor and ASIC QC across all stages of production**
  - Ideally also FF detectors: use the same sensor and ASIC as fTOF

- **Use the same data format (at least, minimum common standard) across all groups involved in TOF**

  - ***Take these into consideration as production database is being customized for TOF!***

- Minimizes duplication of effort
- Facilitates comparison of sensor and ASIC performance as components are being assembled: early identification of assembly steps or procedures that lead to a marked change in behaviour

To be defined

- **Identify relevant tests to be conducted**
- **Decide which points (stages) in detector assembly to conduct them**
- **To balance collecting information with time and labor consumption, consider:**
  - *How probable is failure or change after initial measurement?*
  - *How critical is the impact of said failure or change?*

- **Define cuts: what performance or setting is necessary, and considered a 'usable' component that can be installed in the detector?**

➢ **This interacts with data format and database: the user should upload raw(ish) data from testing, not a Pass/Fail result**

  ➢ Definition of cuts can change as we get further into production and gather experience – only analysis and cut definition needs to change, centrally; users do not need to reanalyse locally or reupload

To be defined

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  - *How critical is the impact of said failure or change?*

Based on the above, tests can be divided (coarsely) into categories:

- Always, on every component
- At certain stages only
- On a subset of components
  - ➢ *Likely more comprehensively in the beginning of production; when a given measurement at a specific stage never shows anomalies, it can be left out or reduced*

ASIC testing

Distinction: global ASIC functionality vs readout performance

- **Global: power, communication, register setting, trigger logic**

- **Channel-level performance: pedestals, noise, threshold, unresponsive channels in analog or digital, interconnect, individual dynamic range, distribution of ADC output, TDC / discriminator output**
  - Homogeneity
  - Yield (how many channels disconnected, elevated noise etc)

Calibrations

- ***Which registers are configurable (e.g. integrator time, preamp gain) on what level? At what stage(s) do they need to be monitored and/or set?***
  - Database needs to account for storing and passing on configuration files to next stage

Examples: always, on every component

Sensor IV

- Leakage current: noise levels, current / power consumption
- Breakdown voltage: premature breakdown renders sensor unusable and increases current draw. Change from previously ‘good’ sensor to ‘bad’ may hint at problems in assembly procedure step

ASIC start-up

- V-I: can chip be turned on / powered at all
- V_{in}, A, VDD(A,D): power rails at required levels, no shorts
- Register setting (and readback?)
- Data transmission test: (eye opening width), correct transmission word with start and end blocks, Idle character as expected

Examples: only on bare components, fraction of components

Sensor CV: depletion, DC and AC capacitance

- Bare sensors: DC capacitance + e.g. some subset of channels for AC capacitance; variation of capacitance within same sensor not expected, change over assembly not expected

Gain: potential for nonuniformity across wafer

- Subset of sensors from different locations of the wafer to establish a ‘range’

TDC jitter (w. clock)?:

- not necessary on every ASIC after initial probing, but has do be monitored on stave level

Global trims (if any): determine before wirebonding

Before wirebonding

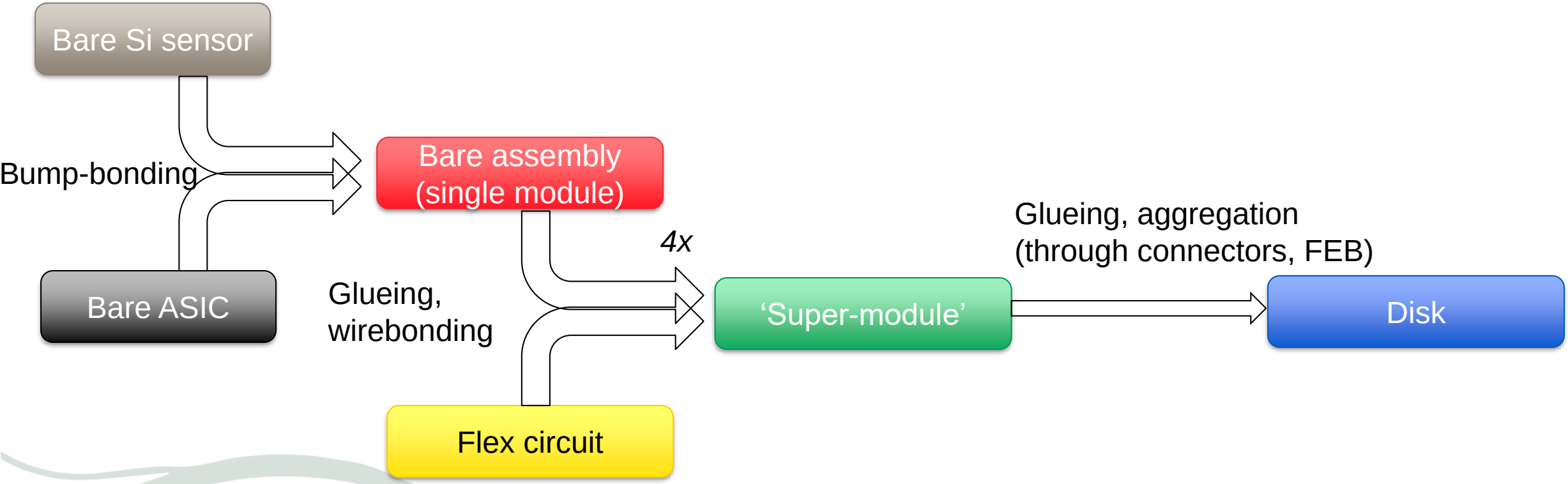
- Large number of channels (128 – 256, 1024) – not feasible to measure individually, except for very small number of individual channel probing
- Very valuable to probe sensors and ASICs before glueing and wirebonding (time-consuming step, complicated or impossible to rework if problems are identified afterwards)

➢ **Use of probe cards**

➢ **Needed cards: pixel sensor, strip sensor, ASIC**

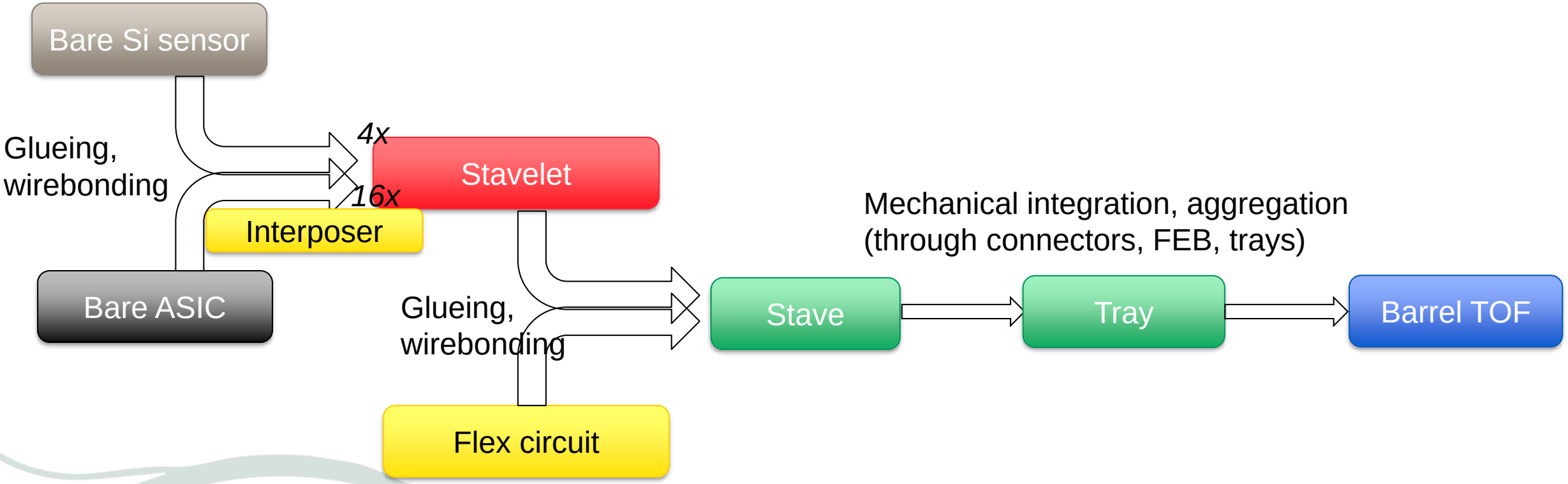
fTOF (and similarly FF)

Leaving out mechanical structures



bTOF

Leaving out mechanical structures



Questions related to QC

At which stages to include signal injection including sensor, and how to accomplish this?

- Laser? Sr-90 source? X-rays?
- Charge injection through ASIC may not identify disconnected channels correctly, or other full-chain phenomena (cf. Alex's talk)
- Anything beyond a stavelet is too large to fit into conventional enclosures

At what temperature shall tests be conducted?

- TOF does not expect cold temperatures and a respective strong impact on assembly through thermal stress, but some repetitions of circulating coolant with front-ends switched off should be considered
- ➢ **E.g., testing at RT / 25 C, and at 10 C? 'Cycling'?**

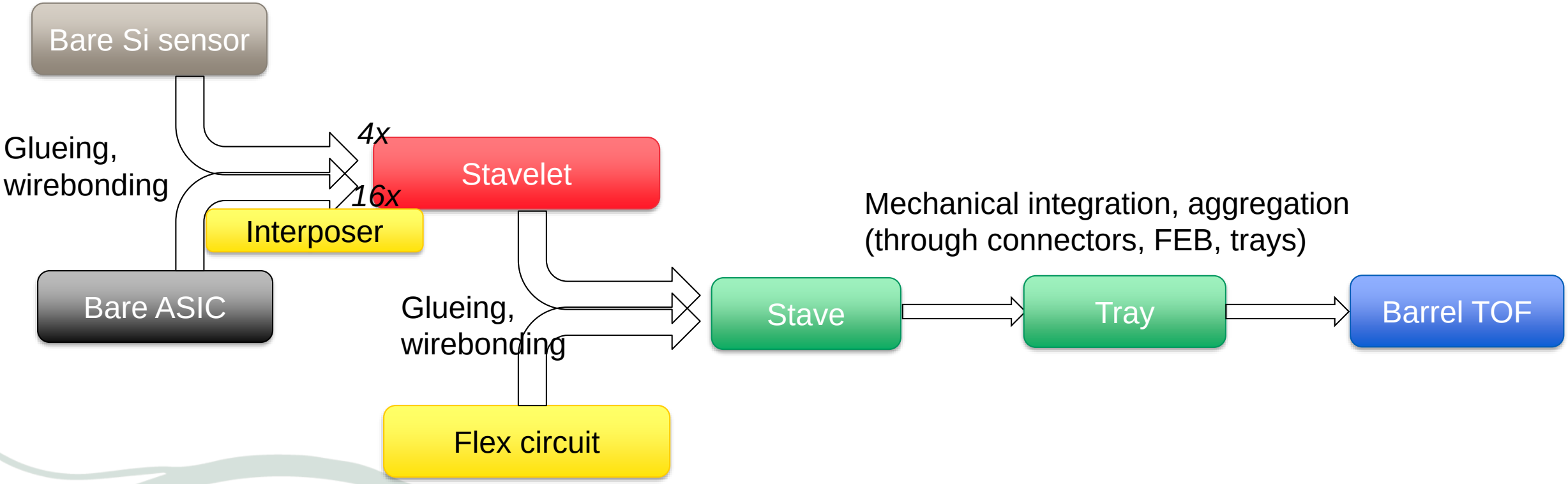
Questions related to QC

Continuous operation / readout, as would be the case in the detector – is a long-term stability or readout test foreseen? At which stage(s)?

bTOF

bTOF

Leaving out mechanical structures



Sensor

Dicing
Shipment: HPK -- UCSC, Hiroshima, Riken, Taiwan NCU

Shipment between sites?

Glueing, wirebonding

Shipment: UCSC, Hiroshima, Riken, Taiwan NCU – Purdue/BNL

Bare Si sensor	Bare Si sensor	Stavelet	Stavelet	Stave	Tray	Barrel TOF

At vendor – before dicing

Split up this stage between glueing and wirebonding??

IV (all sensors) **CV** (all sensors, all channels)	**Visual inspection** (all sensors) **Metrology**: • Sensor X,Y (all sensors) • Sensor thickness (2-5 / wafer) **IV** (all sensors) **CV** (selection of sensors; *OR* DC-CV all sensors, AC-CV on N sensors per wafer?)	**Visual inspection** (all sensors) **Metrology**: (?) • Position X, Y? • Rotation? **IV** (all sensors) **Charge injection measurement (how many units?)**	**Visual inspection** (all sensors) **IV** (all sensors)

To follow up later

Sensor

Suggestion: set aside 1-2 sensors per wafer for more extensive CV measurements and to be mounted and bonded on other LGAD test boards for gain and charge sharing measurements

- Assume that these will *not* return to normal assembly
  - Conducting this on production sensors is additional handling and contamination risk, time-consuming

ASIC

Dicing
Shipment: XXX -- UCSC, Hiroshima, Riken, Taiwan NCU

Shipment between sites?

Glueing, wirebonding

Shipment: UCSC, Hiroshima, Riken, Taiwan NCU – Purdue/BNL

Bare ASIC	Bare ASIC	Stavelet	Stavelet	Stave	Tray	Barrel TOF
At vendor – before dicing		***Split up this stage between glueing and wirebonding??***				
tbd?	**Visual inspection** (all chips) **Metrology**: • ASIC X,Y (all chips) • Thickness? (5-10 / wafer) **ASIC initial QC, register config** (all chips)	**Visual inspection** (all chips) **Metrology**: (?) • Position X, Y? • Rotation? **Wirebonding inspection, pull test** **ASIC follow-up QC tbd**	**Visual inspection** (all chips) **ASIC** power-up, transmission test			

To follow up later

FPC

Shipment: Korea -- UCSC, Hiroshima, Riken, Taiwan NCU

Shipment between sites?

Shipment: UCSC, Hiroshima, Riken, Taiwan NCU – Purdue/BNL

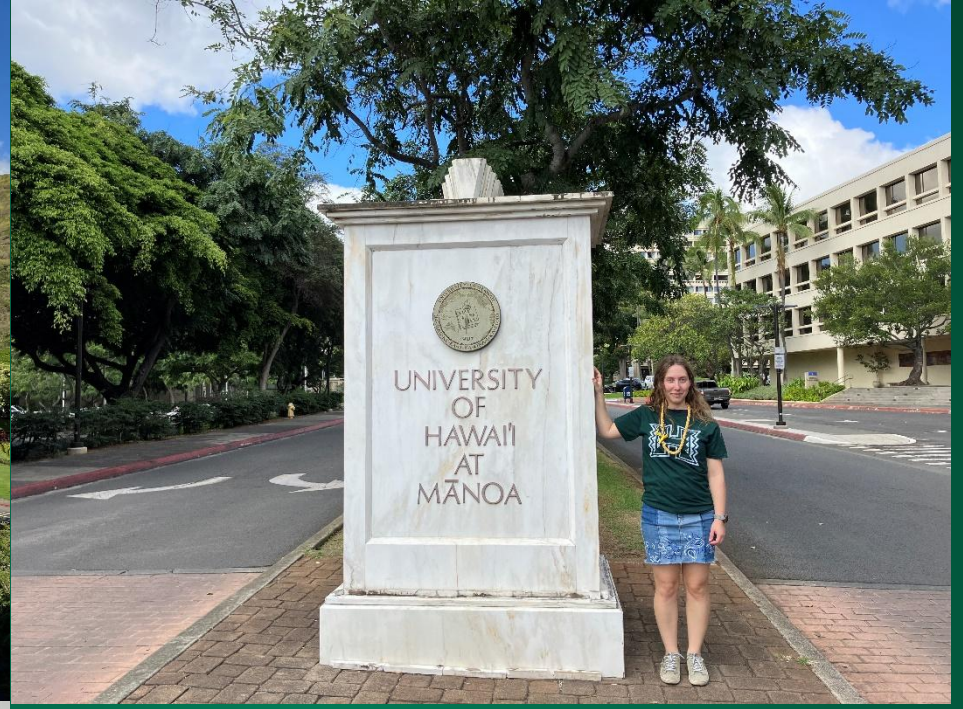
Glueing, wirebonding

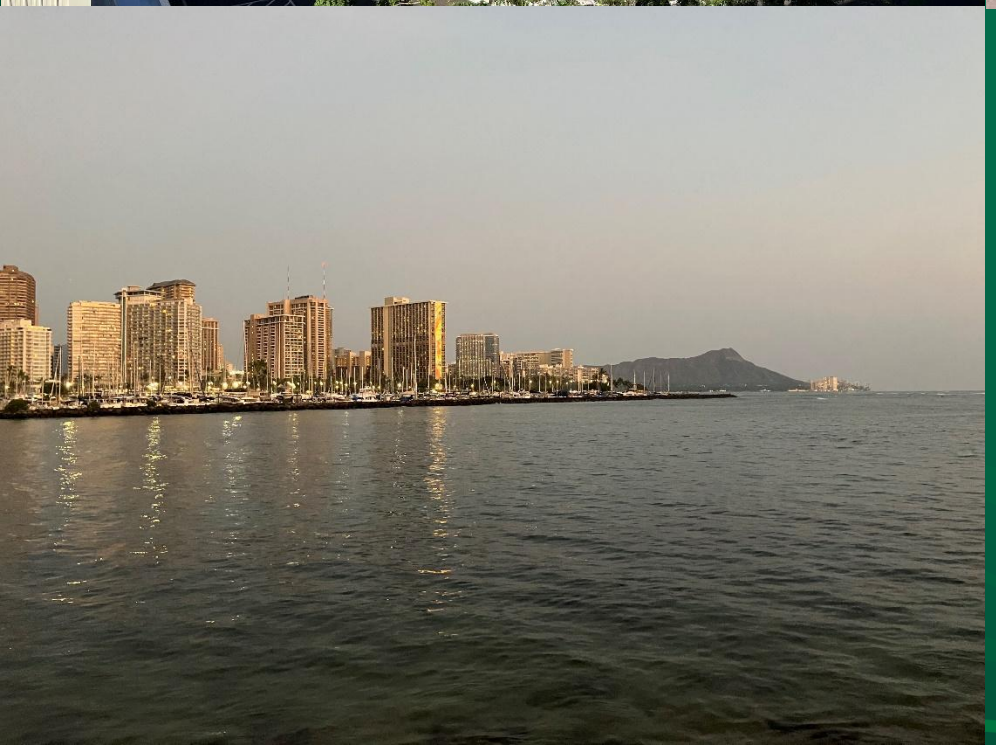
Stavelet FPC	Stavelet FPC	Stavelet	Stavelet	Stave	Tray	Barrel TOF

At vendor?

Split up this stage between glueing and wirebonding??

tbd?	**Visual inspection** (all flexes) **Metrology** (all flexes) • Mass • Thickness (at M points?) • Flex size X,Y • Trace width (at M points?) **Flex electrical** Trace resistance Trace impedance? Capacitance? (what freq's?)	**Visual inspection** (stavelet overall) **Metrology**: • Gap X,Y between sensors and ASICs? • Position X,Y of components? • Flatness (thickness of final silicon+glue+flex) **Overall IV – power consumption** **Thermal inspection: warming?**	**Visual inspection** (stavelet overall) **Overall IV – power consumption** **Thermal inspection: warming?**	*To follow up later*





COLLEGE OF ENGINEERING
UNIVERSITY of HAWAI'I at MĀNOA

Thank you!

fTOF

Bumping, dicing

Shipment: vendor -- ORNL or UH

Shipment: UCSC, Hiroshima, Riken, Taiwan NCU – Purdue/BNL

Flip-chip bonding

Glueing, wirebonding

Bare ASIC	Bare ASIC	Hybrid assembly	Super-module	Disk subunit / support	Disk / fTOF
On wafer					
Tbd	**Visual inspection** (all sensors) **Metrology**: ASIC X,Y (all chips) **IV** (all sensors) **CV** (selection of sensors; *OR* DC-CV all sensors, AC-CV on N sensors per wafer?) Sensor thickness (2-5 / wafer)	**Visual inspection** (all sensors) **Metrology**: (?) • Gap X,Y between sensors • Rotation • Flatness? (thickness of final sensor+glue+flex) **IV** (all sensors)	**Visual inspection** (all sensors) **IV** (all sensors)		