AncASIC MPW1 Test at LBL - Updates

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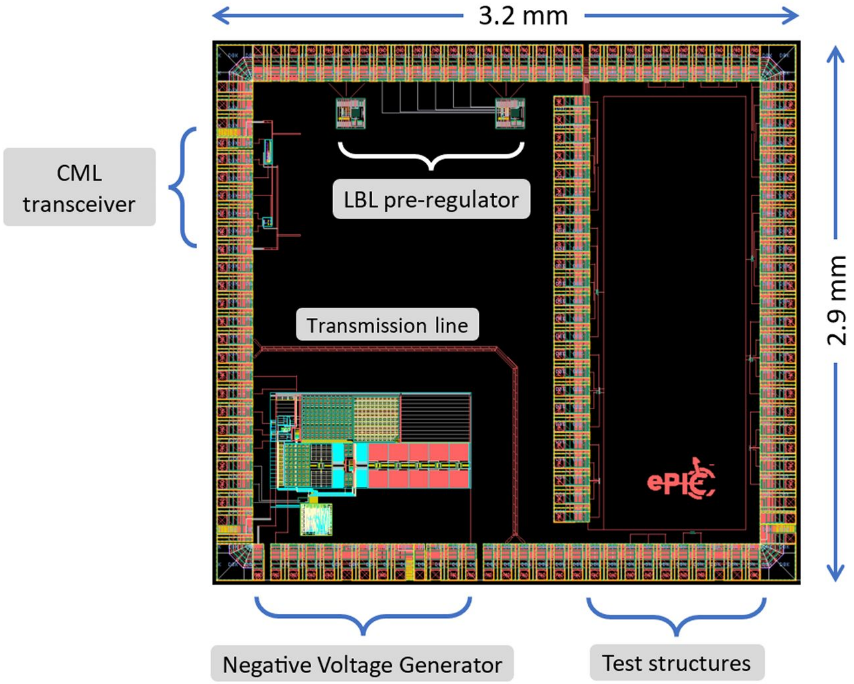
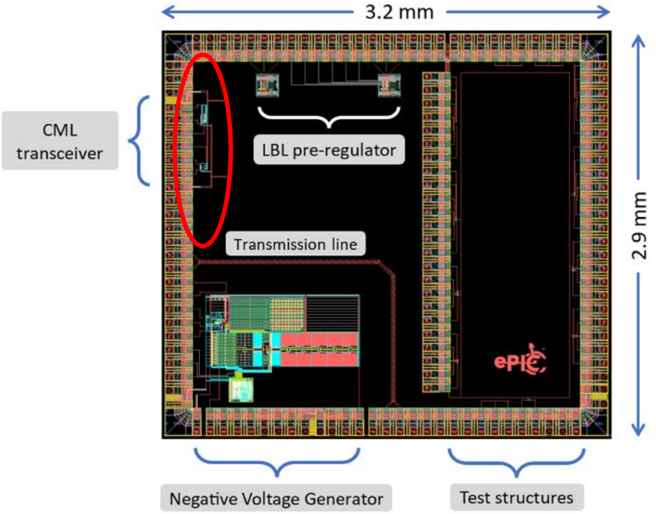
*Thanks to the BNL design team and Amanda Krieger at LBL for useful suggestions/discussions

AncASIC MPW1



- ❑ A passthrough differential transmission line
- ❑ [Current-mode logic (CML) transmitter and receiver]
- ❑ [SLDO Pre-regulator]
- ❑ [An I2C controller]
- ❑ [Negative voltage bias generator (NVBG)]
- ❑ Test devices (MOSFET, BJT, resistor, etc.)

CML Transceiver



➔ A summary of tests performed till now

Test	Details	Status
Single chip	Transceiver output at Rx and Tx, time delay, eye diagram	✔
Daisy chain	Transceiver output, time delay, eye diagram	✔

Instrument:

- Power supplies and batteries to set different voltage
- Signal generator
- Oscilloscope

CML Transceiver

- ❑ Designed to check AC vs DC-coupled slow control links between adjacent serially-powered AncASIC chips

Receiver (Rx)

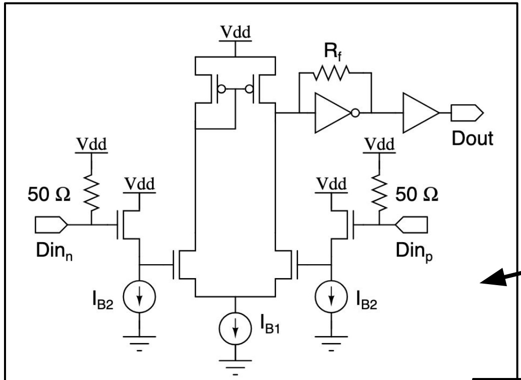


Figure 14: CML receiver.

Transmitter (Tx)

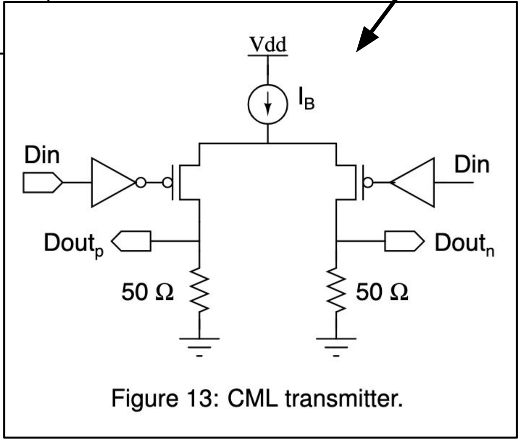
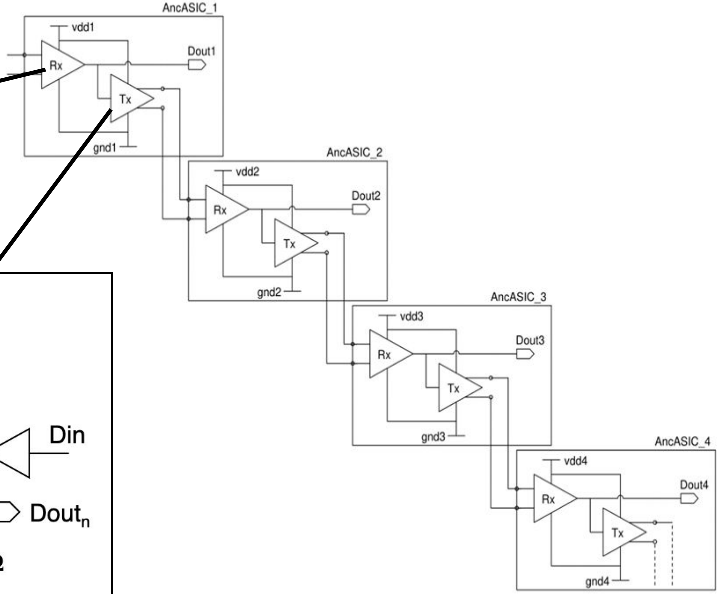


Figure 13: CML transmitter.



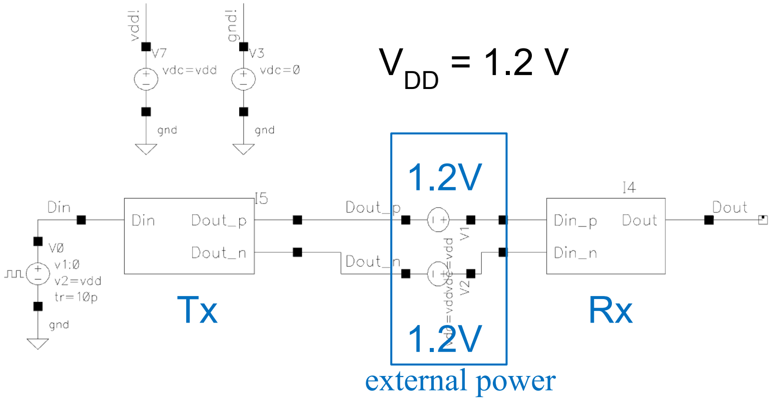
Daisy-chain test structure

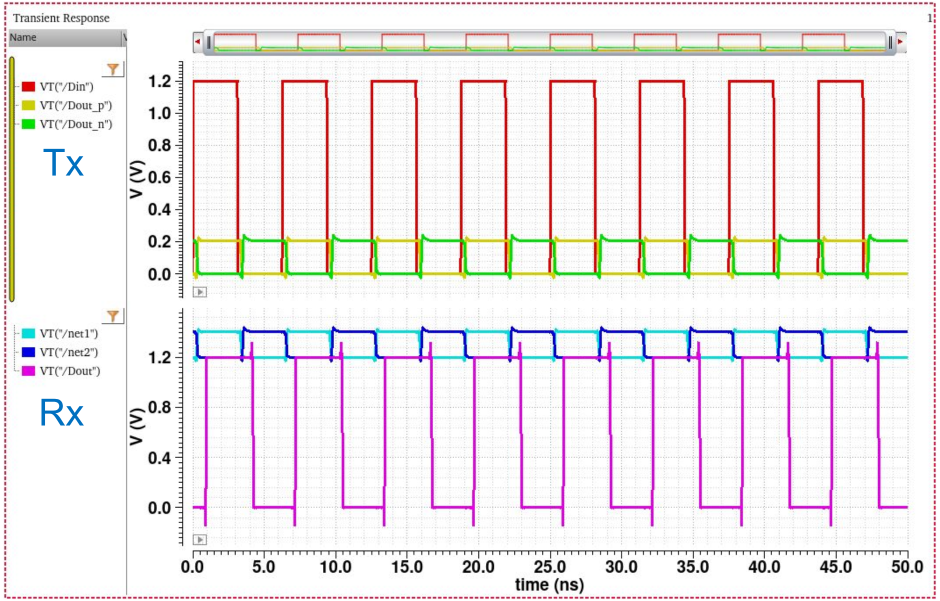
CML Transceiver

Simulation of a DC-coupled link using a simple repeated 0/1 pattern

[slide from Soumyajit]

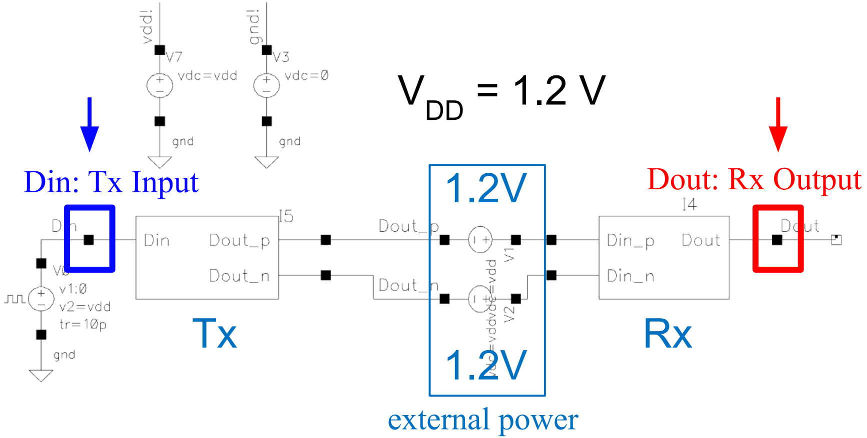
V_{DD} = 1.2 V





- Transmitter: Output swing (into a matched load), Vout = 200 mVpp
- Receiver: Output swing, rail-to-rail (1.2 V)

CML Transceiver
(Single chip)



Din: Tx Input

V_{DD} = 1.2 V

Dout: Rx Output

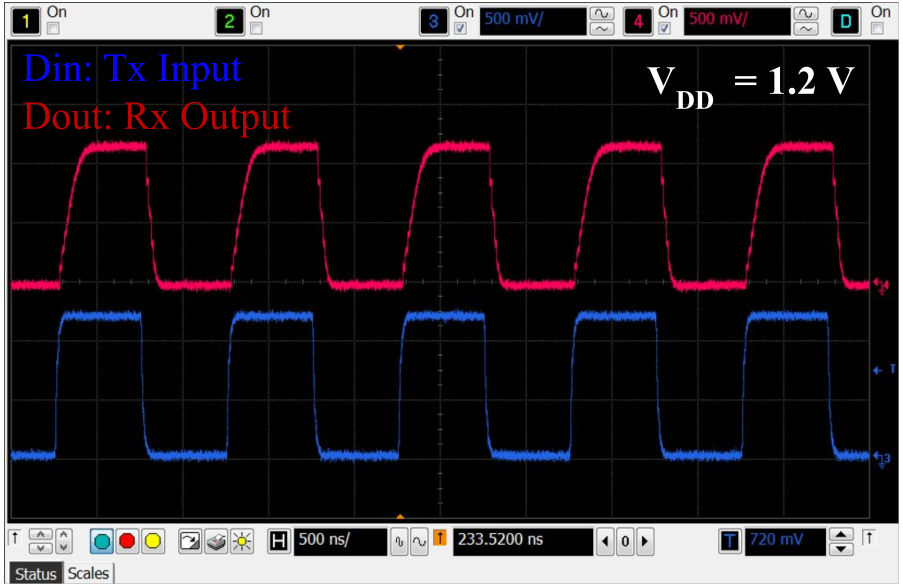
1.2V

1.2V

Tx

Rx

external power



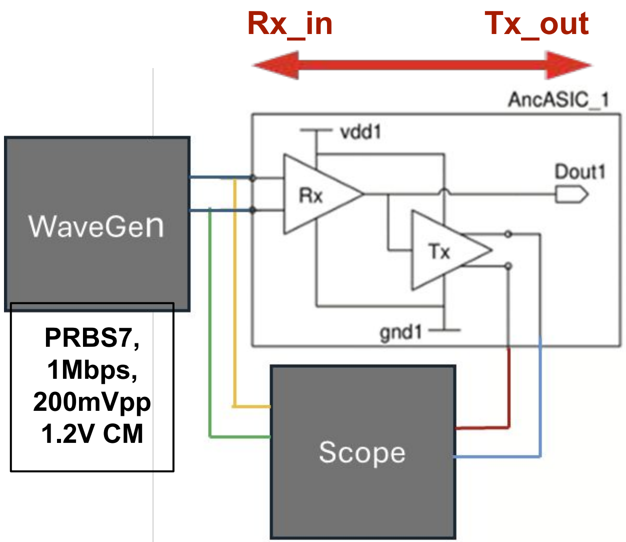
Din: Tx Input

Dout: Rx Output

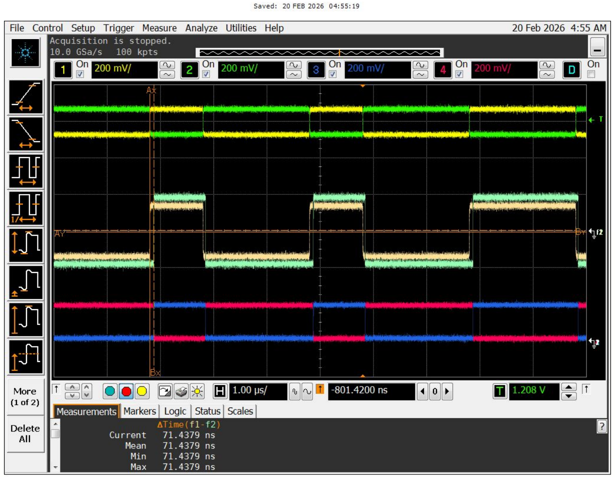
V_{DD} = 1.2 V

- Single ended Tx input: rail-to-rail 0-1.2V
- Single ended Rx output: rail-to-rail 0-1.2V at V_{DD} = 1.2 V
- Matched expected value from the simulation

CML Transceiver (Single chip)

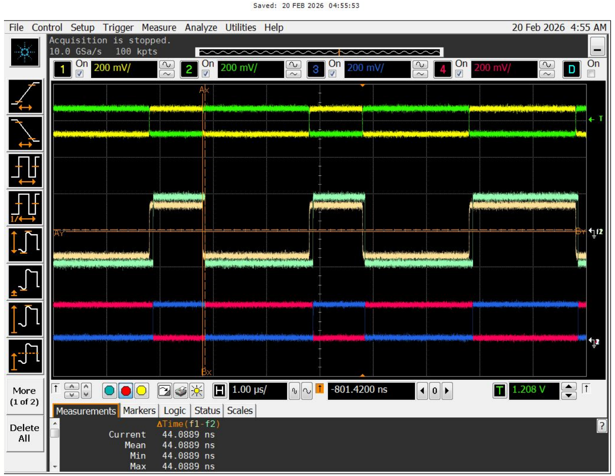


PRBS7,
1Mbps,
200mVpp
1.2V CM



```
Acquisition is stopped.
10.0 GSa/s   100 kpts

        ΔTime(f1-f2)
Current  71.4379 ns
Mean     71.4379 ns
Min      71.4379 ns
Max      71.4379 ns
```



```
Acquisition is stopped.
10.0 GSa/s   100 kpts

        ΔTime(f1-f2)
Current  44.0889 ns
Mean     44.0889 ns
Min      44.0889 ns
Max      44.0889 ns
```

f1 = ch1 - ch2 = diff Rx Input

f2 = ch3 - ch4 = diff Tx output

rise Δtime(f1-f2) ~ 71 ns

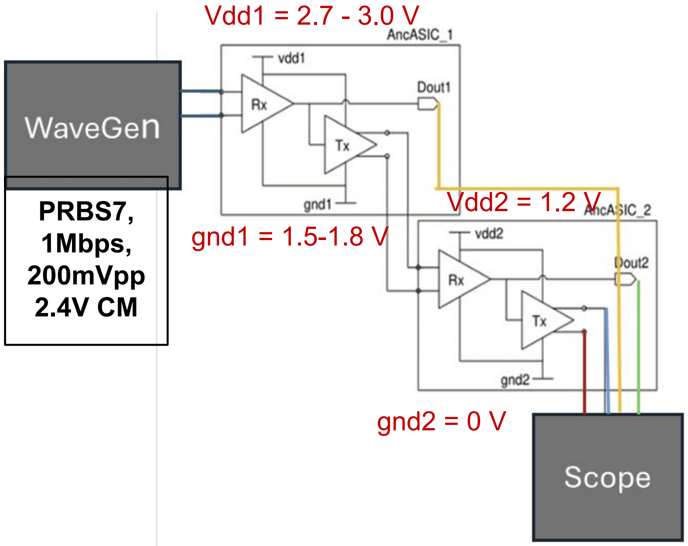
fall Δtime(f1-f2) ~ 44 ns

- 50% threshold used in extracting Δtime, two 4 ft cable contribute ~ 10 ns delay

➔ Delay between Rx Input and Tx Output, ~ 61 ns (rising edge) and ~ 34 ns (falling edge)

- **RX → TX currently goes through an external connection, adding delay**
- **No drive strength on the CMOS side at this stage**
- **Final design will integrate the RX–TX chain internally with sufficiently buffered**

CML Transceiver (Daisy chain)



- **Daisy chain with two AncASIC MPW1s at different potentials connected via DC-coupling**

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Acquisition is stopped.
10.0 GSa/s 200 kpts

1 On 500 mV/ 2 On 500 mV/ 3 On 200 mV/ 4 On 200 mV/ D On

H 2.00 µs/ 0.0 s T 520 mV

0.3 V difference between two AncASIC

Acquisition:
Sampling Mode Real Time
Capture Time 20.0 µs
Effective Res 100 ps/pt
Bits Of Res 8 bits

Trigger:
Mode Edge (↑)
InfiniiScan NA

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Acquisition is stopped.
10.0 GSa/s 200 kpts

1 On 500 mV/ 2 On 500 mV/ 3 On 200 mV/ 4 On 200 mV/ D On

H 2.00 µs/ 0.0 s T 520 mV

0.6 V difference between two AncASIC

Acquisition:
Sampling Mode Real Time
Capture Time 20.0 µs
Effective Res 100 ps/pt
Bits Of Res 8 bits

Trigger:
Mode Edge (↑)
InfiniiScan NA

gnd1 = 1.5 V, Vdd1 = 2.7 V
gnd2 = 0 V, Vdd2 = 1.2 V

Dout2 (offset: 0V): 0 - 1.2 V
Dout1 (offset: 1.5V): 1.5 - 2.7 V
Dout_p (AncASIC_2 Tx): 200 mVpp
Dout_n (AncASIC_2 Tx): 200 mVpp

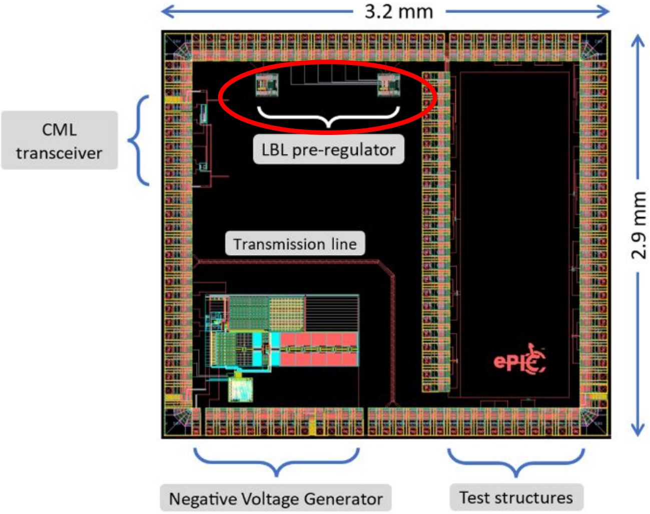
gnd1 = 1.8 V, Vdd1 = 3.0 V
gnd2 = 0 V, Vdd2 = 1.2 V

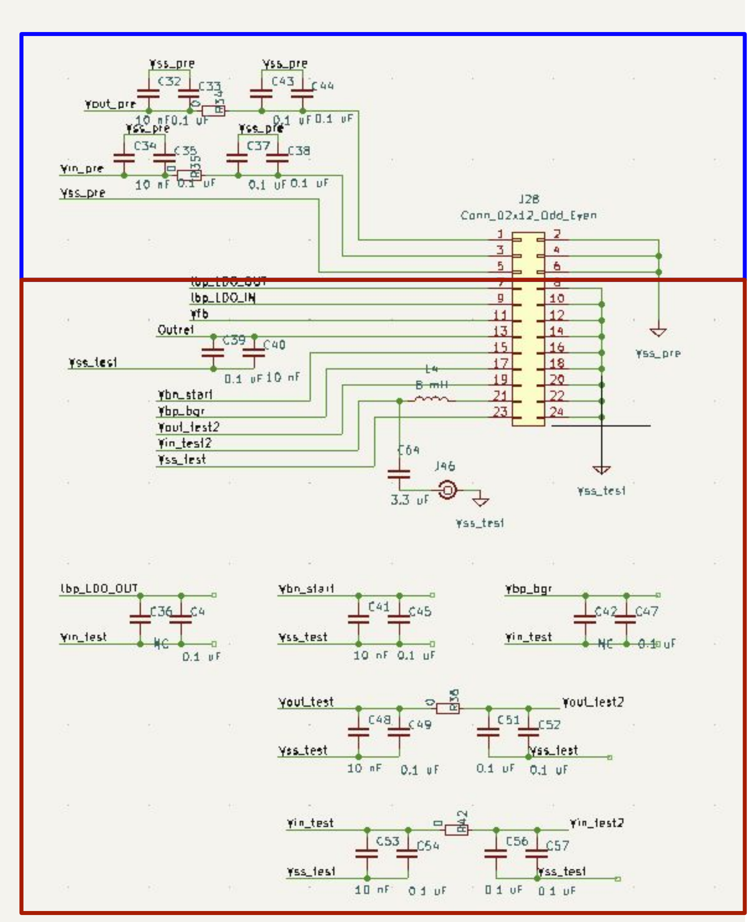
Dout2 (offset: 0V): 0 - 1.2 V
Dout1 (offset: 1.5V): 1.8 - 3.0 V
Dout_p (AncASIC_2 Tx): 200 mVpp
Dout_n (AncASIC_2 Tx): 200 mVpp

*Wavy structure in the Dout1, due to capacitors between the ground of the board and SMA cable ground of AncASIC (Din_p/n, Dout_p/n, Dout, Din), to prevent a direct short between the two boards at different potential when powered.

SLDO Pre-Regulator

Single chip has two pre-regulators,
1. Version that will go to the final chip
2. Another for debug purpose



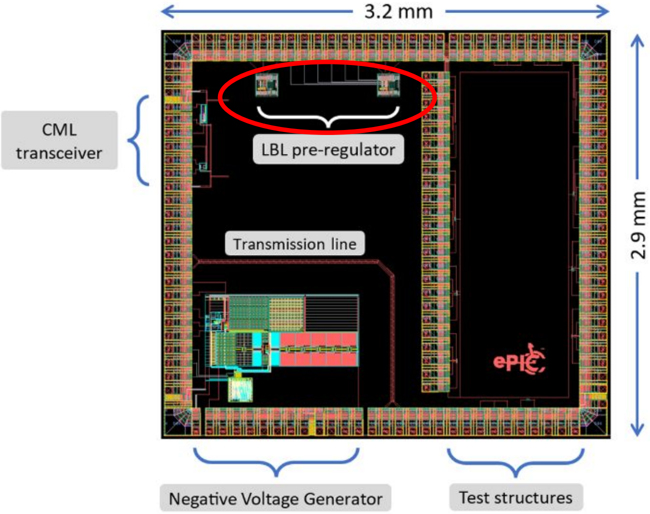


Pre-regulator #1

Pre-regulator #2

SLDO Pre-Regulator

Single chip has two pre-regulators,
1. Version that will go to the final chip
2. Another for debug purpose



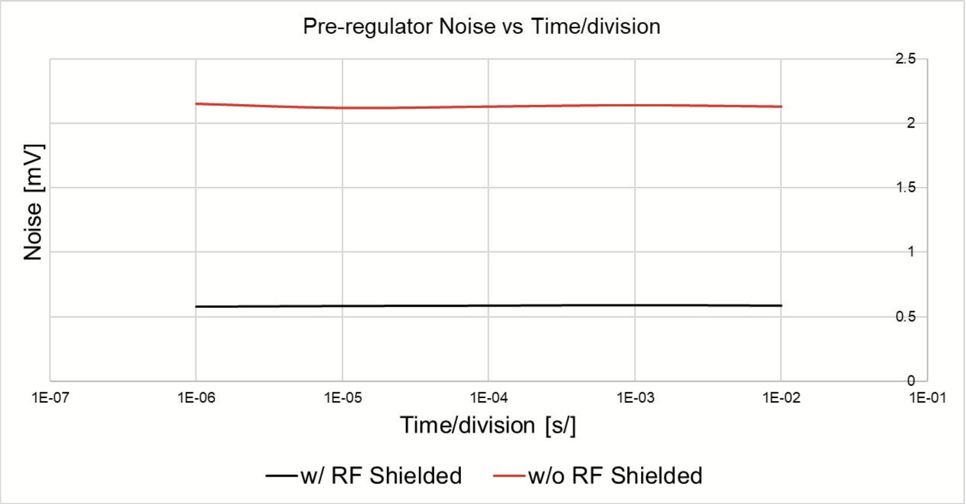
Instrument:
- Power supply, Oscilloscope
- Signal generator to power VDD with ripple
- Environmental chamber for temperature test
- RF Shielding Room for noise measurement

➔ A summary of tests performed till now

Test	Swept parameter	Status
Ramp-up	Different ramp-up time for Vin	✔
	Different capacitive loads	✔
	Different temperature	✔
Output noise and ripple	Different time scale/division	✔
Power supply rejection ratio (PSRR)	Amplitude of the injected noise and frequency	✔
Transient Response	load current (I_L)	ongoing
Repeat the above tests for the pre-regulator #1 on the same chip		debugging

Noise:

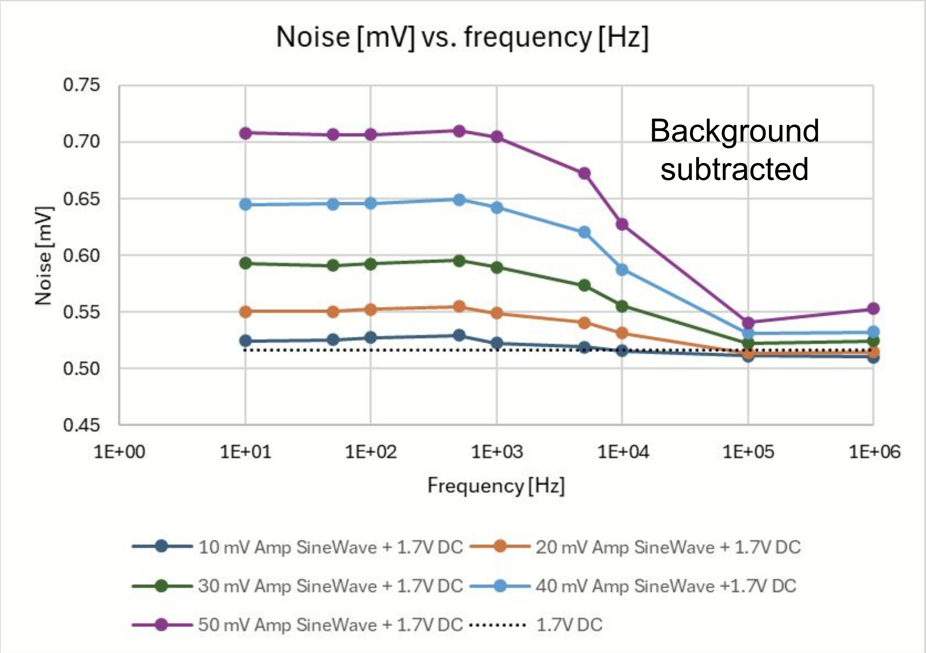
SLDO Pre-Regulator (#2)



- Pre-regulator output noise at fixed DC = 1.7 V inside the RF shielded room and outside
- Noise outside the RF shielded room **(~ 2.2 mV)** is a factor of 5 times larger compared to the inside the RF shielded room **(~ 0.5 mV)**
- Noise values stable across different time division scale starting from 10 ms/ to 1 us/

Noise:

SLDO Pre-Regulator (#2)

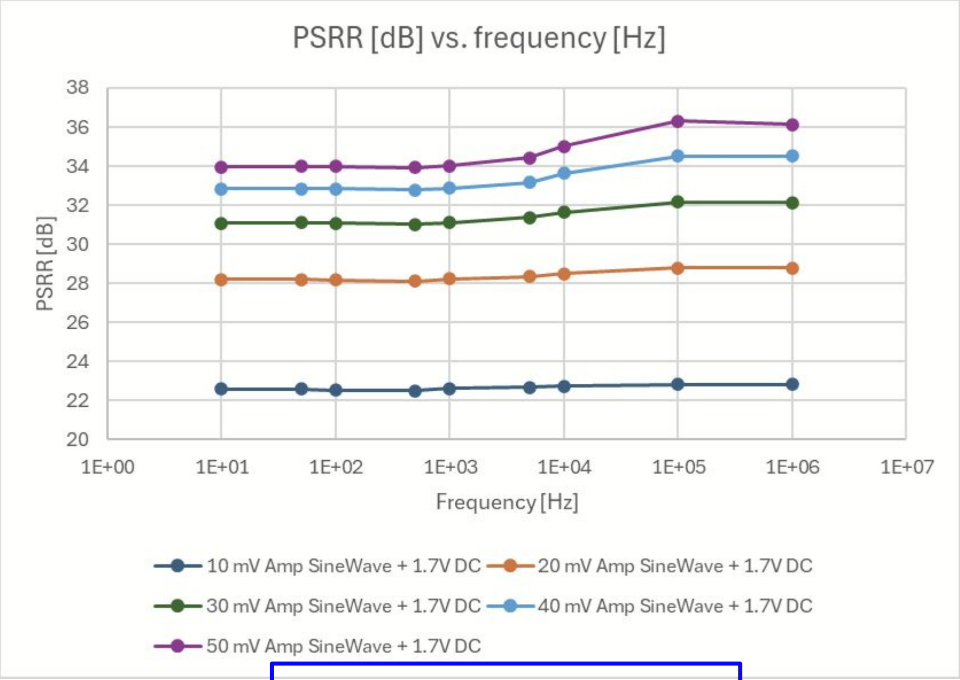


load 2k Ohm || 100pF

- Pre-regulator output noise were studied when additional sinusoidal noise has been injected with the DC offset = 1.7 V
- Sine noise with 10 mV, 20 mV, …, 50 mV amplitude used and swept across frequency range from 10 Hz to 1 MHz
- “Background” noise value has been subtracted in quadrature for all the data points
- Noise value reached maximum ~ 0.7 mV for external 100 mV amplitude sine noise below 1 kHz.

PSRR:

SLDO Pre-Regulator (#2)



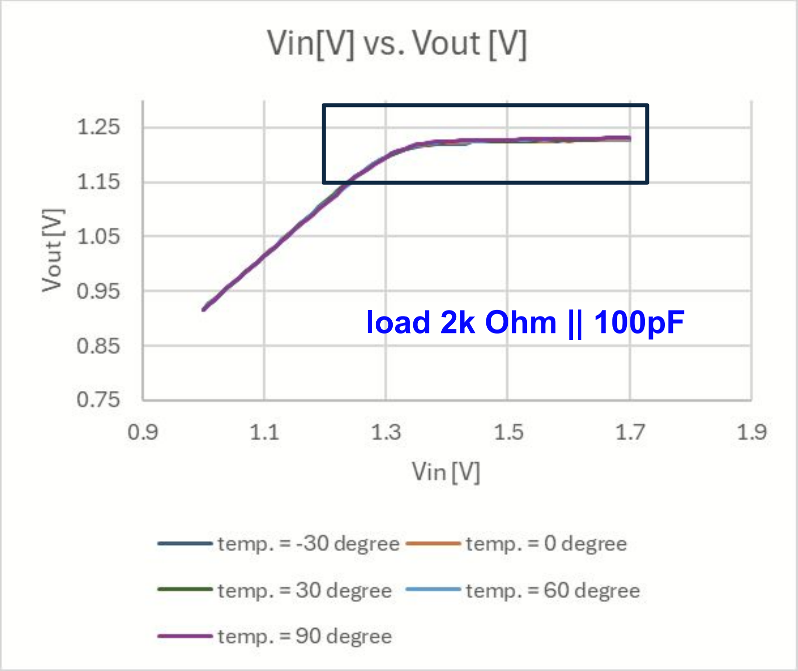
load 2k Ohm || 100pF

- PSRR [dB] = $20\mathrm{Log}_{10}\ (\Delta v_{in}/\Delta v_{out})$, where Δv_{in} is the RMS noise of the input and Δv_{out} is the RMS noise of the output
- PSRR were looked across different frequencies for all different external sinusoidal noise amplitude values
- A minimal dependence of the PSRR with frequency have been observed
- PSRR values depend on the external noise amplitude, reach ~ 22 dB for 10 mV amplitude sine noise and ~ 35 dB for 50 mV amplitude sine noise

SLDO Pre-Regulator (#2)

Ramp-up:
Temperature dependence

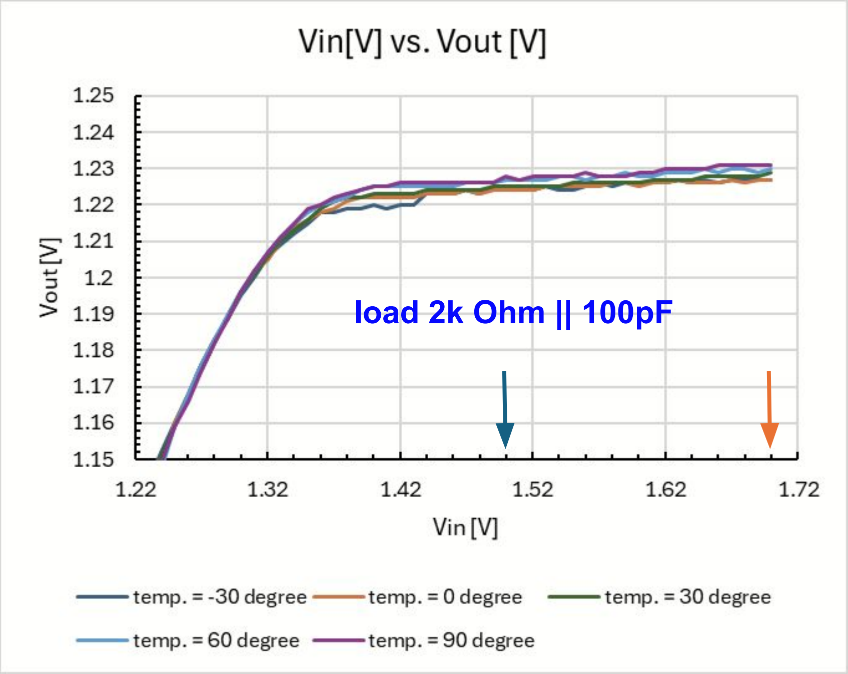
- Environment chamber used for temperature test, ranges of the temperature from -30^{0}C to 90^{0}C
- Start-up ramp test at different temperatures

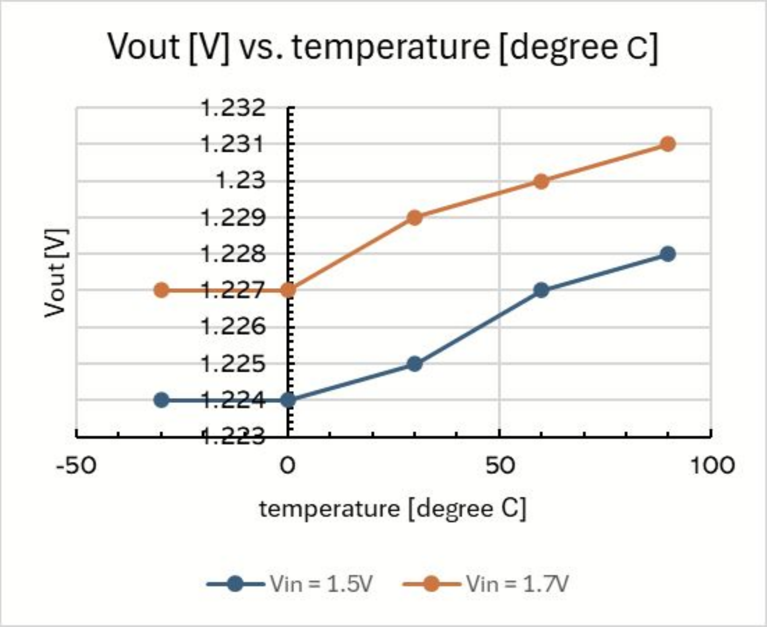


- Fixed DC Vin provided from 1 - 1.7V with 10 mV interval and recorded the Vout
- No visible difference between across different temperature has be observed for Vout ramp-up at this scale

Ramp-up:
Temperature dependence

SLDO Pre-Regulator (#2)



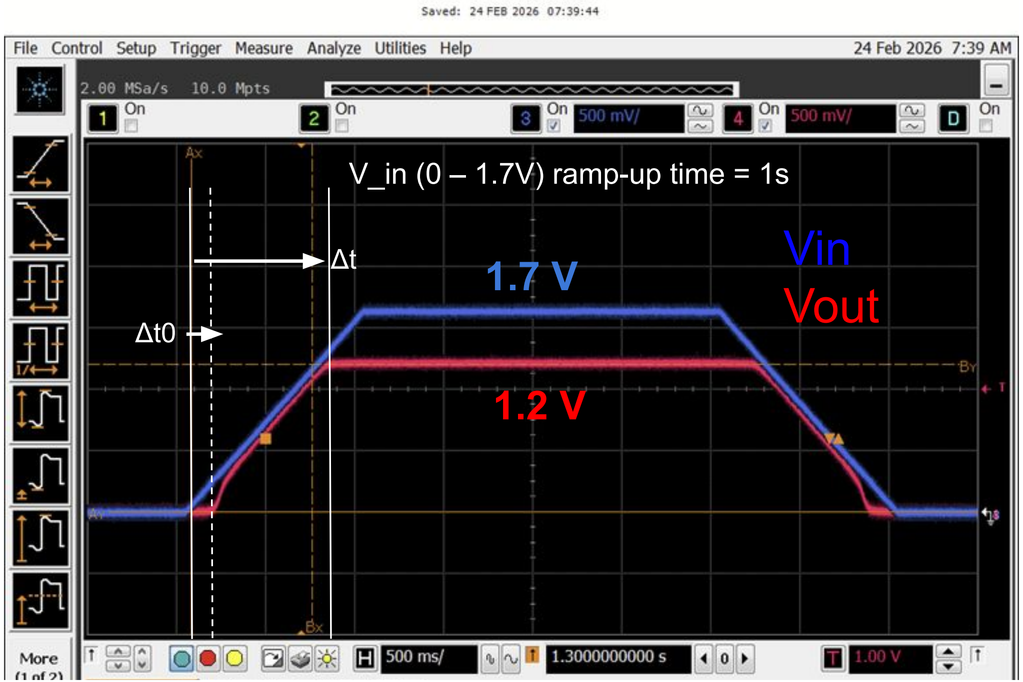


- Vout seems to reach ~ 1.22 - 1.23V for Vin [1.35 - 1.7V]
- ~3-4 mV increment in Vout for change in temperature from -30^{0}C to 90^{0}C

Ramp up:

SLDO Pre-Regulator (#2)

- Used ‘burst’ mode of the oscilloscope to have one ramp-up, i.e., without repeating function
- Repeated the measurements for different ramp-up rates for the V_in from 0 to 1.7 V

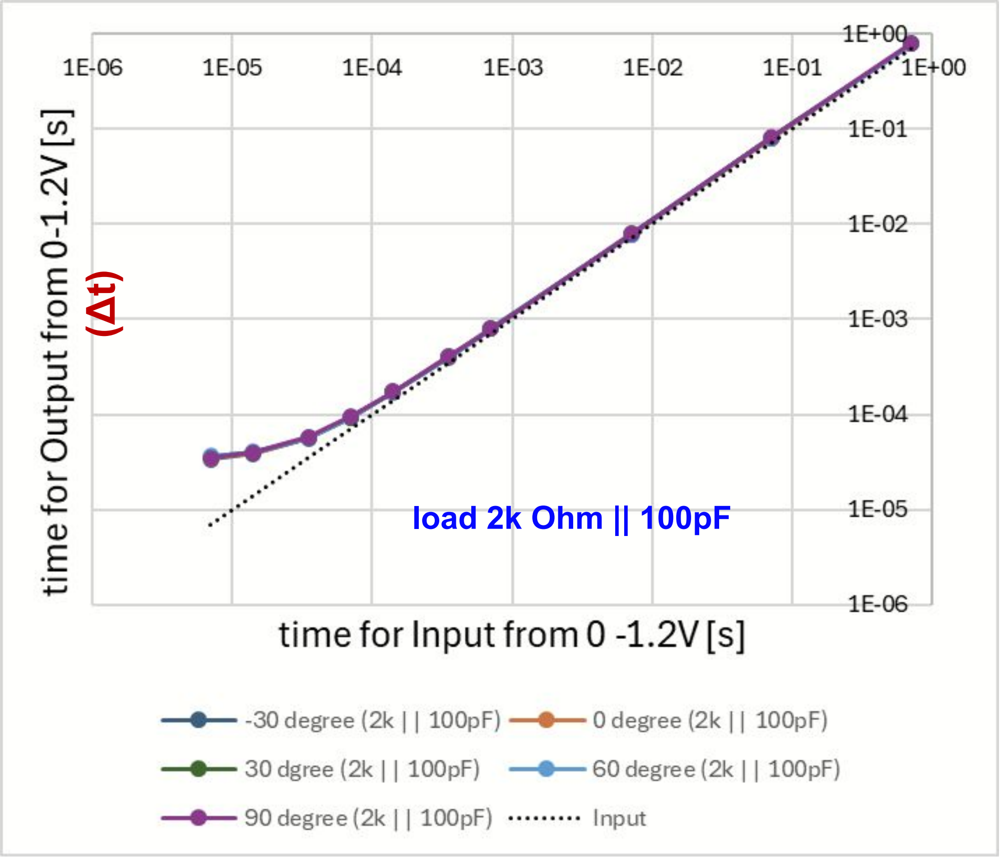


Two time interval has been recorded for each ramp-up rate and temperature

- **Δt = time for Vout to reach 1.2V with respect to Vin turn-on**
- **Δt0 = turn-on time for Vout with respect to Vin turn-on**

SLDO Pre-Regulator (#2)

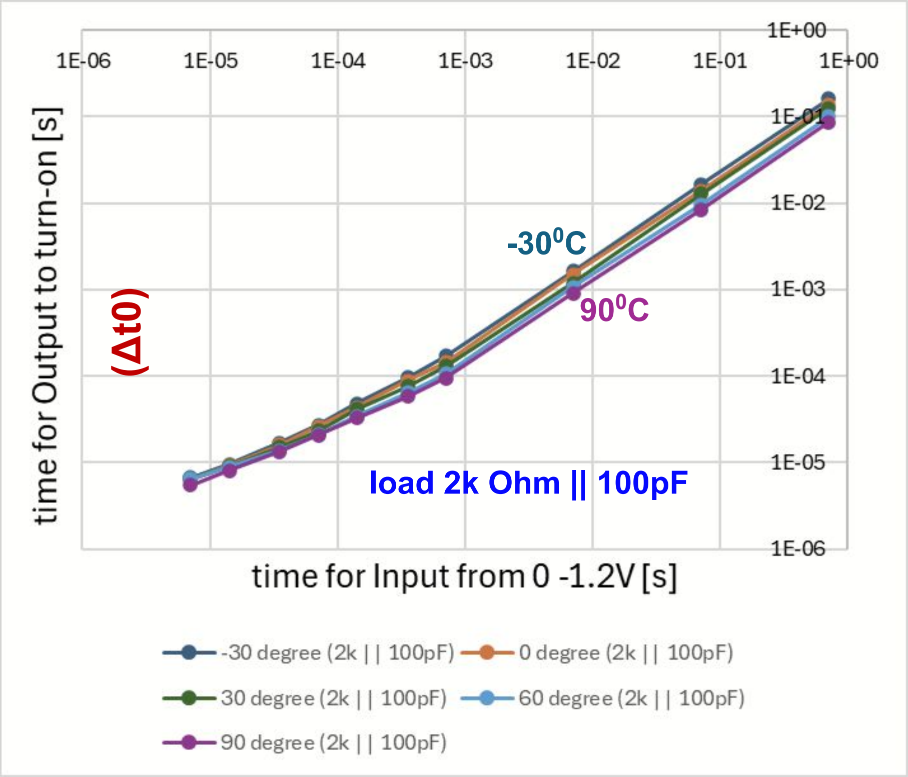
Ramp-up:
Temperature dependence

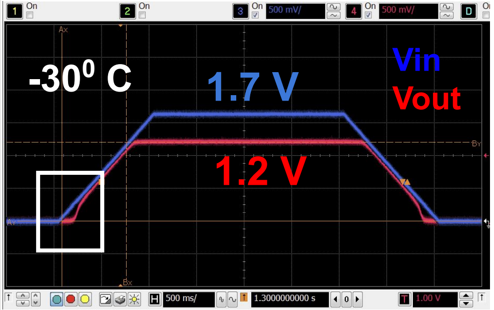


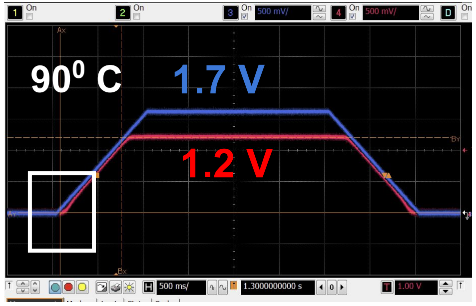
- We studied ramp up time for different temperature
- The difference in the pre-regulator output ramp-up time visible at the faster ramp-up rate (i.e., low ramp-up time) compared to the input ramp-up time
- Pre-regulator output ramp-up time, Δt saturates ~ 50 us
- No visible difference has been observed across different temperatures

Ramp-up:
Temperature dependence

SLDO Pre-Regulator (#2)



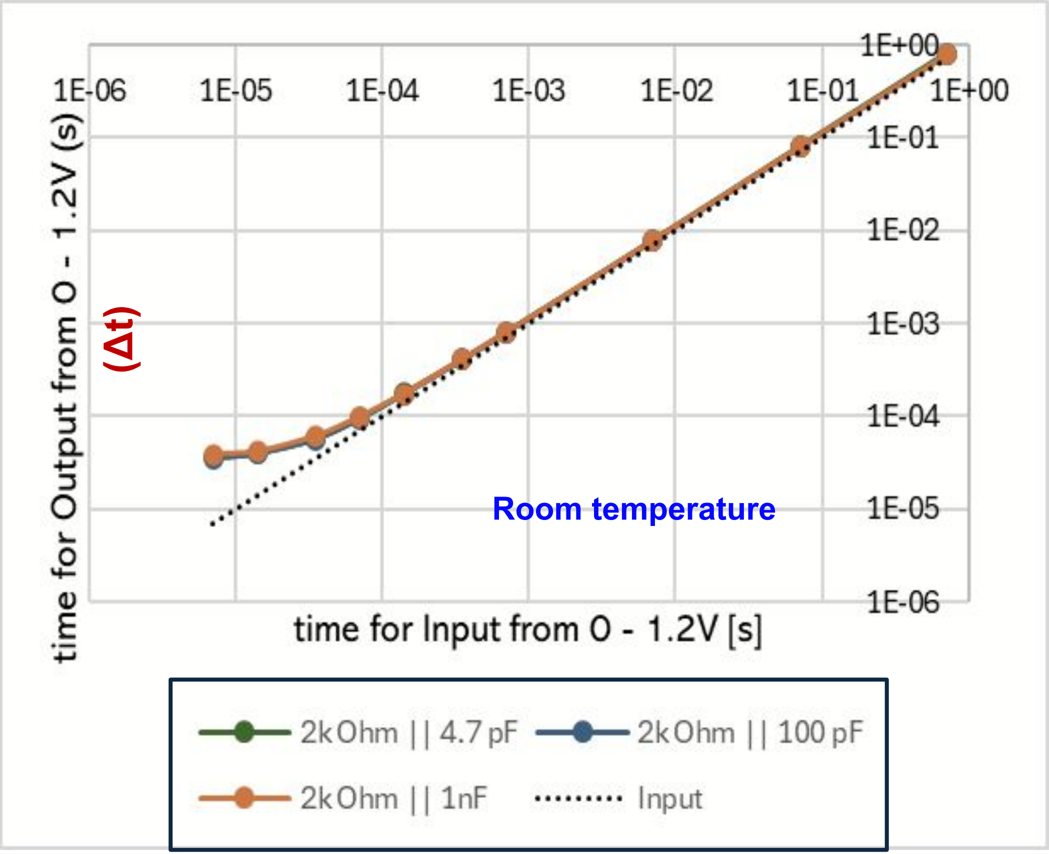




- A larger delay in time (turn-on point) between the output of the pre-regulator with respect to input has been noticed for the lower temperatures.
- Likely be due to threshold voltage changes of the transistors vs. temperature

Ramp up:

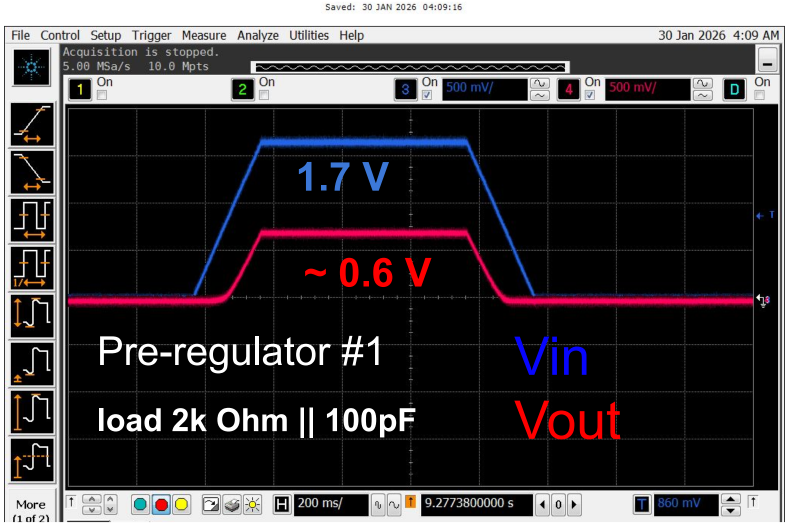
SLDO Pre-Regulator (#2)

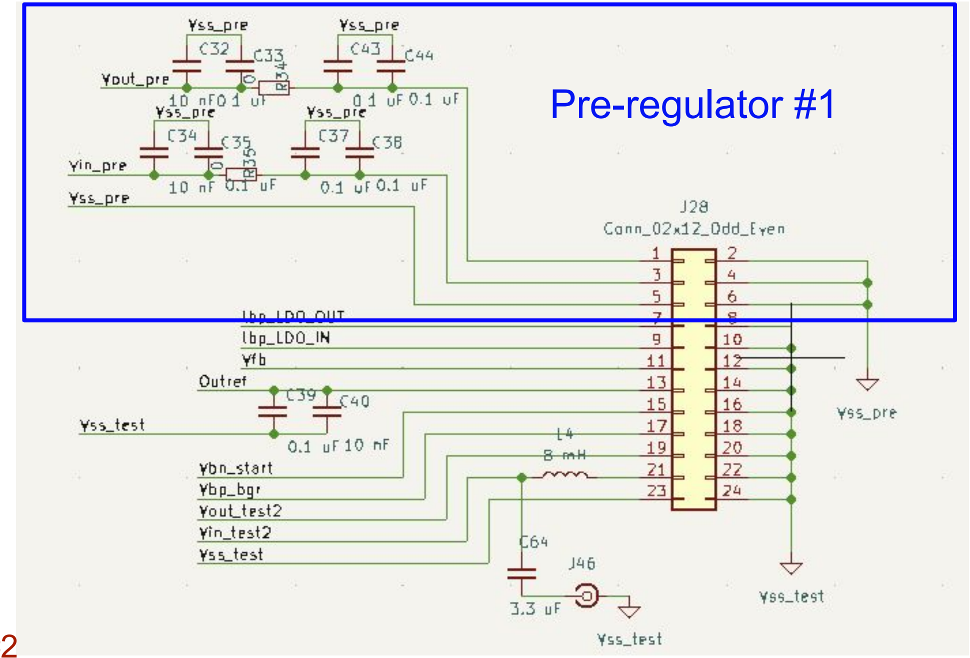


- We studied ramp up time for different capacitive load in parallel with 2k Ohm resistive load for different ramp-up time for Vin
- No visible difference has been observed across different capacitive loads

Ramp-up:
Pre-regulator 1

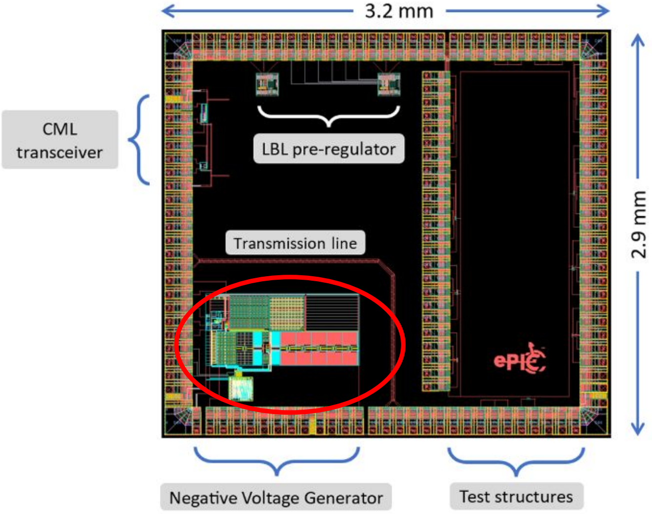
SLDO Pre-Regulator (#1)





- Loading and decoupling same as the pre-regulator #2
- Pre-regulator #1 output not able to reach and stabilize at 1.2V while ramping up (debug ongoing)

Negative Voltage Generator



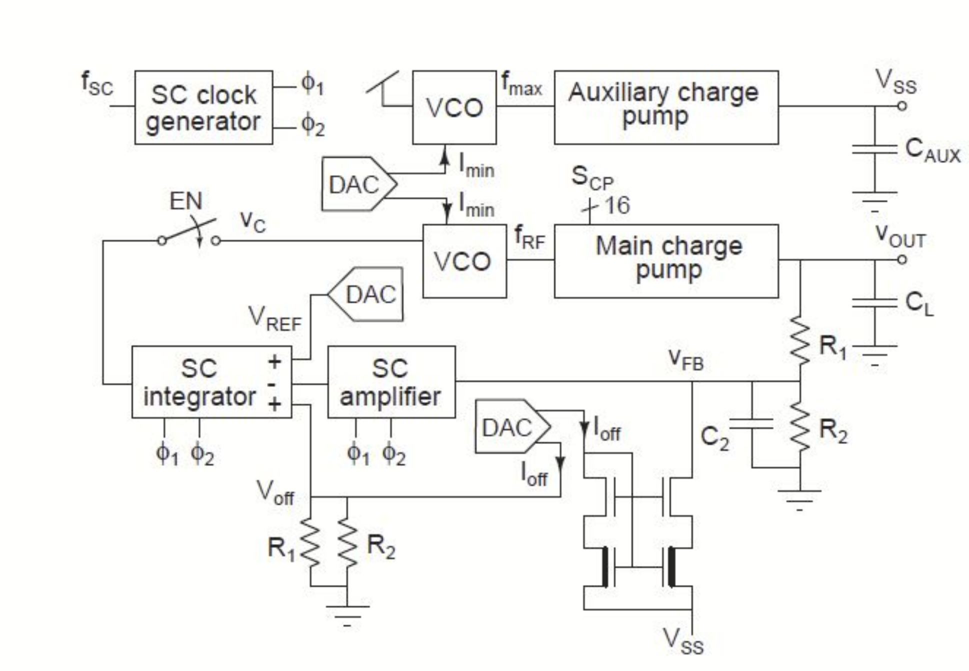
➔ A summary of pre-tests performed till now

Test	Details	Status
Digital control	Verify the I2C programming interface to set register values	✔
NVG output	Verify that NVG output changes w.r.t. register value settings	✔

Instrument:

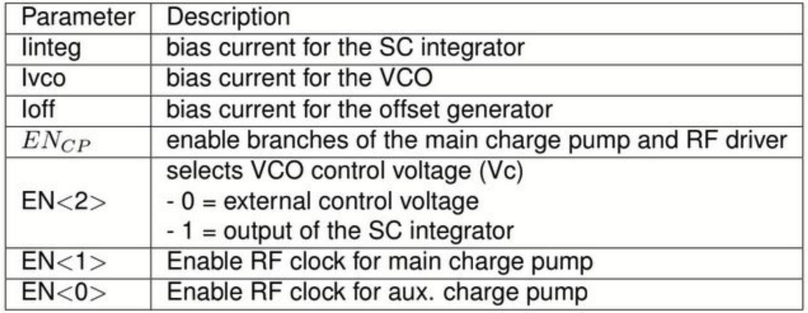
- Power supply for VDD
- Power supply for Vref
- Oscilloscope
- Clock generator for CLK_SC
- Signal generator for power VDD with ripple
- Environmental chamber for temperature test

Negative Voltage Generator



Top-level block diagram of the closed-loop NVG circuit

Programmable control parameters



Parameter	Description
Iinteg	bias current for the SC integrator
Ivco	bias current for the VCO
Ioff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (Vc) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

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Negative Voltage Generator

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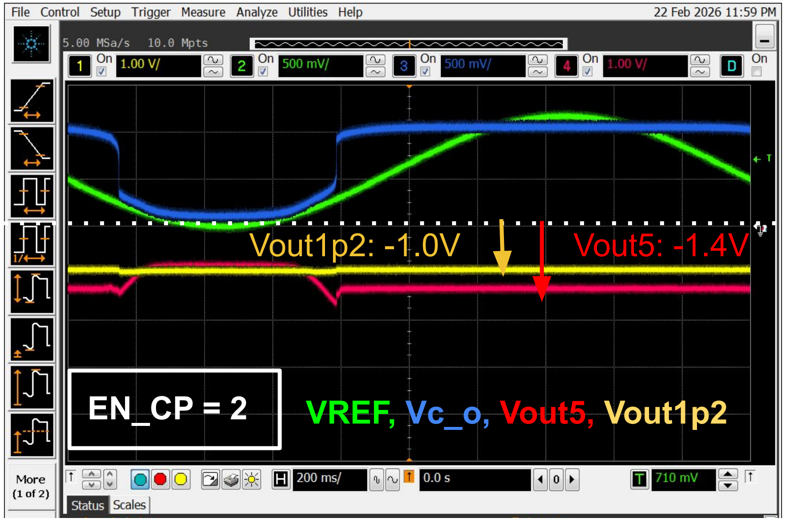

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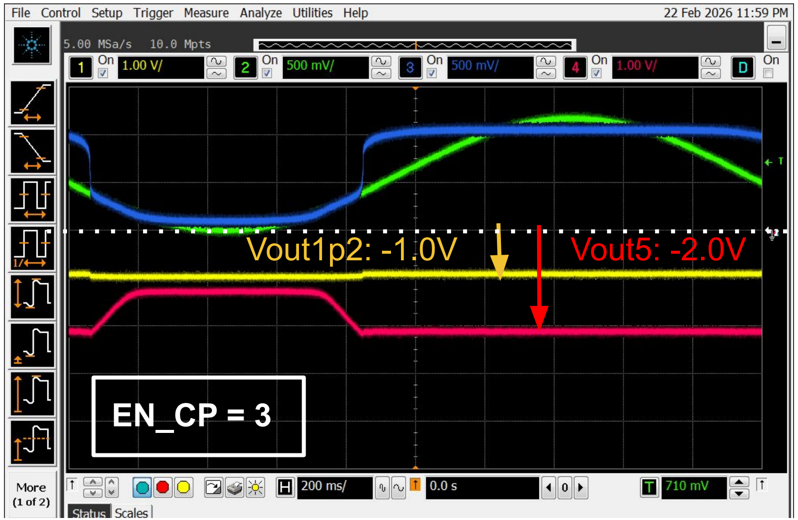


EN<2> = 1 (Internal Vc), EN<1> = 1 (Main CP ON), EN<0> = 1 (Aux. CP ON), I_integ = 10, I_off = 7, I_vco = 0

- Verified the I2C programming interface to set NVG parameters and NVG output responds to the change of register values
- With Aux. CP = ON, the Vout1p2 ~ 1.0V and independent of register values set
- Vout5 value changes with EN_CP values. A limited region of VREF, where the Vout5 drops linearly with VREF, thereafter reach the steady state value

Negative Voltage Generator

A summary of planned tests for verifying the functionality of the NVBG

Test	Swept parameter	Measurement
Output range	V_{REF}, load current (I_L)	Output voltage (Vout), estimate load regulation
Line regulation	Supply voltage (Vdd)	Output voltage (Vout), estimate line regulation
Transient response	V_{REF}, load current (I_L)	Output rise time, settling time, and peak overshoot as a function of V_{REF}
Loop bandwidth	V_{REF}, load current (I_L) for different values of f_{SC}	Verify loop stability by changing value of f_{SC}
Power supply rejection ratio (PSRR)	Ripple in supply voltage	Amplitude of output ripple vs. ripple frequency
Output noise and ripple	V_{REF}, load current (I_L)	Output histogram, peak and rms variability, and frequency spectrum
Temperature effects	Repeat above tests for different temperatures between 25^{0} C and 85^{0} C	

Summary and Outlook

CML Transceiver:

- **Daisy chain with two AncASIC tested**
- **DC coupling is feasible with CML-like inter-chip Tx-Rx link**

SLDO Pre-regulator:

- **Pre-regulator able to provide stable ~ 1.2 V power with noise level ~ 0.5 mV**
- **Minimal dependence of the pre-regulator performance on temperature has been observed**

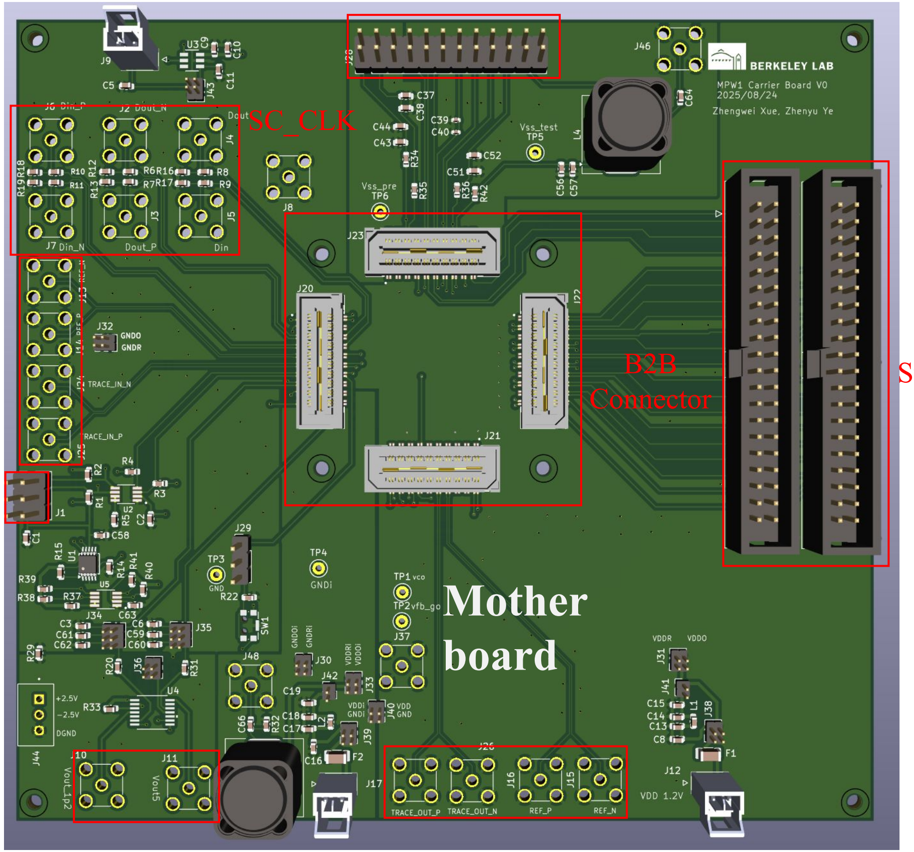
To-do: Study transient response (overshoot and settling time); repeat the tests for the pre-regulator #1

NVBG:

- **Verified the I2C programming interface to set NVG parameters works**
- **NVG output changes w.r.t to register value changes**

To-do: Perform the required tests for verifying the functionality of the NVBG

MWP1 Carrier Board



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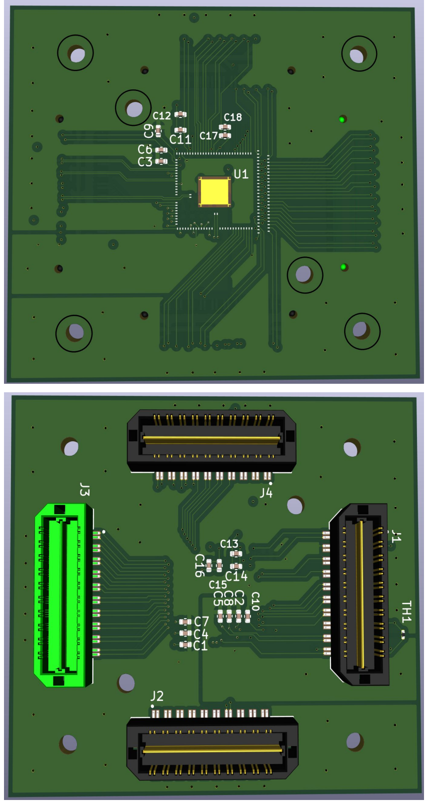
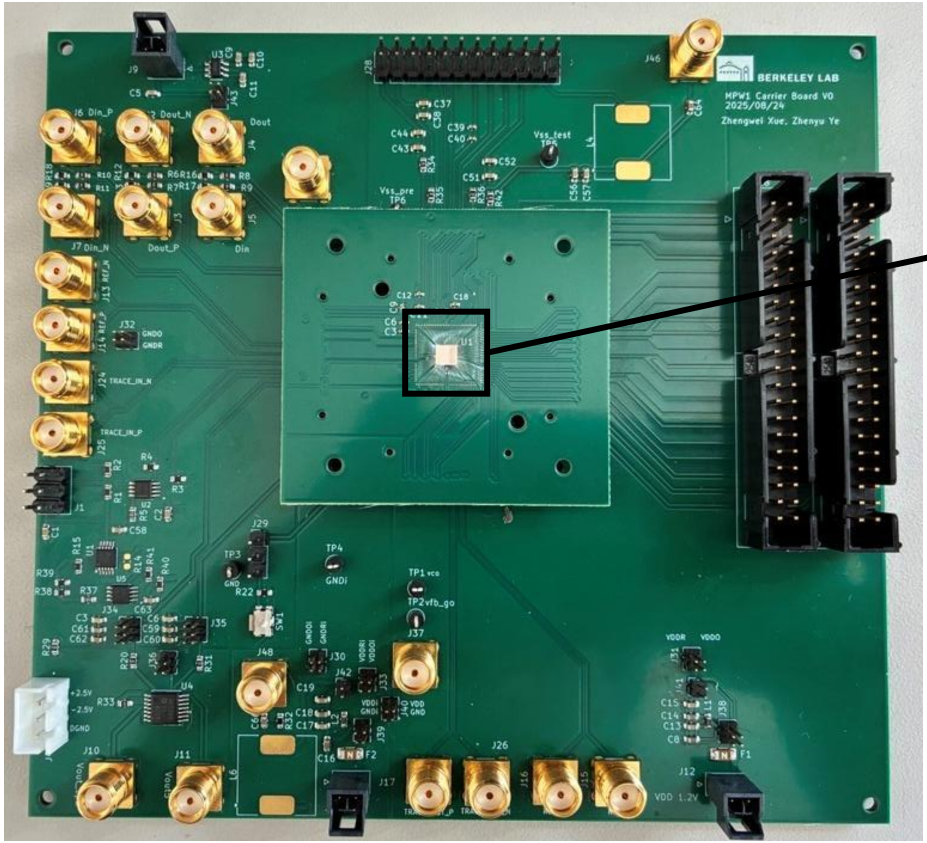
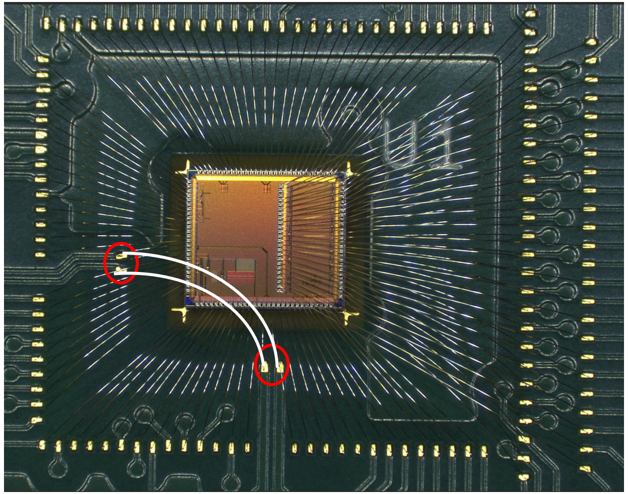


Daughter board

MWP1 Carrier Board

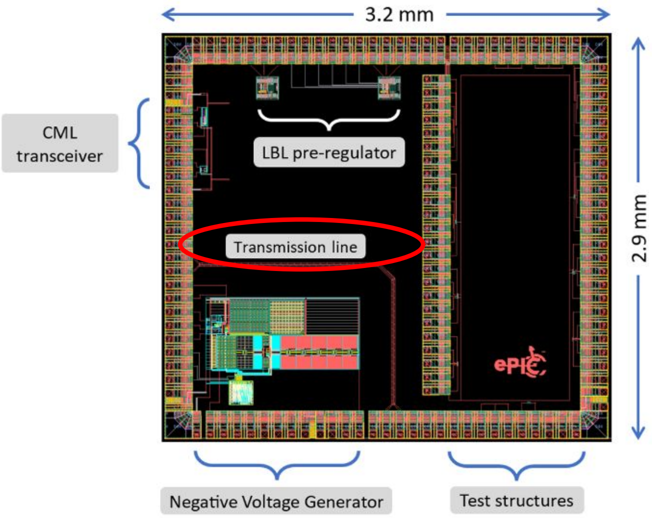




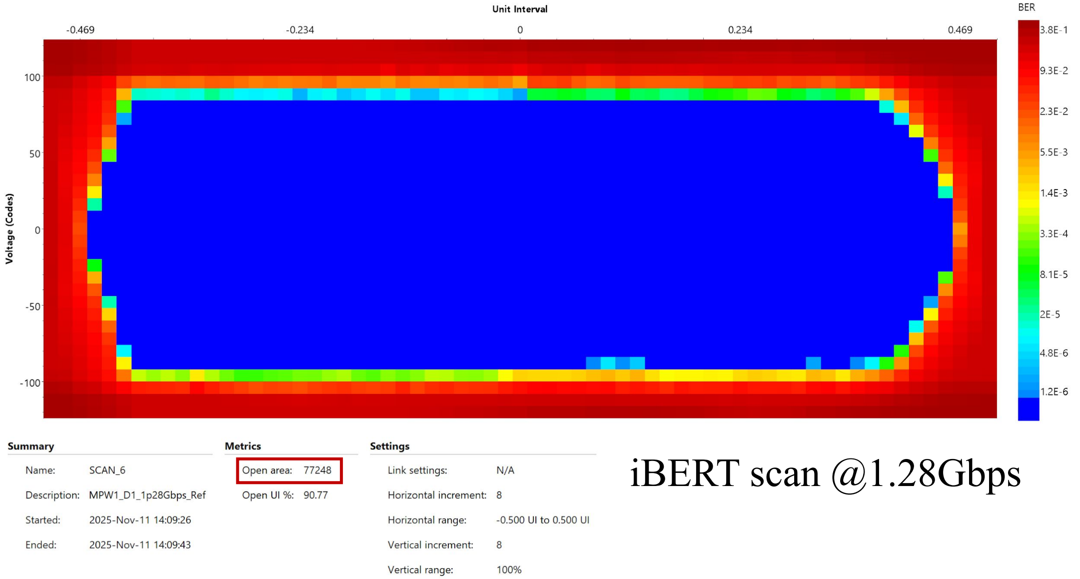
- ☐ MPW1 carrier boards (3 mother and 5 daughter boards) delivered to LBL on Oct 24th

- ☐ Three daughter boards with MPW1 mounted.
- ☐ Two daughter boards with direct wire-bonds (w/o chip)

Transmission line test



- Differential transmission line for testing high-speed data transmission
- A pair of differential trace close to trace of transmission line



Summary

Name: SCAN_6
Description: MPW1_D1_1p28Gbps_Ref
Started: 2025-Nov-11 14:09:26
Ended: 2025-Nov-11 14:09:43

Metrics

Open area: 77248
Open UI %: 90.77

Settings

Link settings: N/A
Horizontal increment: 8
Horizontal range: -0.500 UI to 0.500 UI
Vertical increment: 8
Vertical range: 100%

iBERT scan @1.28Gbps

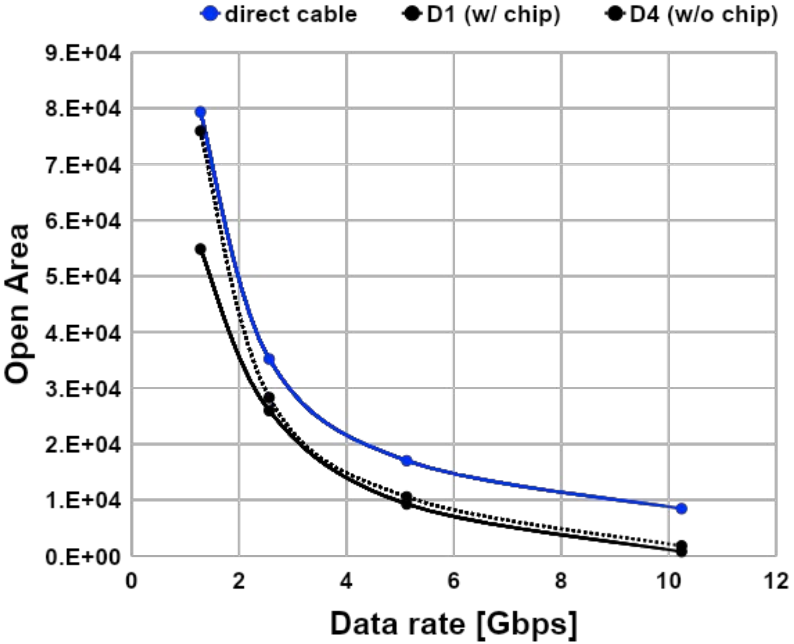
Test Plan:

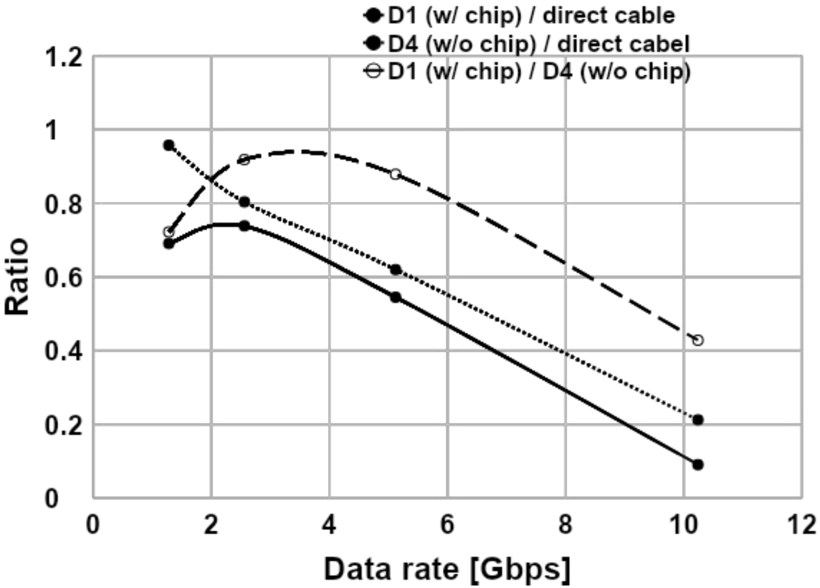
- Eye diagram @different data rates

Instrument:

- FPGA for High-speed data generate and eye diagram

Transmission line test

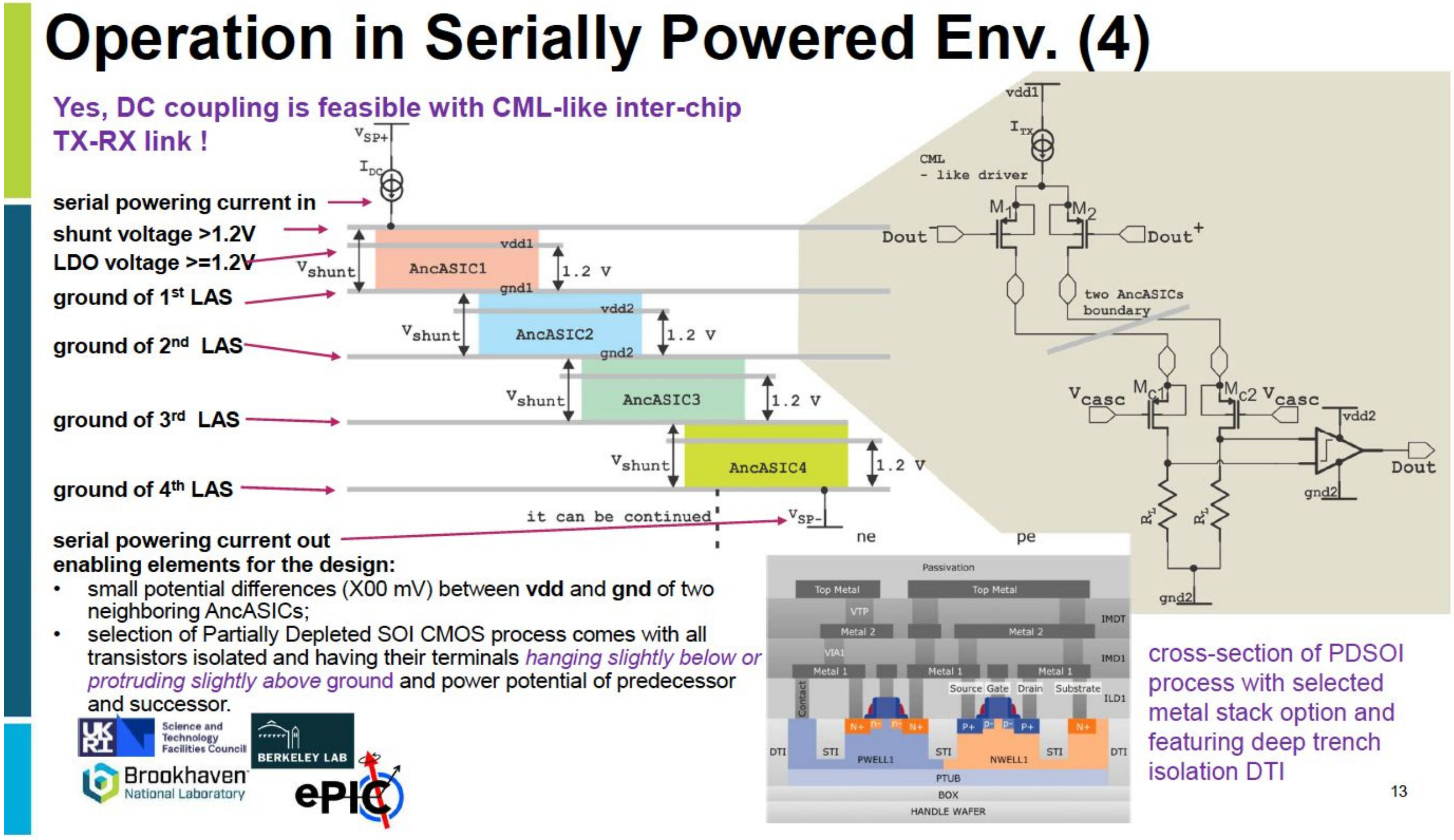




- ❑ Open area or ratio sharply decrease with increasing the data rates, similar behavior across all chips tested
- ❑ Signal quality of the on-chip transmission line path may be suboptimal/compromised @ high data rates

CML Transceiver

slide from Grzegorz



Operation in Serially Powered Env. (4)

Yes, DC coupling is feasible with CML-like inter-chip TX-RX link !

serial powering current in

shunt voltage >1.2V

LDO voltage >=1.2V

ground of 1st LAS

ground of 2nd LAS

ground of 3rd LAS

ground of 4th LAS

serial powering current out

enabling elements for the design:

- small potential differences (X00 mV) between **vdd** and **gnd** of two neighboring AncASICs;
- selection of Partially Depleted SOI CMOS process comes with all transistors isolated and having their terminals *hanging slightly below or protruding slightly above ground* and power potential of predecessor and successor.

cross-section of PDSOI process with selected metal stack option and featuring deep trench isolation DTI

CML Transmitter Test

Transmitter:

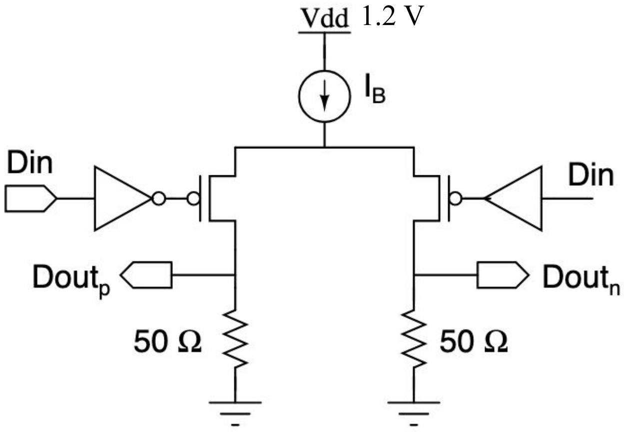
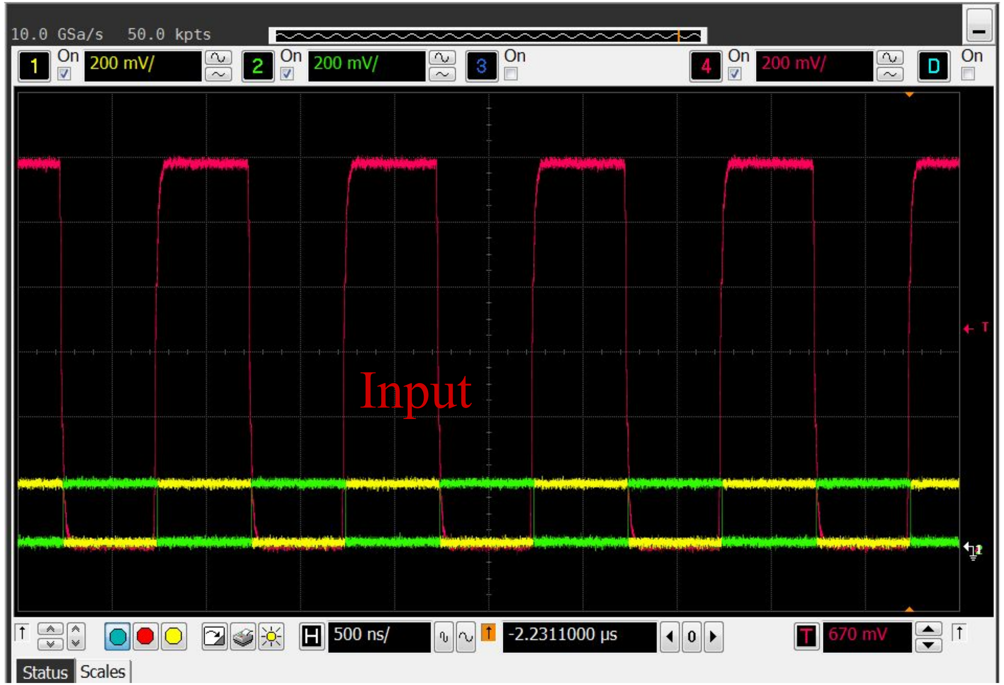


Figure 13: CML transmitter.



Expected differential output from simulation ~ 0.2V Vpp

- Single-end input from signal generator: high-Z, 1MHz square, rail-to-rail 0-1.2V
- Differential output measured on oscilloscope: 50 Ohms, common mode ~ 0.1V, amplitude **0.2V Vpp**

CML Receiver Test

Receiver:

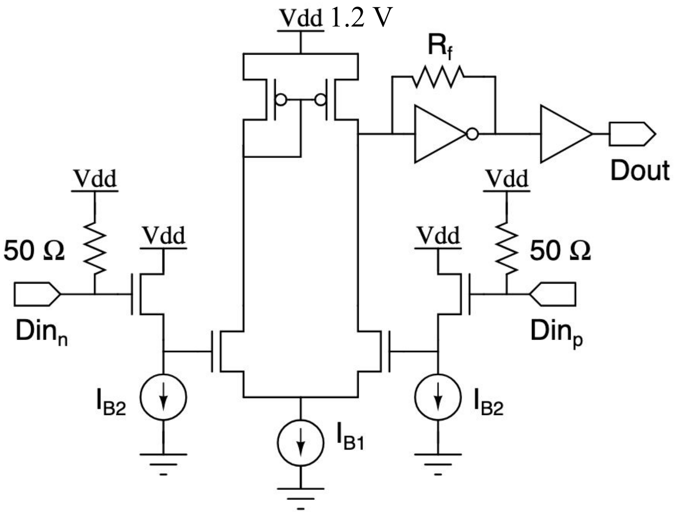
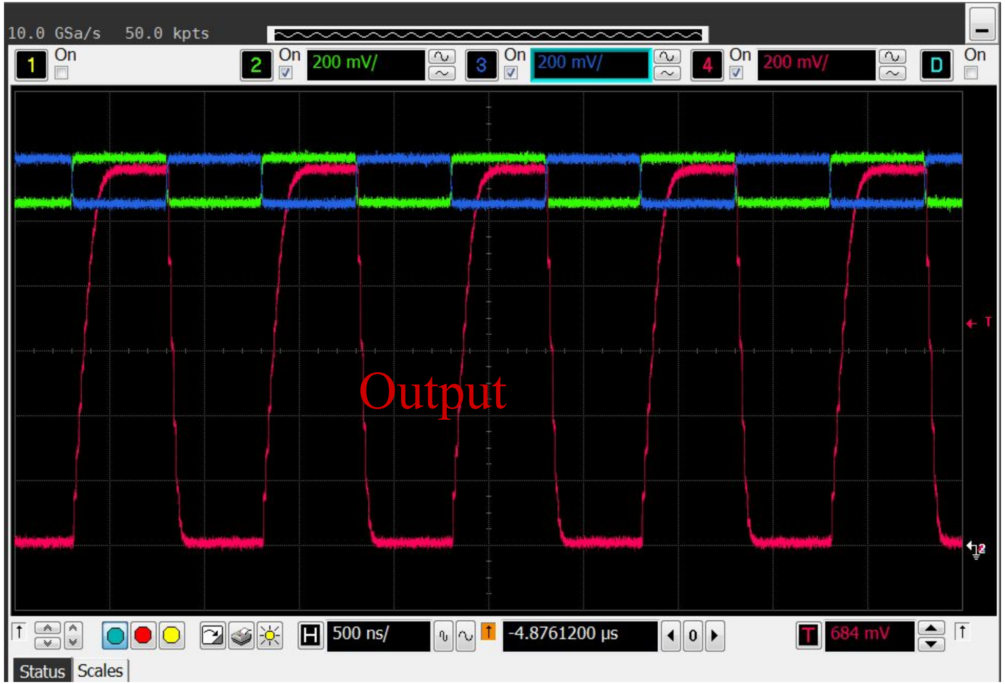


Figure 14: CML receiver.

Expected single-ended output from simulation ~ 1.2V


10.0 GSa/s 50.0 kpts

1 On ☐

2 On ☑ 200 mV/

3 On ☑ 200 mV/

4 On ☑ 200 mV/

D On ☐

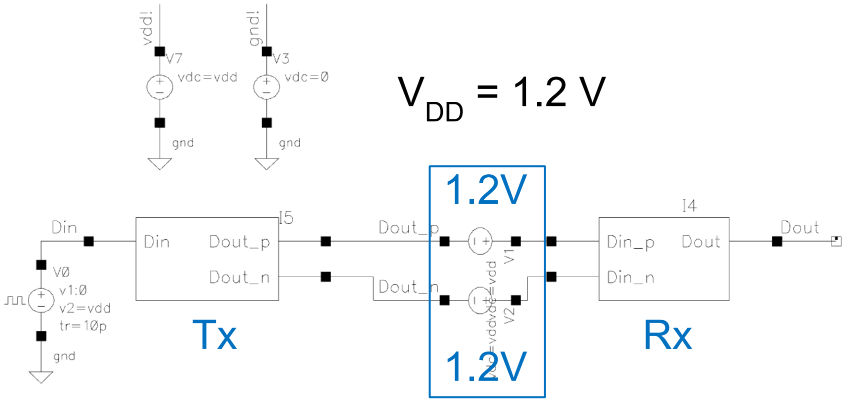
H 500 ns/

-4.8761200 µs

T 684 mV

- Differential input from signal generator: 50 Ohms, 1MHz square, common mode 1.1V, amplitude 0.2V Vpp
- Single-end output measured on oscilloscope setting: 1M Ohms, **0-1.2V rail-to-rail**

CML Transceiver



V_{DD} = 1.2 V

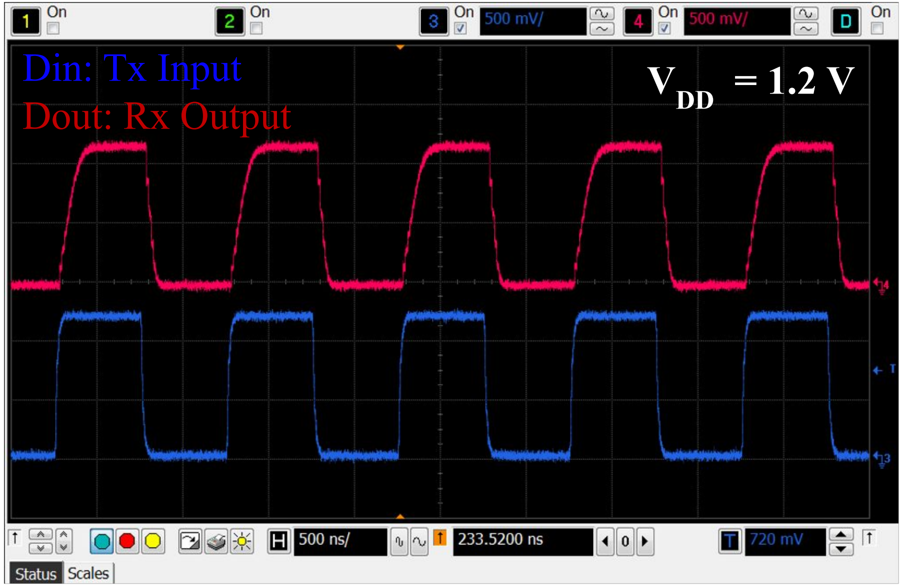
1.2V

1.2V

Tx

Rx

external power



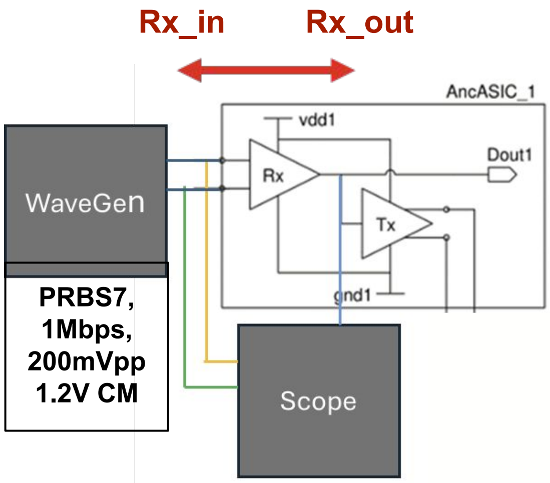
Din: Tx Input

Dout: Rx Output

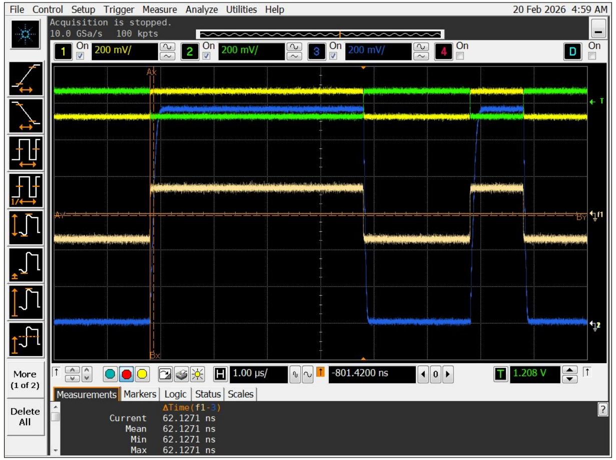
V_{DD} = 1.2 V

- Single ended Tx input: rail-to-rail 0-1.2V
- Single ended Rx output: rail-to-rail 0-1.2V at V_{DD} = 1.2 V
- Matched expected value from the simulation

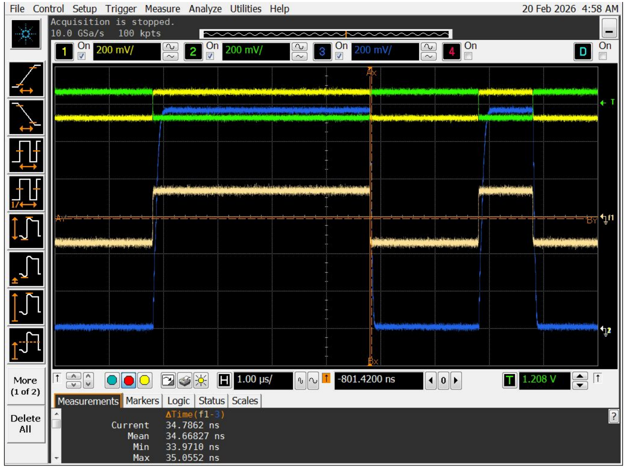
CML Transceiver (single chip)



Saved: 20 FEB 2026 04:59:23



```
Acquisition is stopped.
10.0 GSa/s   100 kpts
1 On 200 mV/   2 On 200 mV/   3 On 200 mV/   4 On   D On
H 1.00 µs/   -801.4200 ns   0   T 1.208 V
           ΔTime(f1-3)
  Current  62.1271 ns
     Mean  62.1271 ns
      Min  62.1271 ns
      Max  62.1271 ns
```



```
Acquisition is stopped.
10.0 GSa/s   100 kpts
1 On 200 mV/   2 On 200 mV/   3 On 200 mV/   4 On   D On
H 1.00 µs/   -801.4200 ns   0   T 1.208 V
           ΔTime(f1-3)
  Current  34.7862 ns
     Mean  34.66827 ns
      Min  33.9710 ns
      Max  35.0552 ns
```

f1 = ch1 - ch2 = diff Rx Input

Ch3 = Rx Output

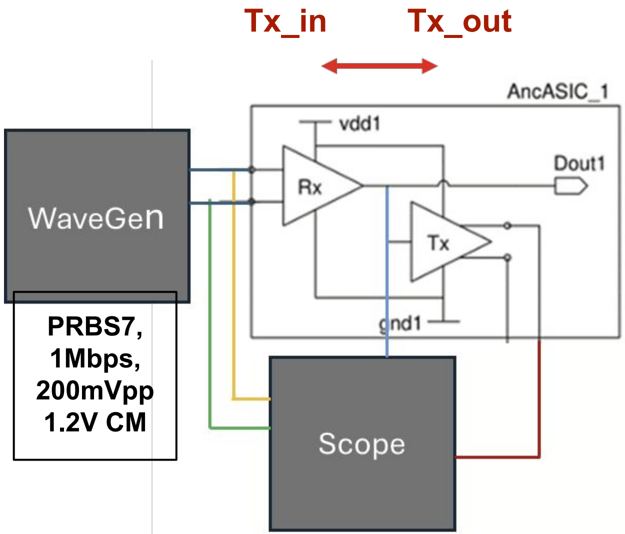
rise Δtime(f1-ch3) ~ 62 ns

fall Δtime(f1-ch3) ~ 34 ns

- 50% threshold used in extracting Δtime
- One 4 ft cable contribute ~ 5 ns delay

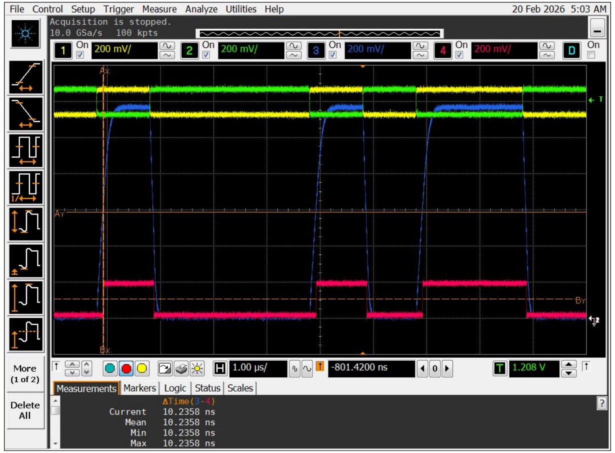
➔ Delay between Rx Input and Rx Output
  - **~ 57 ns (rising edge)**
  - **~ 29 ns (falling edge)**

CML Transceiver (single chip)



PRBS7,
1Mbps,
200mVpp
1.2V CM

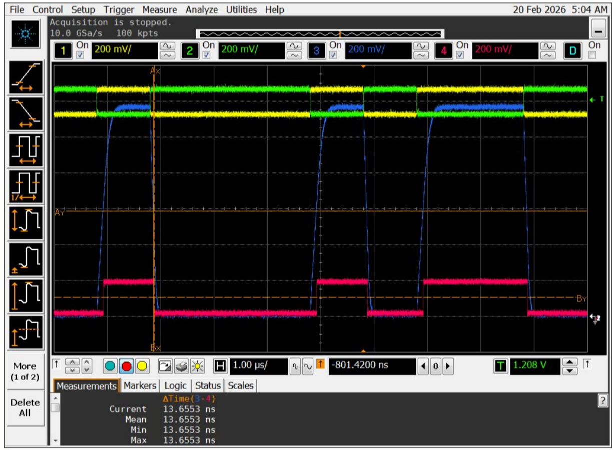
Saved: 20 FEB 2026 05:03:30



```
Acquisition is stopped.
10.0 GSa/s   100 kpts
```

```
         ΔTime(3-4)
Current  10.2358 ns
   Mean  10.2358 ns
    Min  10.2358 ns
    Max  10.2358 ns
```

Saved: 20 FEB 2026 05:04:06



```
Acquisition is stopped.
10.0 GSa/s   100 kpts
```

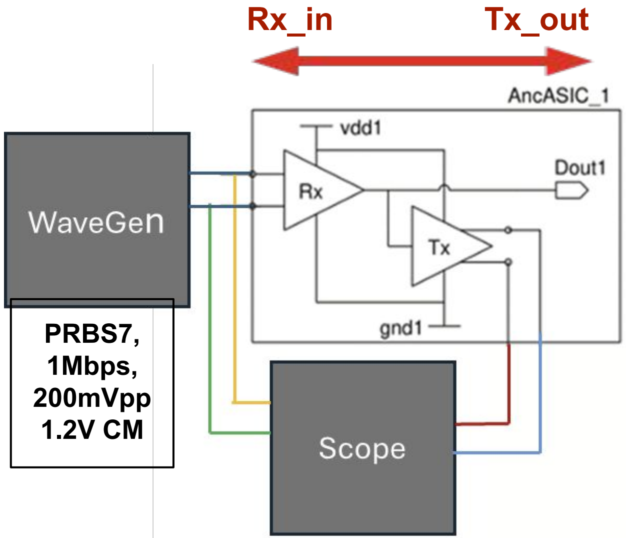
```
         ΔTime(3-4)
Current  13.6553 ns
   Mean  13.6553 ns
    Min  13.6553 ns
    Max  13.6553 ns
```

Ch3 = Tx Input
Ch4 = Tx Output
rise Δtime(ch3-ch4) ~ 10 ns
fall Δtime(ch3-ch4) ~ 13 ns

- 50% threshold used in extracting Δtime
- One 4 ft cable contribute ~ 5 ns delay

➔ Delay between Tx Input and Tx Output
  - **~ 5 ns (rising edge)**
  - **~ 8 ns (falling edge)**

CML Transceiver (single chip)

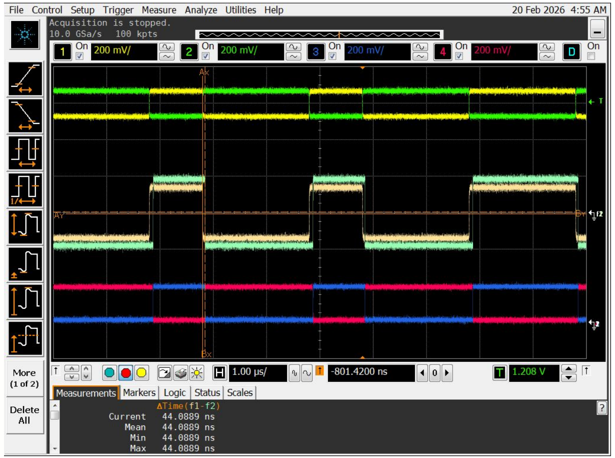


Saved: 20 FEB 2026 04:55:19

```
Acquisition is stopped.
10.0 GSa/s   100 kpts
```

```
          ΔTime(f1-f2)
Current   71.4379 ns
   Mean   71.4379 ns
    Min   71.4379 ns
    Max   71.4379 ns
```

Saved: 20 FEB 2026 04:55:53



```
Acquisition is stopped.
10.0 GSa/s   100 kpts
```

```
          ΔTime(f1-f2)
Current   44.0889 ns
   Mean   44.0889 ns
    Min   44.0889 ns
    Max   44.0889 ns
```

f1 = ch1 - ch2 = diff Rx Input

f2 = ch3 - ch4 = diff Tx output

rise Δtime(f1-f2) ~ 71 ns

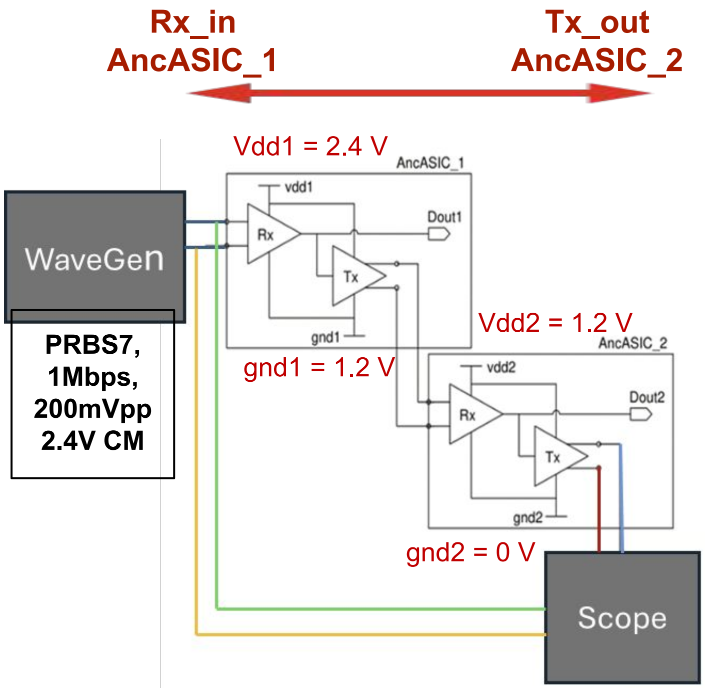
fall Δtime(f1-f2) ~ 44 ns

- 50% threshold used in extracting Δtime
- Two 4 ft cable contribute ~ 10 ns delay

➔ Delay between Rx Input and Tx Output

- **~ 61 ns (rising edge)**
- **~ 34 ns (falling edge)**

CML Transceiver (daisy chain)



Rx_in
AncASIC_1

Tx_out
AncASIC_2

Vdd1 = 2.4 V

gnd1 = 1.2 V

Vdd2 = 1.2 V

gnd2 = 0 V

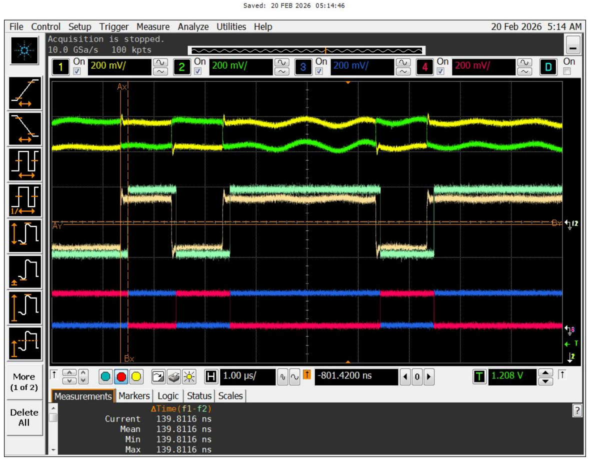
PRBS7,
1Mbps,
200mVpp
2.4V CM

f1 = ch1 - ch2 = diff Rx Input of AncASIC_1

f2 = ch3 - ch4 = diff Tx output of AnCASIC_2

rise Δtime(f1-f2) ~ 139 ns

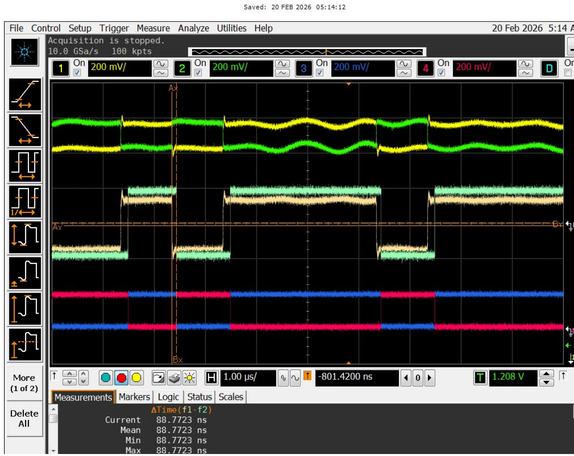
fall Δtime(f1-f2) ~ 88 ns



Saved: 20 FEB 2026 05:14:46

Acquisition is stopped.
10.0 GSa/s 100 kpts

```
        ΔTime(f1-f2)
Current   139.8116 ns
   Mean   139.8116 ns
    Min   139.8116 ns
    Max   139.8116 ns
```



Saved: 20 FEB 2026 05:14:12

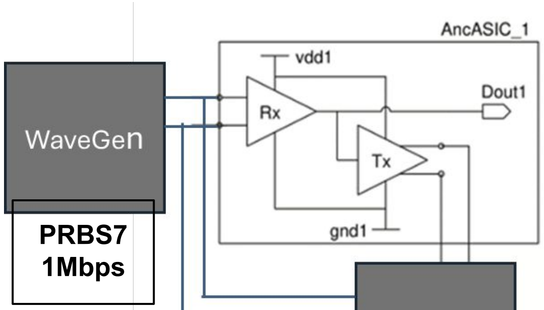
Acquisition is stopped.
10.0 GSa/s 100 kpts

```
        ΔTime(f1-f2)
Current   88.7723 ns
   Mean   88.7723 ns
    Min   88.7723 ns
    Max   88.7723 ns
```

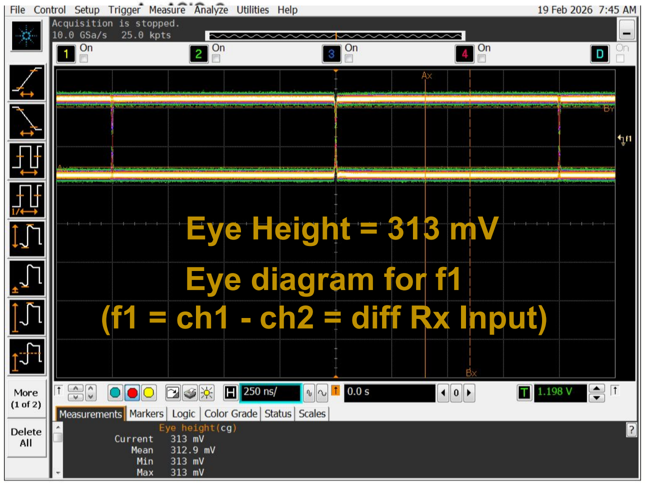
- 50% threshold used in extracting Δtime
- Four 4 ft cable contribute ~ 20 ns delay

➔ Delay between Rx Input and Tx Output
  - **~ 119 ns (rising edge)**
  - **~ 68 ns (falling edge)**

CML Transceiver (single chip)



PRBS7
1Mbps

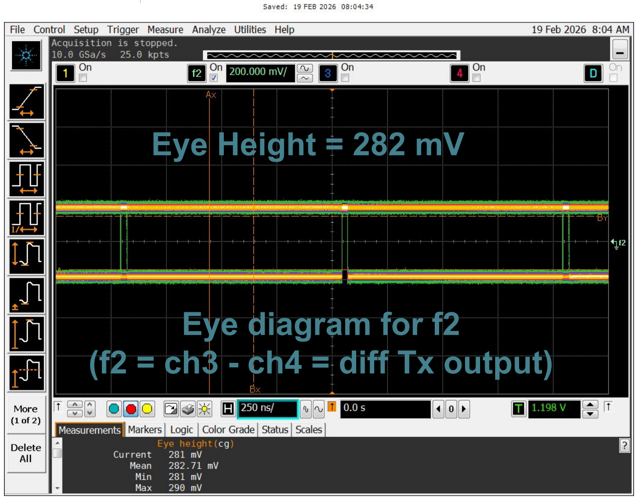


```
Acquisition is stopped.
10.0 GSa/s   25.0 kpts
```

Eye Height = 313 mV

Eye diagram for f1
(f1 = ch1 - ch2 = diff Rx Input)

```
        Eye height(cg)
Current  313 mV
   Mean  312.9 mV
    Min  313 mV
    Max  313 mV
```



```
Acquisition is stopped.
10.0 GSa/s   25.0 kpts
```

Eye Height = 282 mV

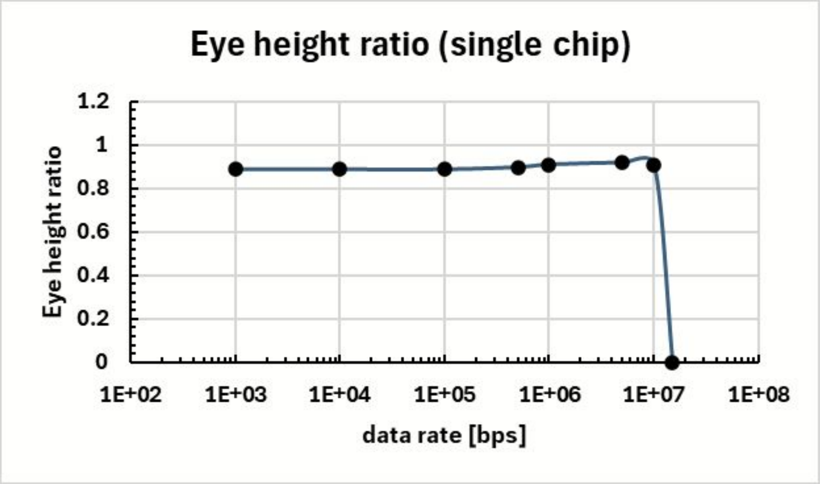
Eye diagram for f2
(f2 = ch3 - ch4 = diff Tx output)

```
        Eye height(cg)
Current  281 mV
   Mean  282.71 mV
    Min  281 mV
    Max  290 mV
```

Eye Height ratio = (Eye Height of diff Tx Output) / (Eye Height of diff Rx Input) = 0.9

- Performed the data-rate scan from 10 kbps - 20 Mbps, recorded delay and eye height ratio

CML Transceiver
(single chip)



PRBS7 at 10 Mbps

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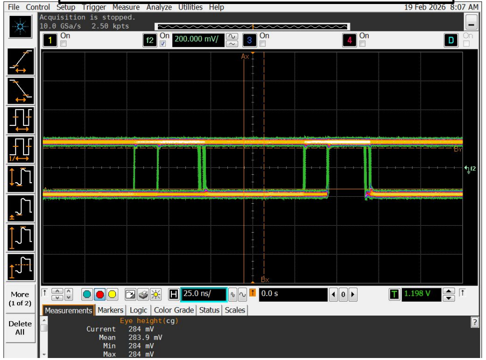
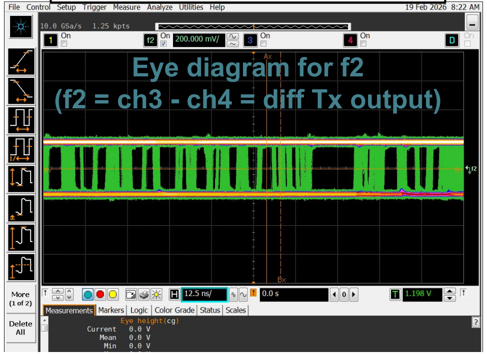


```
Acquisition is stopped.
10.0 GSa/s   2.50 kpts
```

```
          Eye height(cg)
Current   284 mV
   Mean   283.9 mV
    Min   284 mV
    Max   284 mV
```

PRBS7 at 15 Mbps

Saved: 19 FEB 2026 08:22:36

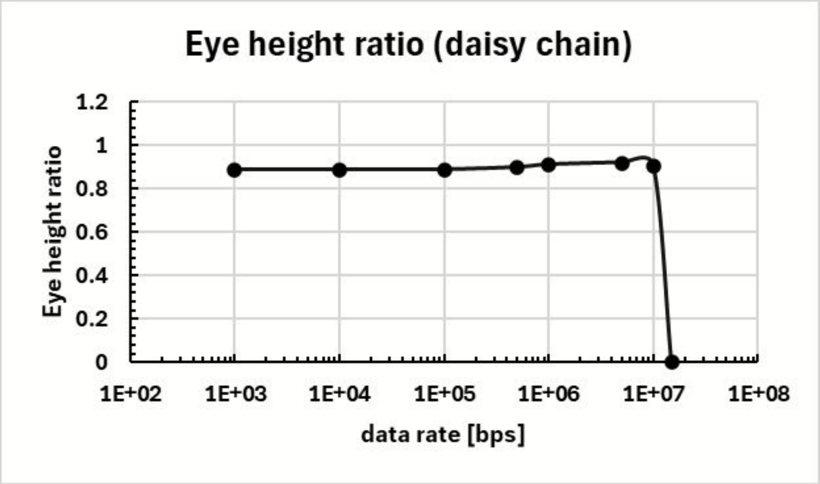


```
10.0 GSa/s   1.25 kpts
```

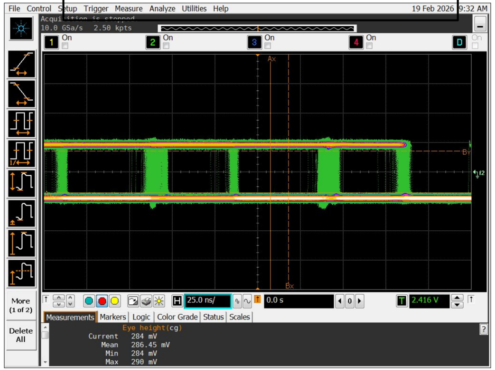
```
          Eye height(cg)
Current   0.0 V
   Mean   0.0 V
    Min   0.0 V
```

- Eye height of the Tx output for a single chip uniform until 10 MBps
- > 10 Mbps, scope not able to found an eye; the eye height for diff Tx output shows 0 mV

CML Transceiver (daisy chain)

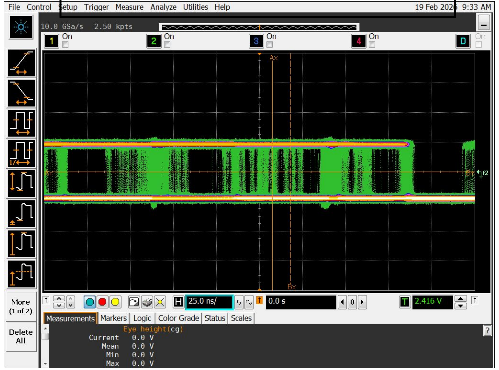


PRBS7 at 10 Mbps



```
Eye height(cg)
  Current   284 mV
     Mean   286.45 mV
      Min   284 mV
      Max   290 mV
```

PRBS7 at 15 Mbps



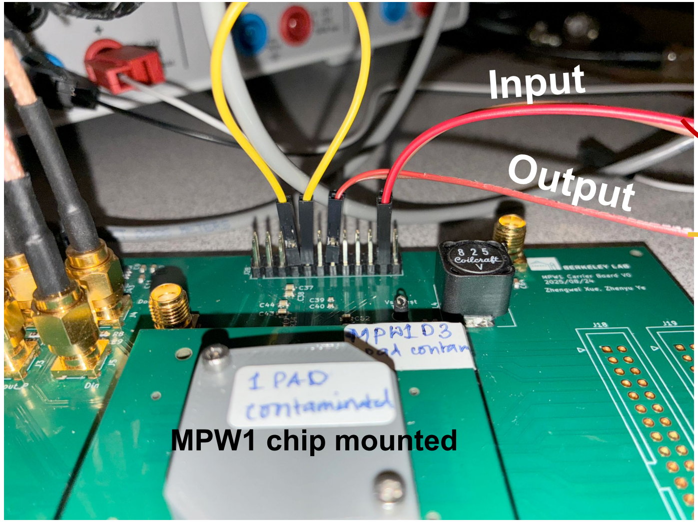
```
Eye height(cg)
  Current   0.0 V
     Mean   0.0 V
      Min   0.0 V
      Max   0.0 V
```

- > 10 Mbps, scope not able to found an eye, therefore the eye height for diff Tx output of AncASIC_2 shows 0 mV
- Uniform eye height height ratio (~ 0.9) for the daisy chain until 10 Mbps goes to 0 for data rate > 10 Mbps

SLDO Pre-Regulator

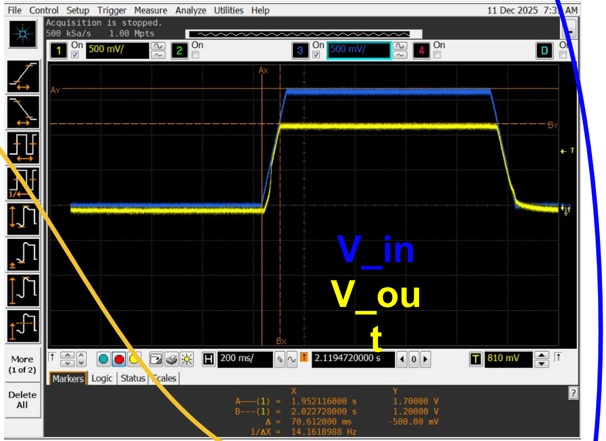
Setup description:

- A DC power supply, wave generator, oscilloscope has been used for the measurements



Wave Generator

Oscilloscope



```
Acquisition is stopped.
500 kSa/s    1.00 Mpts
```

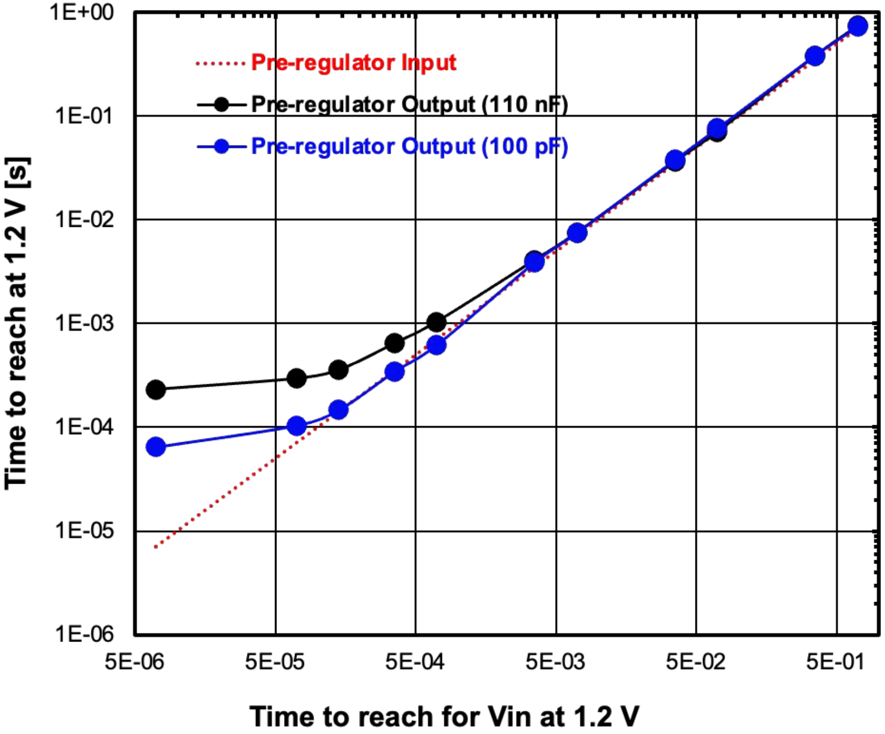
```
                 X                  Y
A——(1) =   1.952116000 s      1.70000 V
B---(1) =  2.022728000 s      1.20000 V
      Δ =  70.612000 ms     -500.00 mV
   1/ΔX =  14.1618988 Hz
```

- Output waveform of the pre-regulator recorded on the scope
- T-connector used to send the input waveform to the pre-regulator and record it at the oscilloscope
- When using the RF-shielded enclosure, only the test board was placed inside the enclosure, and operated from outside of the enclosure

Ramp up:

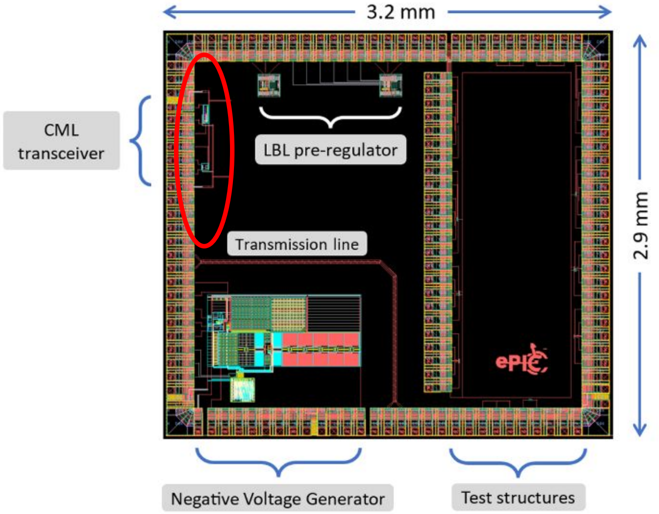
SLDO Pre-Regulator

- Extracted Δt_out (Δt_in) for pre-regulator V_out (V_in) when both ramp-up from 0 to 1.2 V
- Repeated the measurements for all ramp-up times for the V_in from 0 to 1.7 V



- We studied ramp up time for two different loads (110 nF and 100 pF) on Vout
- The difference in the pre-regulator output ramp-up time visible at the faster ramp-up rate (i.e., low ramp-up time) for two different loads of Vout
- Pre-regulator output ramp-up time, Δt_out saturates ~ 200 – 300 us for 110 nF and ~ 100 us for output load with 100 pF
- We will investigate for other suggested output load values such as 1pF, 10pF, and 1nF.

CML Transceiver



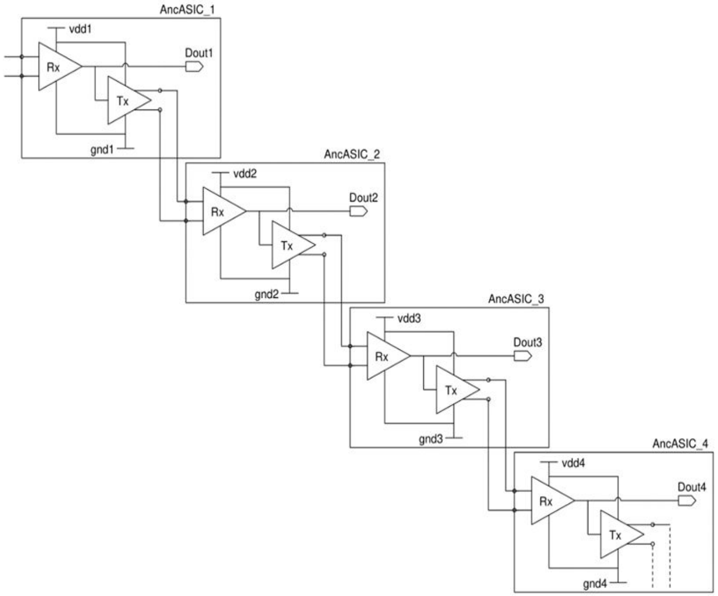
- ❑ Designed to check AC vs DC-coupled slow control links between adjacent serially-powered AncASIC chips

Test plan:

- Transmission loss, time delay, and eye diagram for **single chip tests** and **daisy-chain tests with DC or AC-coupling** with Tx and Rx under different common voltage.

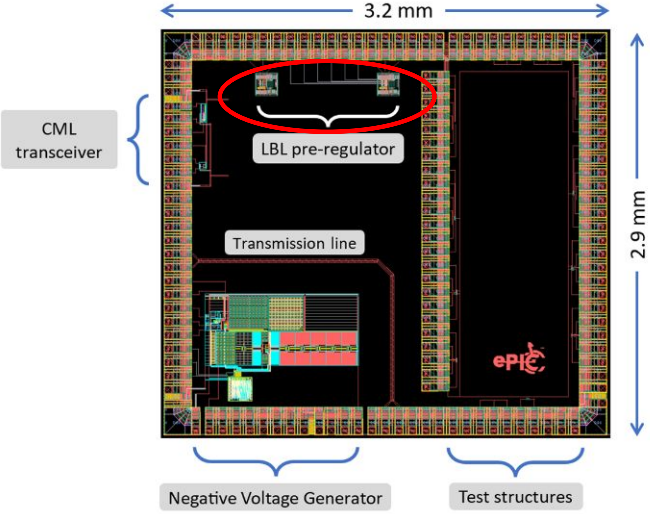
Instrument:

- Power supplies and batteries to set different voltage
- Signal generator
- Oscilloscope



Daisy-chain test structure

SLDO Pre-Regulator



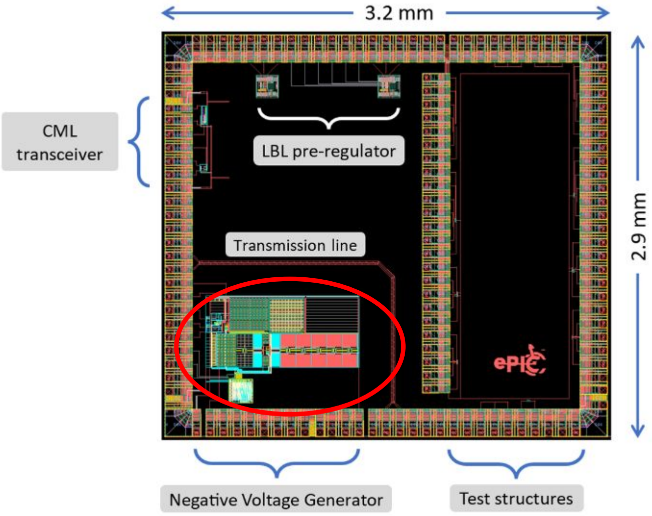
Test Plan:

- **Start-up:** Plot the Vin and Vout signal response while ramping the Vin at specified rates. Determine the voltage at Vin and Vout where the Vout response stabilizes (flat). Vin: ramp 0 to 1.7V; Ramp rates 0 to 1.7V: 10u, 100u, 1m, 10m, 100m, 1s
- **Output Ripple/Noise:** Measure the RMS noise on Vout with Vin at 1.7V using an instrument math function, or with a true-RMS noise meter. Plot Vout at 10 mV full scale at time scales 10 ms, 1ms, …, 1 us per division.
- **Transient Response (overshoot and settling time):** ESR - 3.5k; With Vin at 1.7V plot the Vout signal response while switching a +/- 100uA load onto Vout. Measure the DC value of both signals before and after the step.
- **PSRR and line regulation:** With Vin at 1.7V plot the Vin and Vout signal response while asserting a 10 mV step on Vin. Measure the DC value of both signals before and after the step. If equipment is available, sweep Vin from 10 Hz to 10 MHz at a DC offset of 1.7V at an AC amplitude of 10 mV and plot the Vout response.
- **Load Capacitance:** Repeat the start-up ramping test at the 1pF, 10pF, 100pF, 1nF
- **Temperature Range:** Repeat the start-up ramping test at -30 C, 0 C, 60 C, 90 C

Instrument:

- Power supply, Oscilloscope
- Signal generator to power VDD with ripple
- Environmental chamber for temperature test
- RF Shielding Room for noise measurement

Negative Voltage Generator



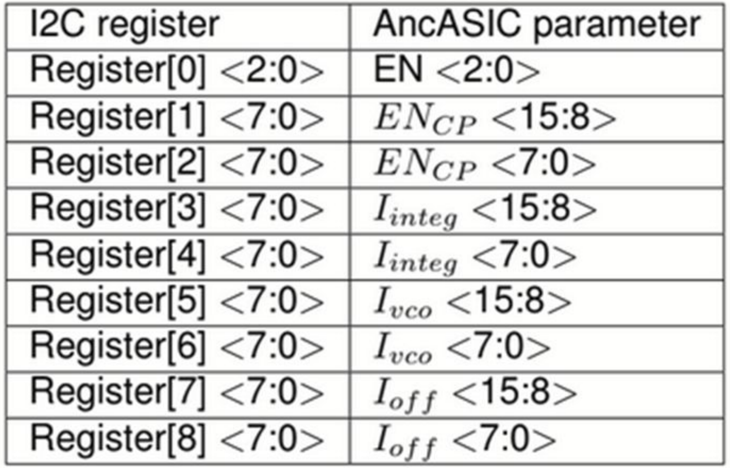
Test Plan:

- **Output range**
  Change Verf, verify:
  $$V_{OUT} = -(20/3)V_{REF}.$$
- **Line regulation**
  Change VDD (1-1.4V), get the curve between VDD & Vout;
- **Transient response**
  Catch the waveform of Vout & Vdd. estimate the rise time, settling time, and peak overshoot as a function of VREF. Repeat for different values of the load current, I_load.
- **Loop bandwidth**
  Repeat test 3 in different f_sc. Verify loop stability.
- **Power supply rejection ratio (PSRR):**
  Inject sinusoidal ripple on the power VDD, measure the ripple on Vout
- **Output noise and ripple:**
  Use oscilloscope record Vout in different Vref & I_load,
  Analyze the output histogram, peak, rms and frequency spectrum.
- **Temperature:**
  Repeat the above tests from 25℃ to 85℃

Instrument:

- Power supply for VDD
- Power supply for Vref
- Oscilloscope
- Clock generator for CLK_SC
- Signal generator for power VDD with ripple
- Environmental chamber for temperature test

Negative Voltage Generator



I2C register	AncASIC parameter
Register[0] <2:0>	EN <2:0>
Register[1] <7:0>	EN_{CP} <15:8>
Register[2] <7:0>	EN_{CP} <7:0>
Register[3] <7:0>	I_{integ} <15:8>
Register[4] <7:0>	I_{integ} <7:0>
Register[5] <7:0>	I_{vco} <15:8>
Register[6] <7:0>	I_{vco} <7:0>
Register[7] <7:0>	I_{off} <15:8>
Register[8] <7:0>	I_{off} <7:0>

I2C configuration map

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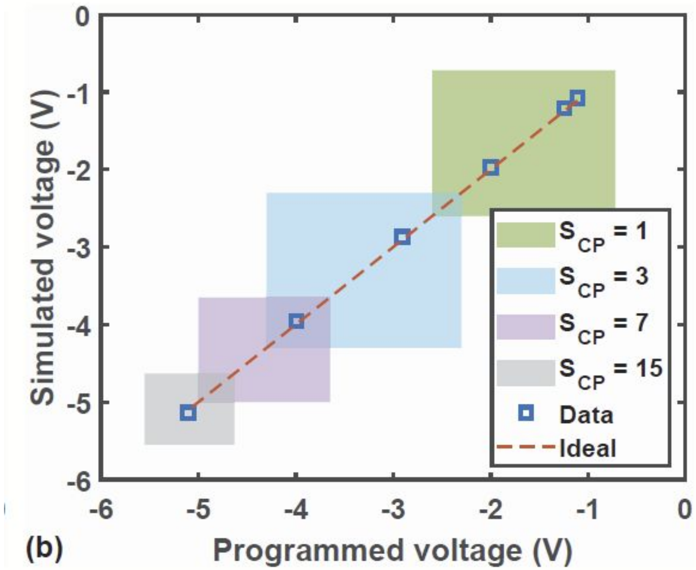
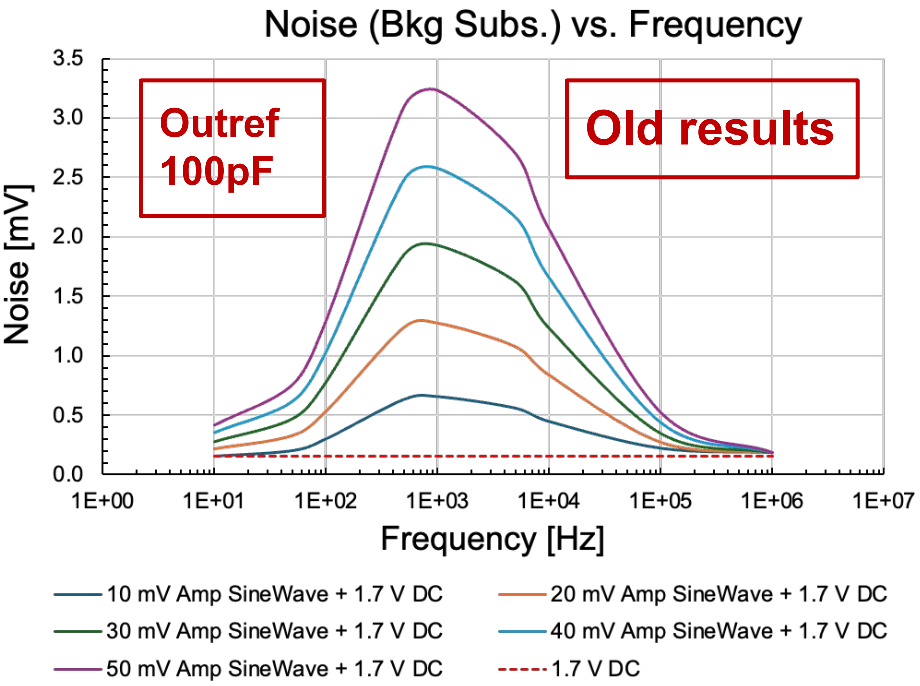


- Output voltage in steady-state obeys the expected relationship

$$V_{OUT} = -(20/3)V_{REF}.$$

SLDO Pre-Regulator

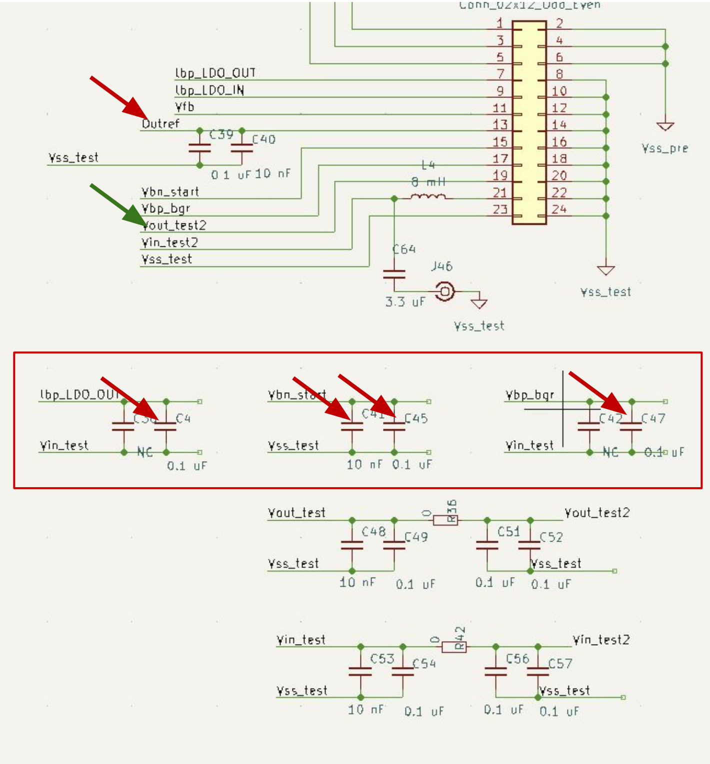
Noise:



Outref 100pF

Old results

- Pre-reg sinusoic 1.7 V
- Sine no and swe
- “Backgr quadrat
- Noise v amplitu
- A deper observe



- “Outref” will be the band-gap direct output voltage (can't drive much load)
- Decoupling capacitors have been removed to make the configuration same as in the final chip version

- “Vout” will be a buffered version of “Outref” (can load with up to 2k/300pF)