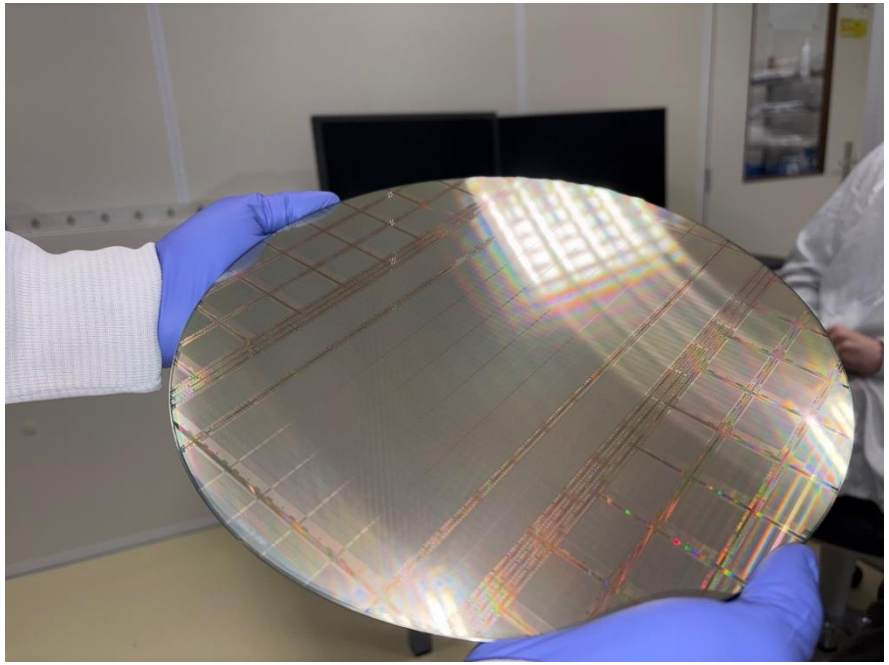
ER2 testing status update

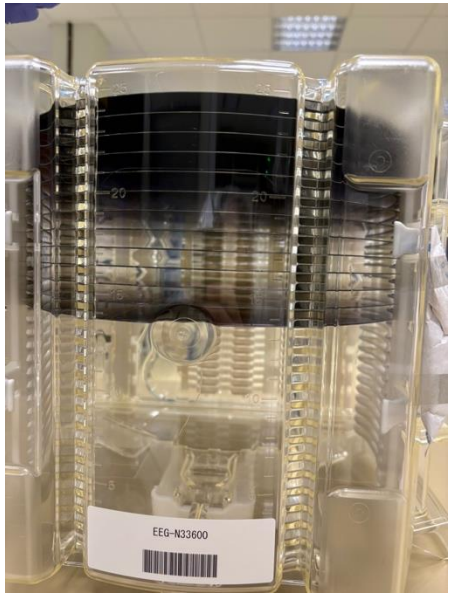
G. Eberwein *on behalf of the testing team*

SVT DSC meeting, 3 March 2026

ER2 arrival

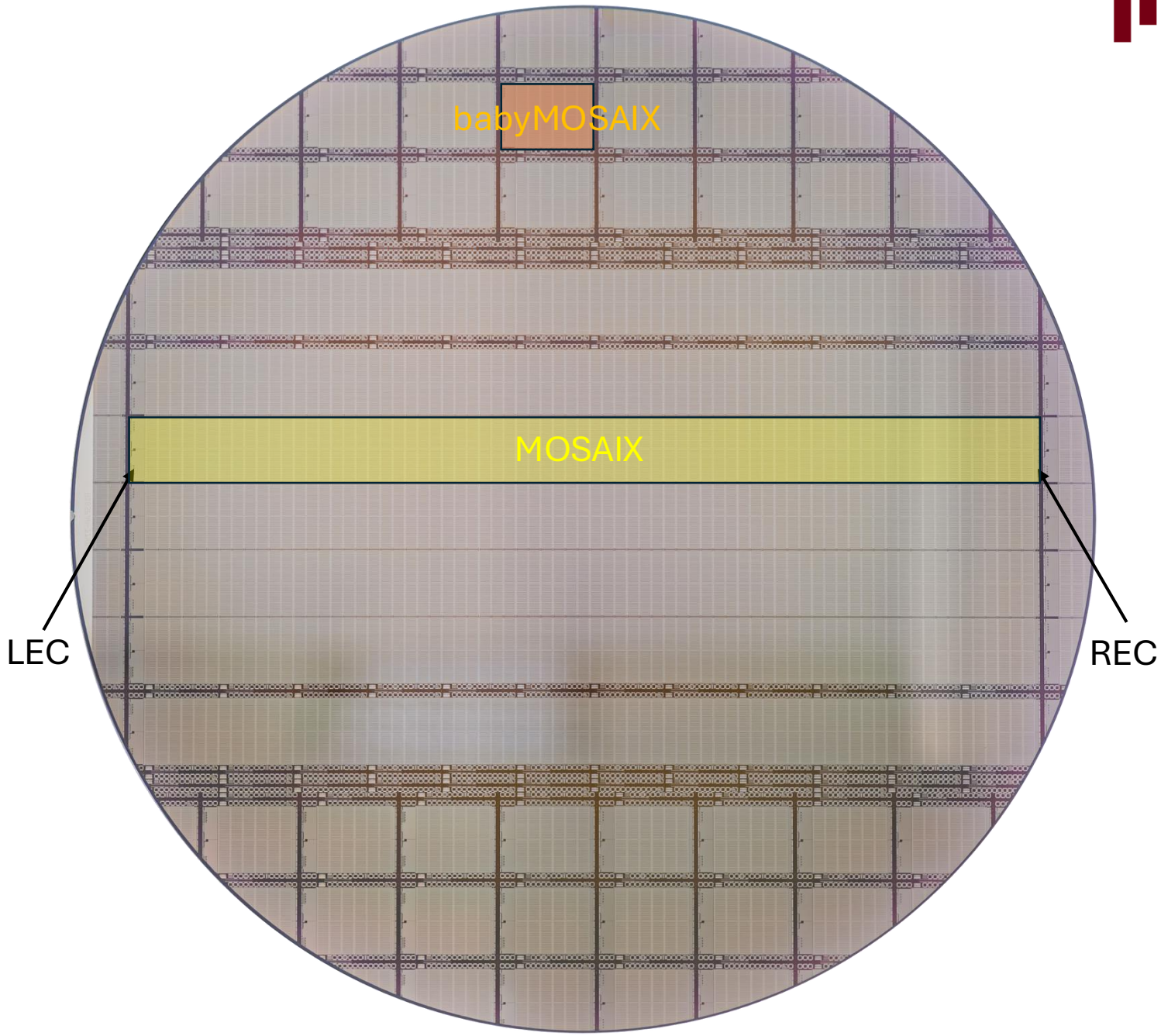
- Wafers received @CERN 16. Feb 2026
  - Lot of 25
- Sorted (partially ITS3 subset for immediate thinning and dicing)
  - First wafer selected for testing





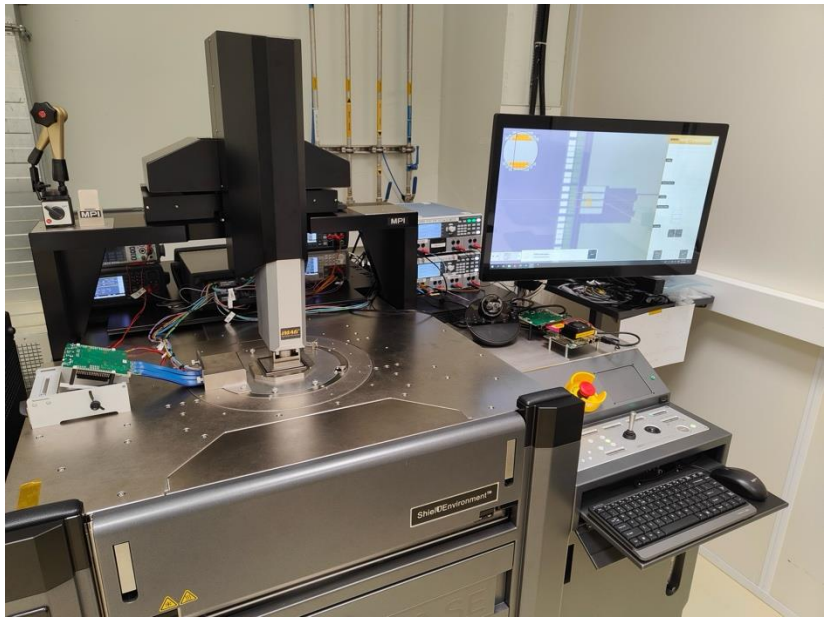
ER2 recap

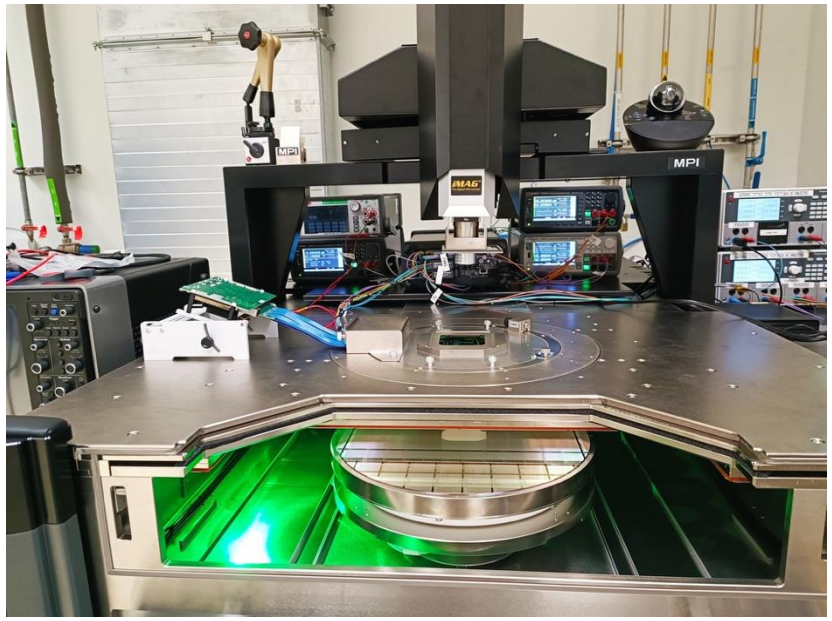
- 5x MOSAIX
- 20x babyMOSAIX
- +50x chiplets

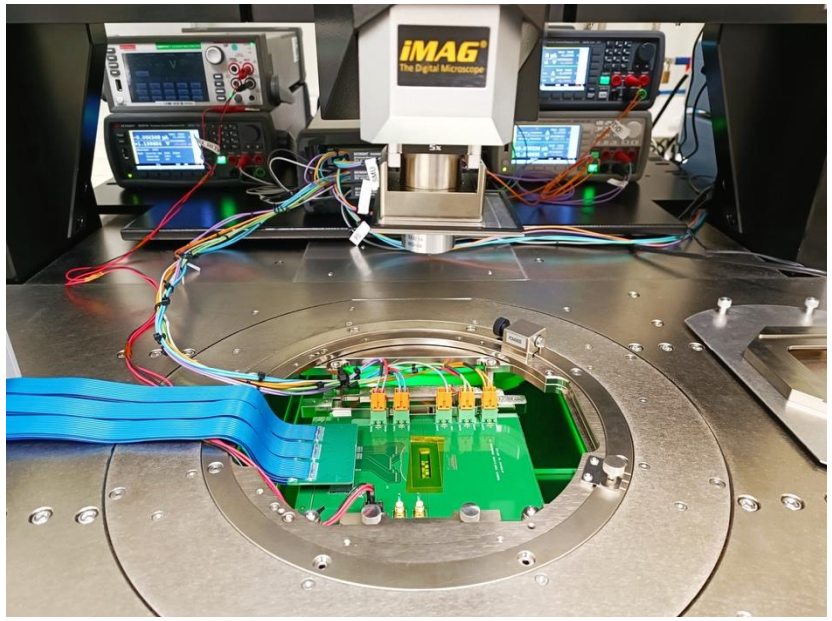


First wafer probing tests

- Day 1 readiness for tests – large effort by ITS3 team (SW/FW/HW)
- Cantilever probecard (low speed) installed in MIT prober, only setup used for first tests
  - Vertical probecard (high-speed) expected next week

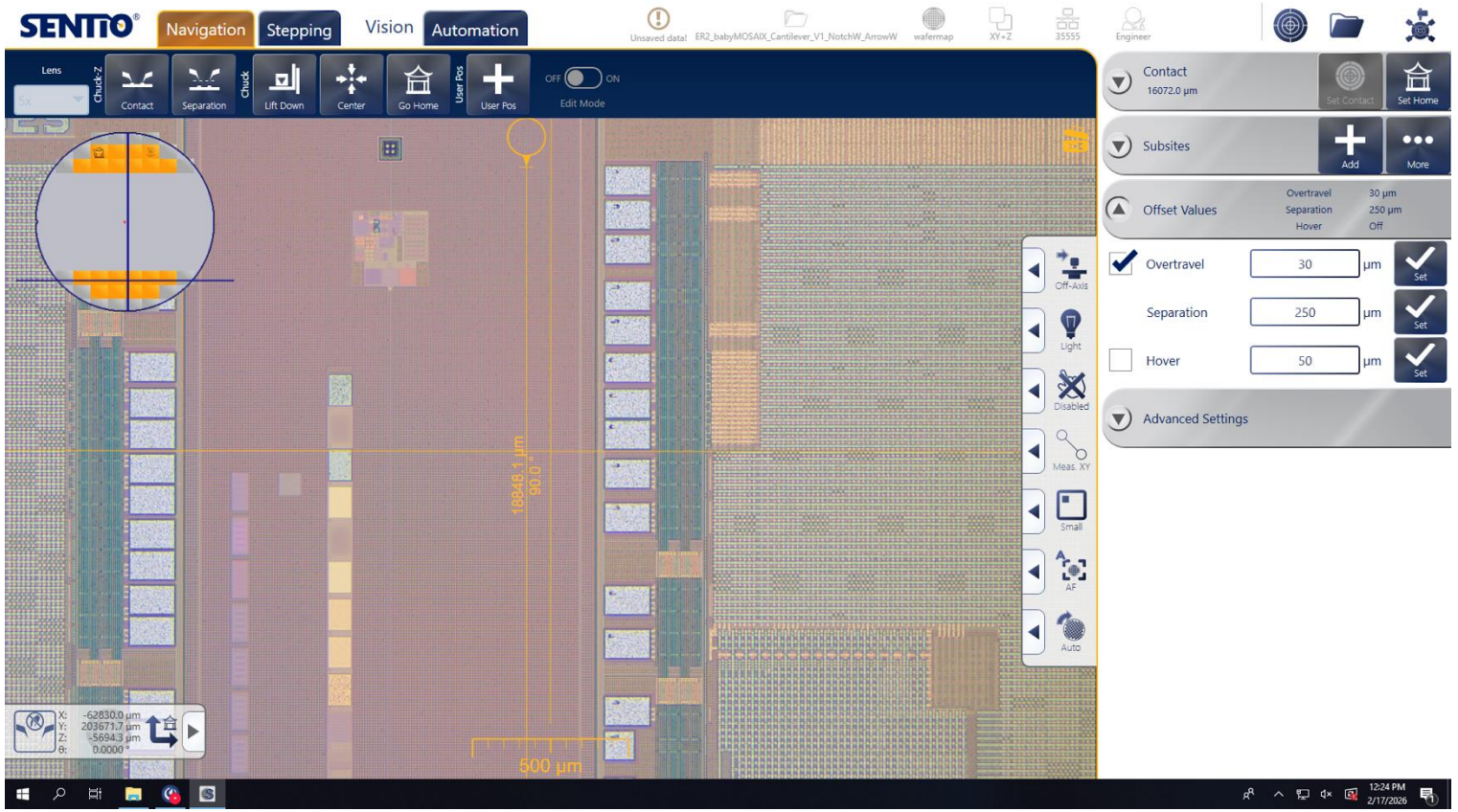






Readiness for probing @MIT waferprober

- Wafer maps were prepared for both babyMOSAIX and MOSAIX using the padwafers
  - ER2 wafers were contacted right after selection of wafer

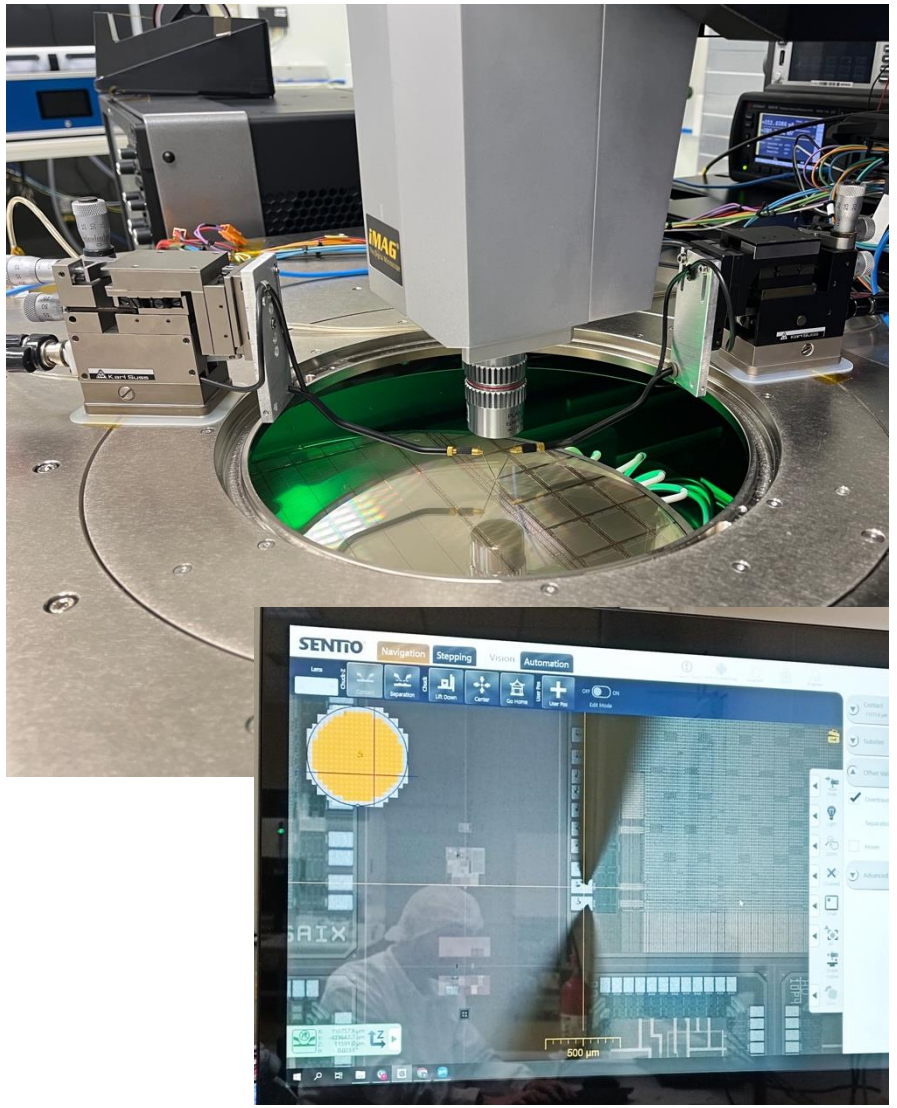


First tests on ER2

- Performed on babyMOSAIX
- Impedance test (-50mV to +50mV scan)
  - Check if there are shorted power domains on-chip
- Power step ramps (ramp-up domains sequentially)
  - Global services domain (GSVDD)
    - Followed by a slow control endpoint check, service nodes needed for tile power switches
  - Global digital and analog domains (GDVDD, GAVDD)
  - Power up tiles by setting service node registers
    - Connect local tile supply monitoring to analog monitoring rail and out-pad

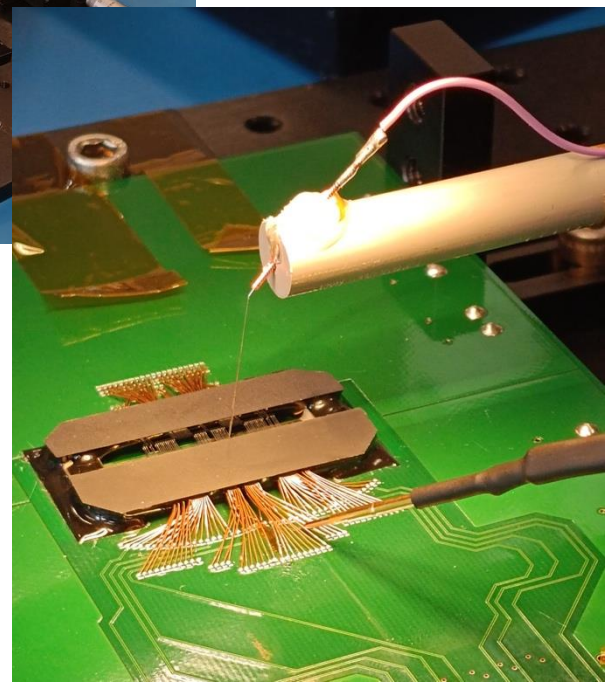
Impedance tests and debugging

- First tests showed concerning GSVDD-GSVSS short
  - Blocked any other tests in sequence
- Immediate debugging needed:
  - Nets probed with adapted micromanipulators
    - No shorts on chip!



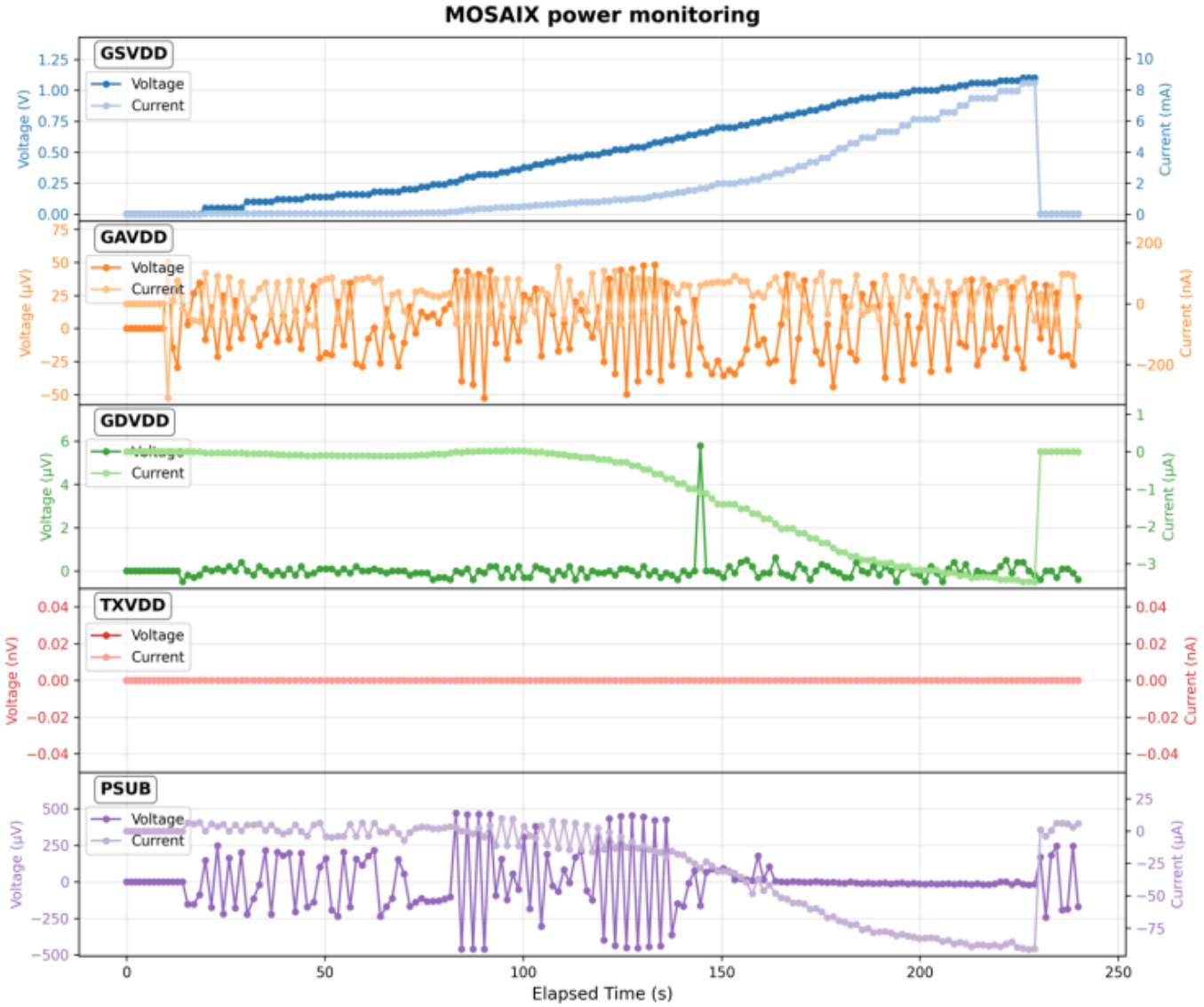
Impedance tests and debugging

- First tests showed concerning GSVDD-GSVSS short
  - Blocked any other tests in sequence
- Immediate debugging needed:
  - Nets probed with adapted micromanipulators
    - No shorts on chip!
  - Made ad-hoc test fixture for probing the probecard
    - Confirmed needle swaps
    - Reworked @CERN
    - Debugged and patched in ~ 4 days



Power ramp-up – global services

- Global services ramped up
  - Reasonable current consumption
- Now one can talk to the chip
  - Reading/writing to services slow control enpoints confirmed
    - Debugged a FPGA locking issue, stable afterwards



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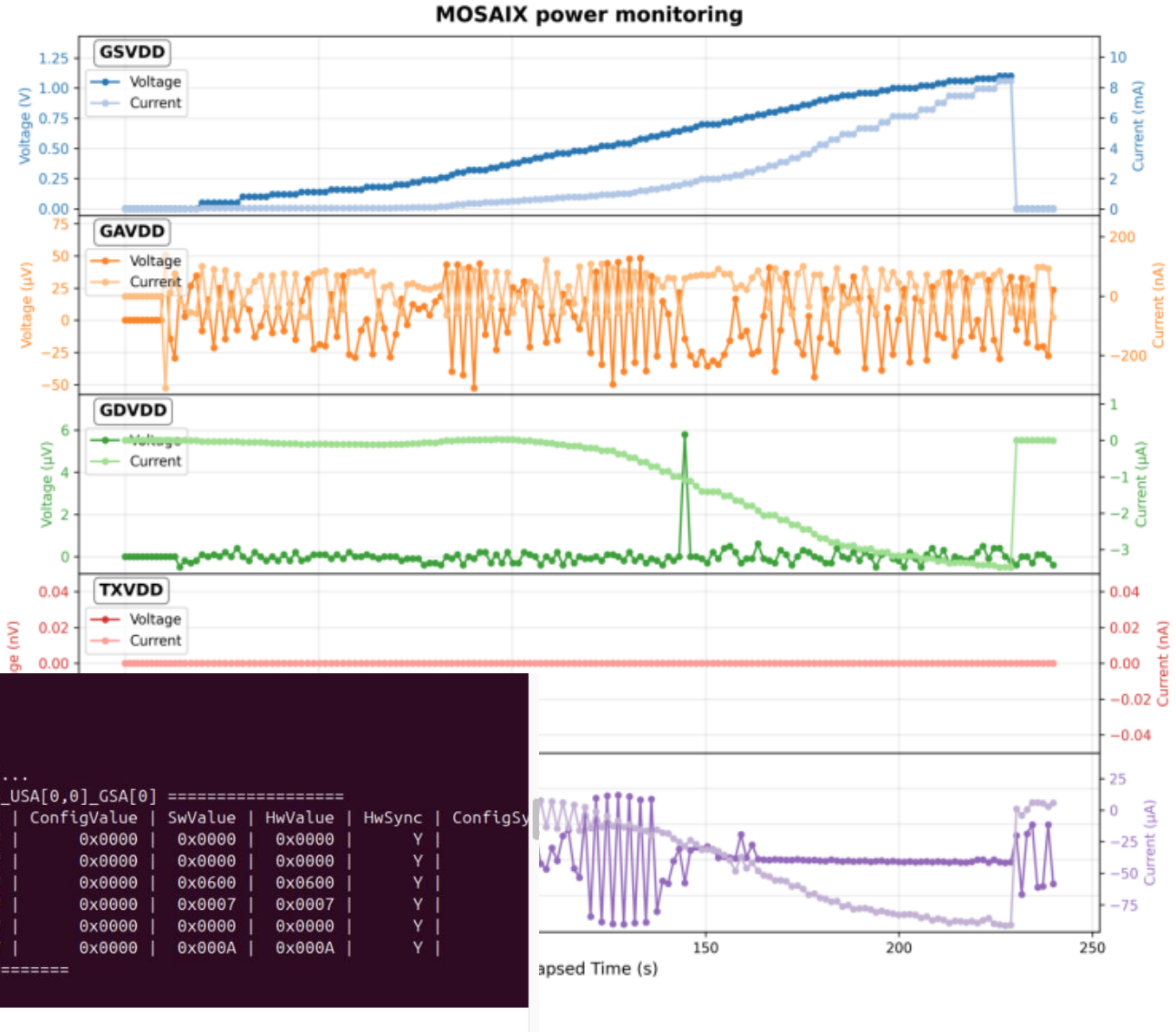
    - Debugged a FPGA locking issue, stable afterwards
  - Sericve nodes can be reached




```
mosaix[0]:sn-USA[0,0]> read-all-registers
INFO     [2026-02-25 14:48:10.186]: Reading all readable registers from hardware...
INFO     [2026-02-25 14:48:10.188]: Read 6 readable registers from hardware
mosaix[0]:sn-USA[0,0]> dump-registers
INFO     [2026-02-25 14:48:12.081]: Dumping ServiceNode USA[0,0] registers to screen...
INFO     [2026-02-25 14:48:12.081]: ================== Register Dump for ServiceNode_USA[0,0]_GSA[0] ==================
INFO     [2026-02-25 14:48:12.081]: Name                            | Address | Mode | ConfigValue | SwValue | HwValue | HwSync | ConfigSy
INFO     [2026-02-25 14:48:12.081]: TILE_POWER_SWITCHES_CFG         |  0x0000 |   RW |      0x0000 |  0x0000 |  0x0000 |      Y |
INFO     [2026-02-25 14:48:12.081]: ANALOG_MONITORING_CFG           |  0x0001 |   RW |      0x0000 |  0x0000 |  0x0000 |      Y |
INFO     [2026-02-25 14:48:12.081]: SBB_TILE_SER_CFG                |  0x0002 |   RW |      0x0000 |  0x0600 |  0x0600 |      Y |
INFO     [2026-02-25 14:48:12.081]: TILE_RESET_CONTROL              |  0x0003 |   RW |      0x0000 |  0x0007 |  0x0007 |      Y |
INFO     [2026-02-25 14:48:12.081]: GATE_SRV_NODE_ENDPOINT_RESPONSE |  0x0004 |   RW |      0x0000 |  0x0000 |  0x0000 |      Y |
INFO     [2026-02-25 14:48:12.081]: SCRATCH                         |  0x0005 |   RW |      0x0000 |  0x000A |  0x000A |      Y |
INFO     [2026-02-25 14:48:12.081]: ================== End Register Dump ==================
mosaix[0]:sn-USA[0,0]>
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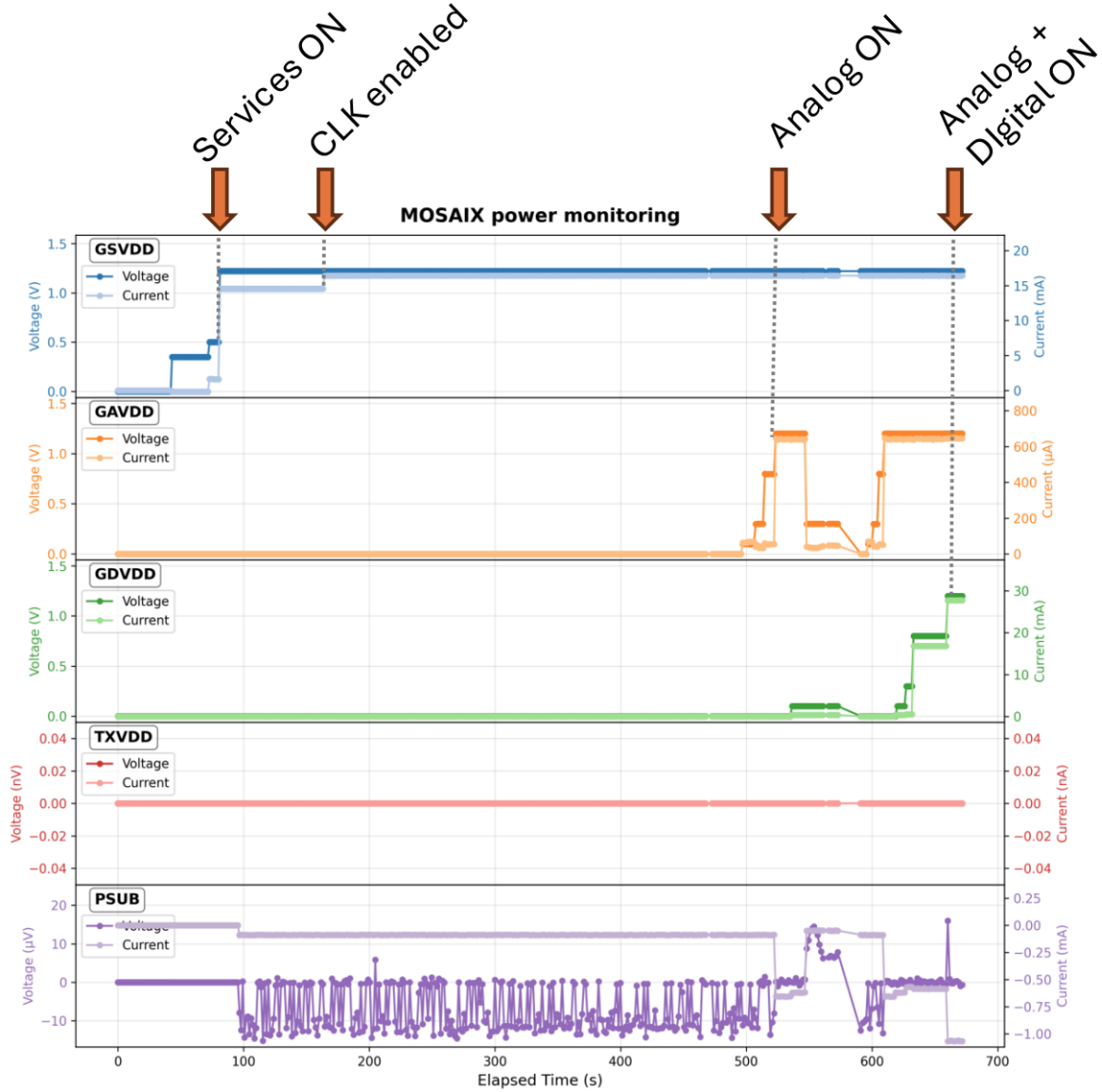
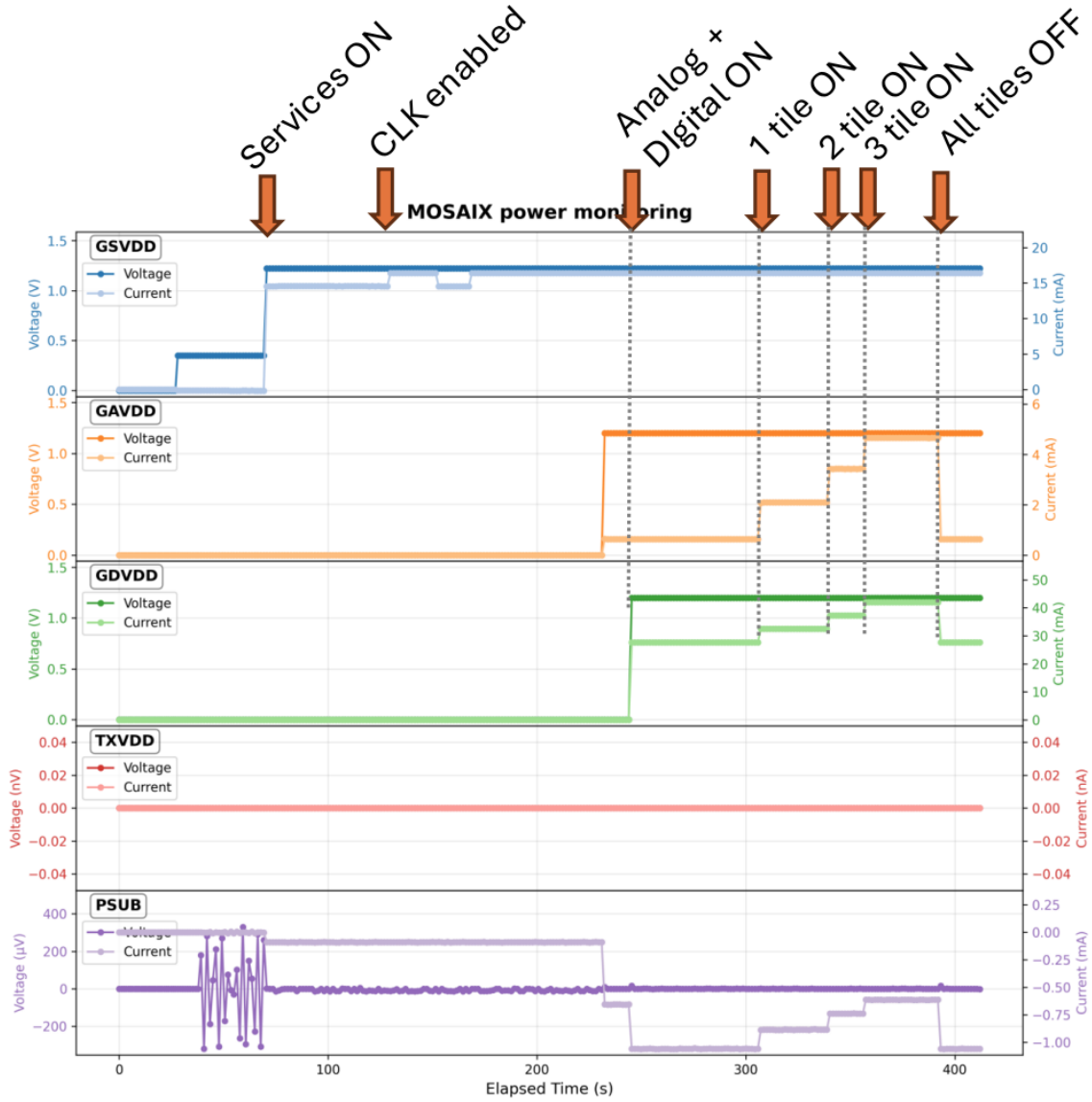
Power ramp-up – global digital/analog

- Successful power-up of the global domains (GSVDD, GDVDD, GAVDD)



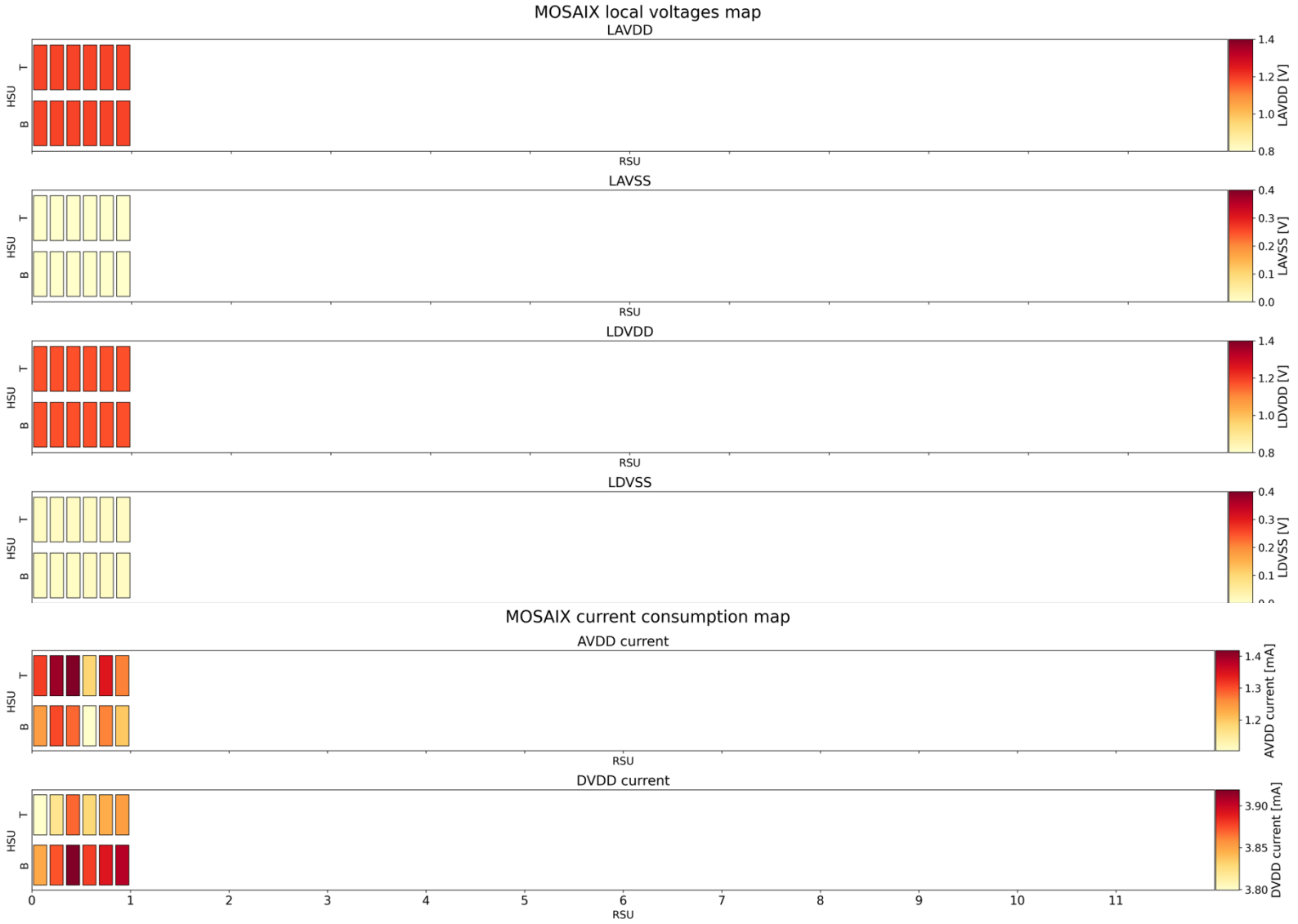
Power ramp-up – tiles

- Successful power-up of the global domains (GSVDD, GDVDD, GAVDD)
  - Now, tiles can be turned on
  - Also, all tiles powered successfully



Power ramp-up – tile monitoring preview

- Tile registers read and written
- Monitoring features working
  - Measured local tile supplies and currents via analog monitoring rail



Summary

- Day 1-readiness for testing achieved
- Probe card issue resolved quickly (~ few days)
  - High-speed probe card expected next week
- Very fast progress after probecard fix
  - Domain independence confirmed (impedance test)
  - Power up services and full babyMOSAIX
  - Service and Core slow control functional
  - Monitoring feature excercised for local supply level
- Smaller refinements being implemented and systematic testing to be resumed