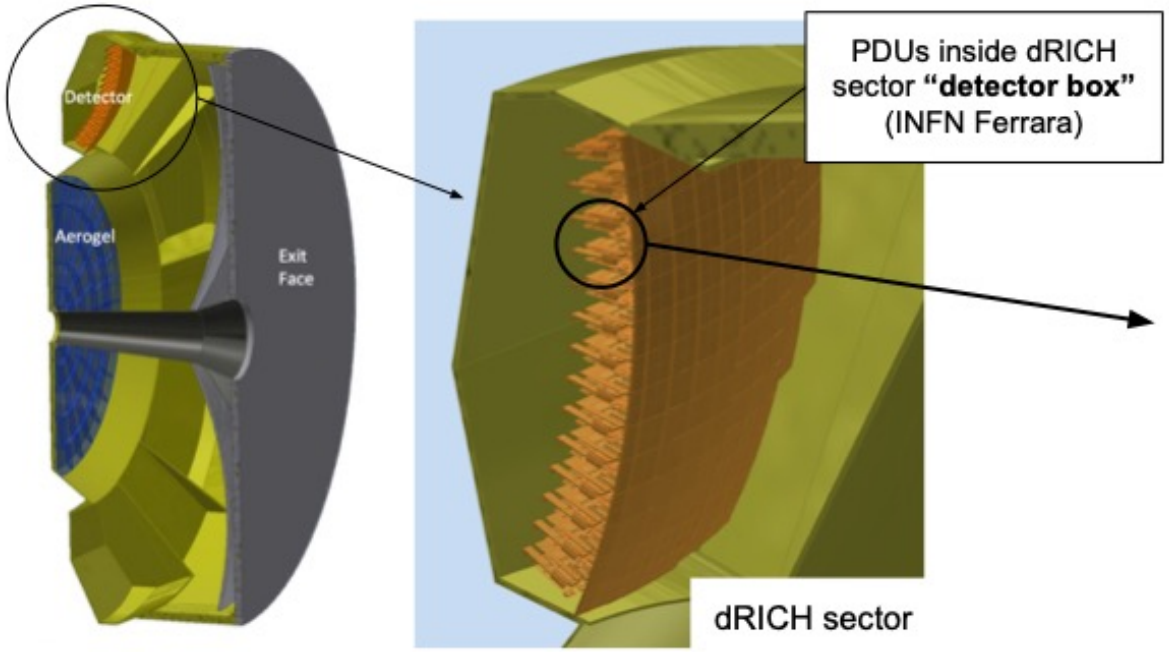
ePIC dRICH DAQ

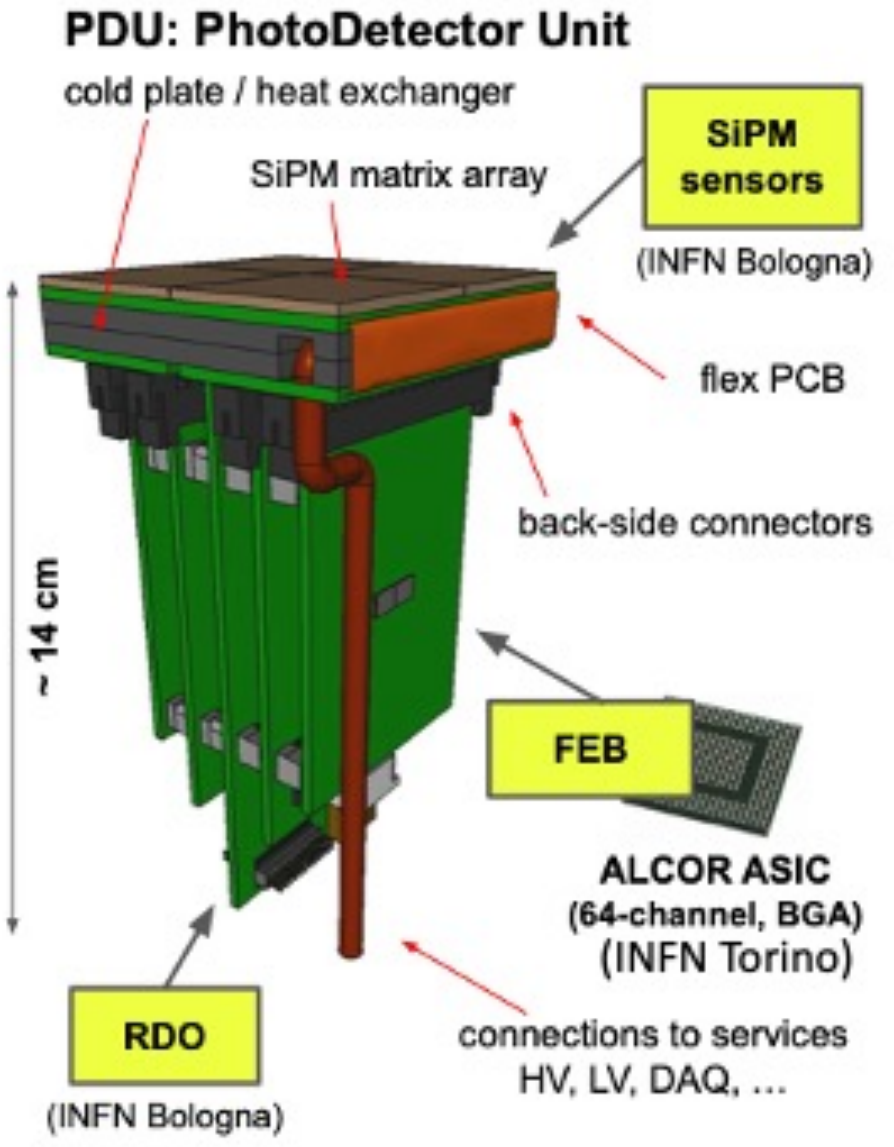
Introduction

P. Antonioli – INFN Bologna

March 26, 2026

dRICH recap in three slides (I): electronics





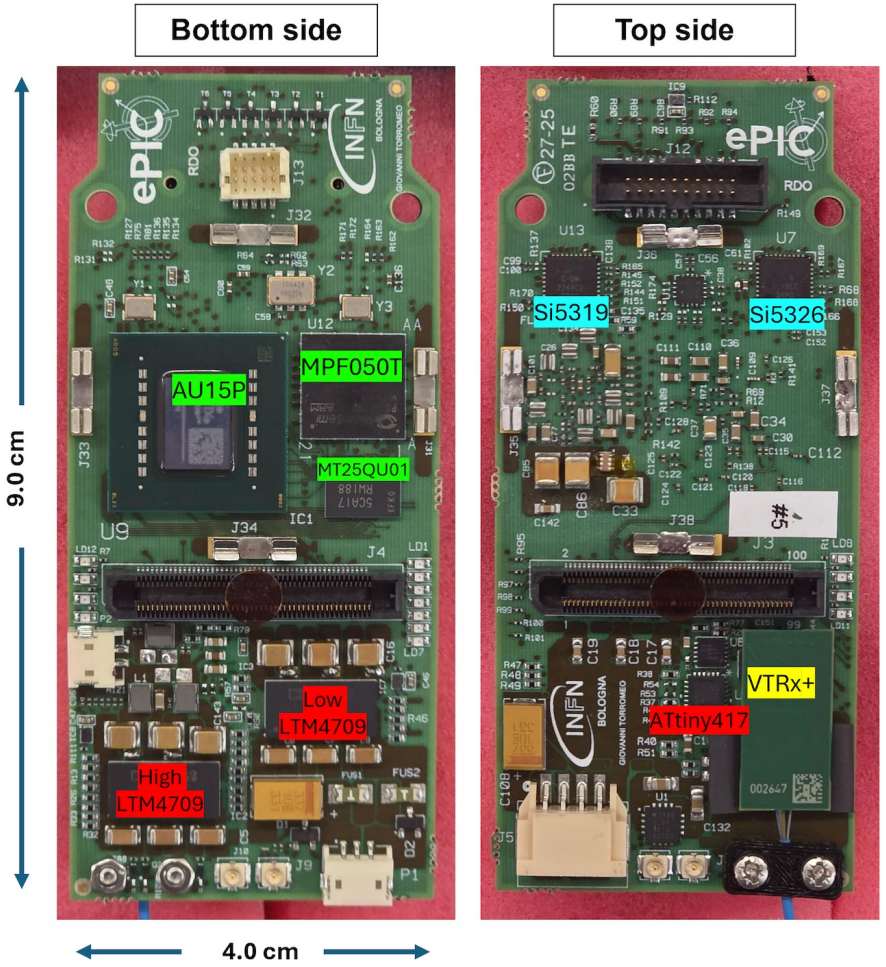
dRICH status & intro : M. Contalbrigo @RICH2025
Photosensors (SiPM): N. Rubini et al., NIM A 1082 (2026) 170890 (Wien 2025)
ALCOR (FEE ASIC): F. Cossio @PD2025
PID performance: T. Boasso @RICH2025
dRICH Interaction tagger: S. Vallarino @EICUG-ePIC 2025
RDO: P. Antonioli @EICUG-ePIC 2025
RDO rad. tests: S. Geminiani @TWEPP2025
ML for data reduction in DAMs: C. Rossi @RICH2025
dRICH DAQ: towards a full push-data architecture: P. Antonioli @SRO XII – Dec 2025
dRICH DAQ from ALCOR to DAM: F. Lo Cicero @ePIC meeting – Jan2026
ALCOR last updates: F. Cossio @Elec&DAQ WG – Mar2026
RDO last updates: D. Falchieri@Elec&DAQ WG – Mar2026

dRICH recap in 3 slides: DAQ building blocks

FEB

ALCOR-64

RDO



FLX-155

dRICH recap in three slides (III): ePIC throughput

Summary of Channel Counts and Data Flow in ePIC

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					187	4976	323	323	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364		1364	30	50	12
PID Cherenkov			318k		143k	1334	1334	1242	1334	33	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		3.4k					25	289	11	37	8
Lumi		128k	5.1k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**2,661**	**10,234**	**2,393**	**4,113**	**113**	**1,774**	**109**

Summary of Data Flow

Aggregate	2.0 Tb/sec
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	2.0 Tb/sec
Per RDO (Avg)	0.7 Gb/sec

Aggregate	115 Gb/sec
Collision Signal	62 Gb/sec
Synchrotron Rad	6 Gb/sec*
Electron Beam	4.5 Gb/sec
Hadron Beam	1.0 Gb/sec
Noise	41 Gb/sec

Scale of the system:

- **Electronics**
  - ~ 25 detector subsystems
  - ~ 5 Readout Technologies
  - ~ 2500 RDOs (on detector/in racks)
  - ~ 110 DAM boards (DAQ room)
  - GTU (with interface boards)
- **Maximum Data Volume**
  - ~ 2 Tb/sec digitized
  - ~ 115 Gb/sec recorded
- **Online Computing (Echelon 0)**
  - ~200 nodes (DAQ Room/SDCC)

* Synchrotron radiation caveats:

1. Rates are based upon hit rate for all ePIC detectors. In fact, data volumes depend upon specific detector hit (64 bits/hit assumed)
2. Highest Synchrotron radiation / electron beam gas will correspond to lower values for collision signal
3. Plan to analyze by component soon

dRICH is one of the **bad guys** within a continuous readout approach for ePIC

Slide courtesy: D. Abbott and J. Landgraf

Note

at EIC zero-day (and during all commissioning) throughput will be 10^2 lower

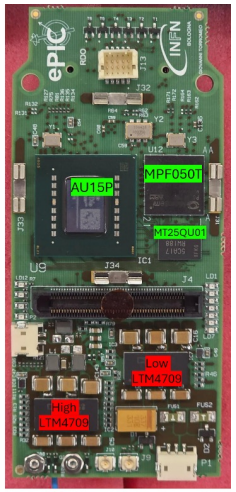
how to approach dRICH throughput?

0	cool down the sensors → -40 C heal the damage → annealing optimize overvoltage and choice of the sensors	sensors	INFN-BO/INFN-FE/
1	electronics gated: ALCOR shutter	electronics, clock distribution, RDO	INFN-TO/INFN-BO
2	understand if the event is noise or signal → **deploy ML techniques on DAM**	DAM	INFN-RM
3	understand if the event is noise or signal with a **dRICH interaction tagger** → give a trigger to DAM		INFN-GE
4	get an external trigger from another sub-detector (Forw. HCAL?) → give a trigger to DAM		ePIC

dRICH DAQ building blocks

INFN-TO

- ALCOR-64 design/validation
- FEB design/production
- packaging / test
- radiation tests

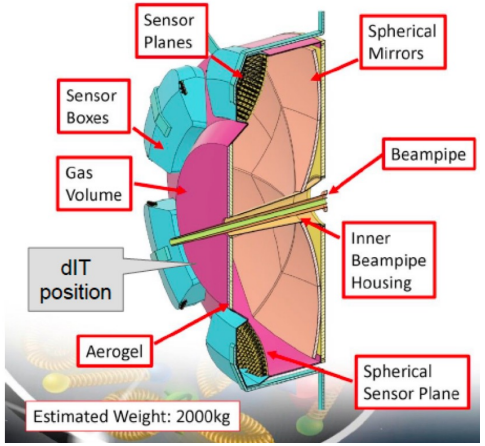


INFN-BO

- RDO design/validation
- RDO design/production
- Test Bench RDO
- RDO – DAM link over VTRx+
- radiation tests

INFN-RM

- DAM “DAQ” firmware
- ML algorithms → neural networks
- RDO – DAM communication
- DAM – GTU communication



INFN-GE

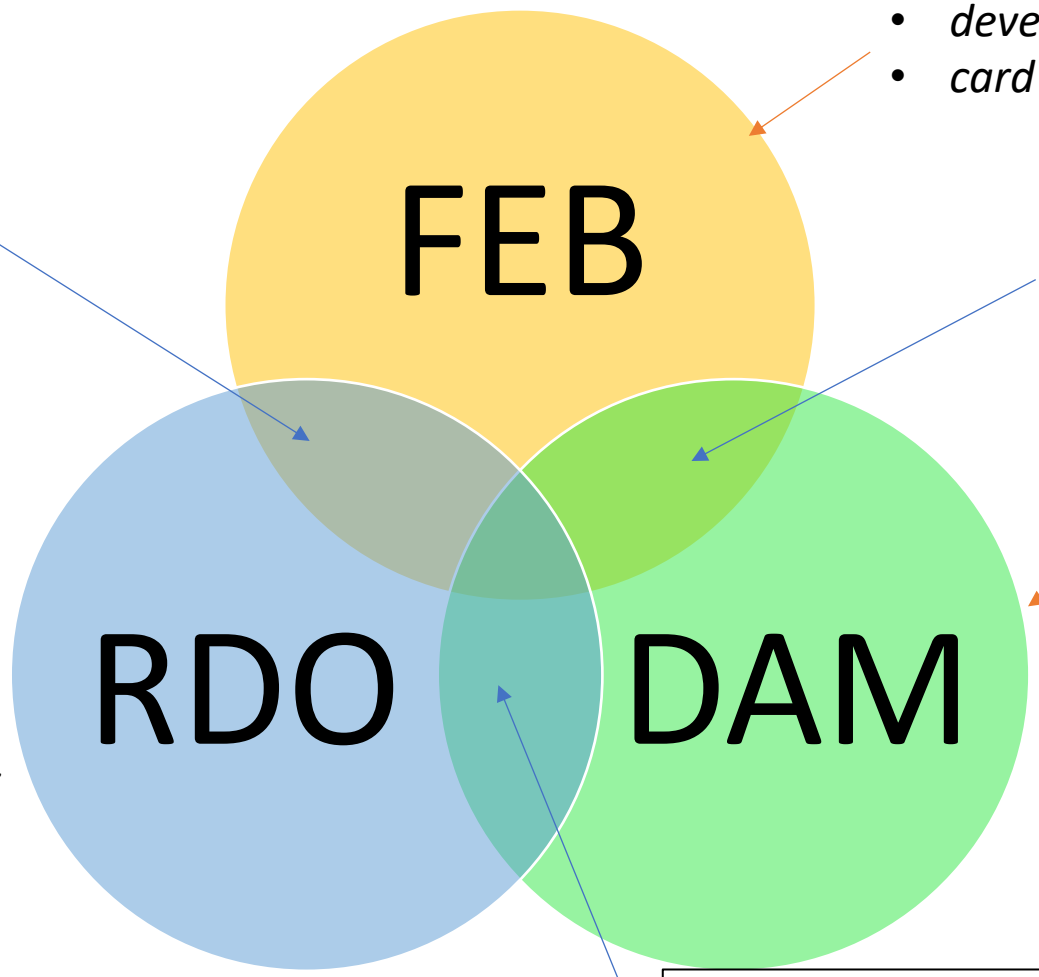
- dIT design/simulation
- dIT test (scint. fibers)
- dIT → validation
- dIT → construction
- dIT to DAM (or to GTU)

dRICH DAQ: key joint areas

DAQ WG: INFN BO + INFN RM + INFN TO / meeting every 2 weeks / mailing list available to subscribe

shutter
time ordering
ALCOR data
ALCOR bus

- *develop ALCOR*
- *card design + production + test*



configuration load
slow control

- *FPGA firmware*
- *NN model – performance*
- *communication with GTU*
- *communication with echelon*

- *FPGA firmware*
- *card design + production + test*

opt. link. protocol
clock recovery
time ordering (calibrated data)
data format

dRICH DAQ: today agenda

are ALCOR data pushed ordered by time?
→ Chiara Ferrero [ALCOR simulations] INFN-TO

how we can optimize data at RDO level to help DAM processing
→ Sandro Geminiani [RDO status] INFN-BO

Activities for back-end design and development
→ Ottorino Frezza [DAM status] INFN-RM

preliminary DATA FORMAT proposal relevant also for implementation of ML algorithms on DAM

NEXT:
- Neural Network / Machine Learning algorithm performance
- dIT status

dRICH throughput modelling (I)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM	30
Input link in DAM	42
Output links from DAM to TP	1
Number of DAM Trigger Processor	1
Input link to DAM Trigger Processor	30
RDO-DAM Link Bandwidth (VTRX+) [Gb/s]	10
DAM to Echelon-0 Switch Bandwidth [Gb/s]	100
dRICH Interaction tagger reduction factor	1
Interaction tagger latency [s]	1,00E-04
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	(if you put 10 ns == no shutter)

There are two reduction handles in this table:
- the shutter
- something external (can be NN on DAMs, dIT or ..?)

dRICH backend DAQ reorganized following studies from INFN Rome (see next slides) from 27+1 to 30+1 FLX-155: 30 DAMs + 1 Trigger Processor (TP)

Reduction factor via shutter
RF = 10 ns/(shutter width)

Reduction factor provided by whatever external trigger (including NN on dRICH DAMs)

dRICH throughput modelling (II)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	1		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	2	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

This is worst case!

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	55,20	800,00	
Throughput to serializer [Mb/s]	34,50	788,16	
Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
Input at each DAM [Gbps]	45,28	420,00	
Buffering capacity at DAM [Mb]	4,64		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	1.358,44	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

*Take home message

Using only the shutter with a reduction factor 5 (2 ns over 10 ns BC) we keep 1.3 Tbps throughput and we stay within all limits (including transfer from DAM to Echelon-0)

dRICH throughput modelling (III)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	5		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	10	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	276,00	800,00	
Throughput to serializer [Mb/s]	172,50	788,16	
Throughput from ALCOR64 [Mb/s]	1.380,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	5,39	10,00	based on VTRX+
Input at each DAM [Gbps]	226,41	420,00	
Buffering capacity at DAM [Mb]	23,18		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	6.792,19	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

10 ns means no shutter

data reduction via "another method"

further risk mitigation here might be applied using two TX links instead of one

*Take home message

If shutter is not effective we need a reduction factor 5 from a dRICH interaction tagger method and we stay within all limits (including transfer from DAM to Echelon-0)

Will the shutter be effective?

Simulations of hit time distribution at dRICH entrance window (before aerogel) within the context of dRICH Interaction tagger studies

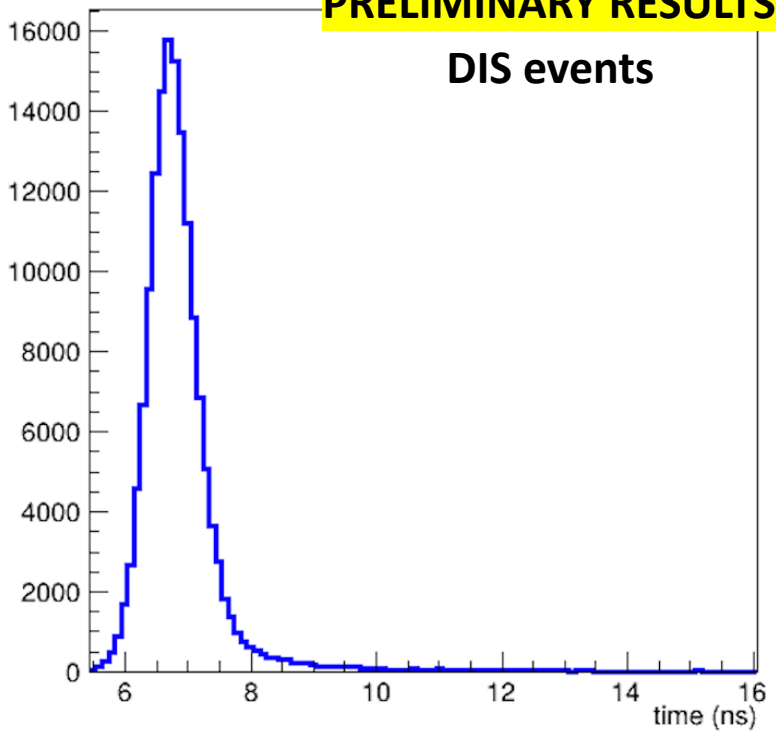
- Hit time distribution (primaries) has Gaussian shape + a tail
- Bulk of primary hits lies **within 2 ns** ($\sigma_{pr} \cong$ 260 ps**)**
- added in quadrature time zero jitter (σ_{t0}= 250 ps) + front-end resolution (σ_{FE}= 150 ps)

$$\sigma = \sqrt{\sigma_{pr}^2 + \sigma_{t0}^2 + \sigma_{FE}^2} \approx \text{ 400 ps}$$

- from cumulative distribution 99% of particles included with a shutter window of 5 ns (from 5.5 ns to 10.5 ns → **50% DCR data reduction**)

PRELIMINARY RESULTS

DIS events



Full simulation in progress:

→ we don't expect a large spread added by photon emission + propagation (confirmed already by simulation)

→ impact of time slewing effect to be assessed (could impact with the need of 2 ns additional window – see backup)

Towards full data-push architecture: time ordering

The problem: ALCOR timestamps are not *"immediately"* out

Pixel TDC conversion defines time required for digitization:

- TDC max conversion time = 1.5 x 128 = 192 clock cycles ≃ 500 ns
- TDC min conversion time = 0.5 x 128 = 64 clock cycles ≃ 170 ns
- Max ΔT = 500 ns - 170 ns = 330 ns (inside ALCOR channel) → down to the column and transmit off-chip

ALCOR data transmission:

- 1 word: 40 bits → 40 b / 788 Mb/s = 51 ns per event word (we have 8 channels for each Tx link)
- If no other hits in the column, 2 hits (separated by 128 clk cycles in the pixel) are only separated by idle words (K.28.5 "comma" are filtered by RDO) → [dependency on data rates → see Chiara's talk]

- Time reference given by ALCOR frame structure →

@DCR = 300 kHz/ch, Δt_{frame} = 12.7886*0.092 μs → $N_{events} = 8 \cdot DCR \cdot \Delta t_{frame} = 28.3$

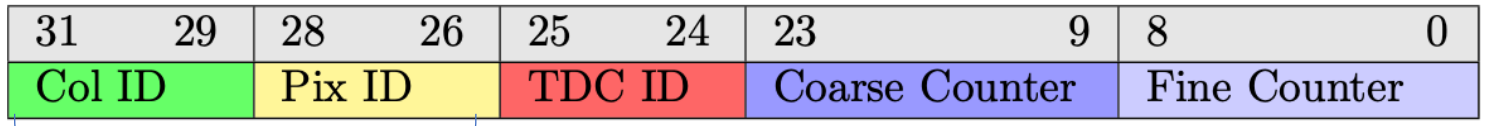
- 28.3 event words per frame (mean value, 2x in ToT mode, add physics)

→ can hits be sent time ordered (BC) by RDO to ease DAM work? → see Sandro's talk

ALCOR data (raw) and ePIC data (I)

ALCOR hits "event word" are timestamps

accelerator BC: bits 23 – 11



3 bits to identify the column (LVDS TX lane) [0 to 7]

3 bits to identify the pixel [0 to 7]

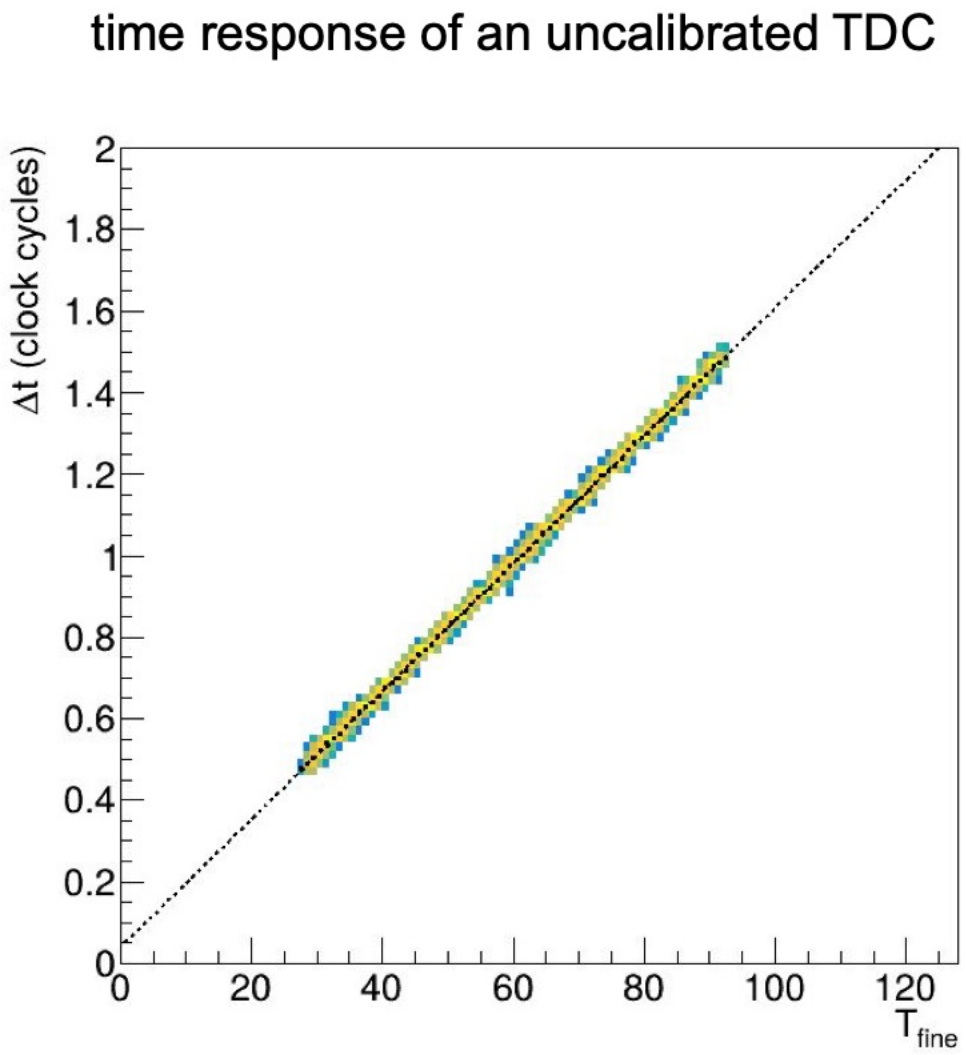
4 TAC TDC IDs: 2 bits
→ 2 TDCs for leading edge
→ 2 TDCs for trailing/slew rate

these nine bits are the fine measurement of the TDC
you can reach 20-40 ps LSB at 394 MHz.
Calibration needed → can't be used at DAM level "as it is"

394 MHz → coarse counter LSB 2.54 ns (currently 320 MHz → 3.125 ns)
15 bit coarse counter (0x7FFF = 32767)

Coarse counter expires every 83.228 µs > 12.78 µs (EIC orbit)
At each EIC orbit we get a RevTick signal from DAM (main EIC "synch")
→ this trigger a coarse counter reset and a frame structure injected in data flow

Time Calibration



the 9 bits of Tfine report the absolute time of the hit with respect to clock (phase) with 9 bits encoding

Tfine → to be converted in values ranging [0.5 – 1.5]
→ Tphase = Tfine*A + B

+ offsets (inside B)
+ time_walk effects (this is for offline!)

see RobertoP presentation at DAQ meeting 27/2/2026

ALCOR data and ePIC data (II) + link protocol

DISCLAIMER NOTICE: all this is VERY 

RDO "prepares" data reduction
DAM "does" data reduction

RDO

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

- 51-bit AWORD: leading + trailing
- Bit optimization: EIC orbit / and max ToT
- 51/64=**21% data reduction**

opt-link protocol

	DF3	DF2	DF1	DF0	DCS (free)		AWORD		AWORD		AWORD		AWORD	
FULL	255	254	253	252	251	204	203	153	152	102	101	51	50	0
lpGBT	223	222	221	220	219	204	203	153	152	102	101	51	50	0

link protocol operated at **39.4 MHz** CLK (5/2 of EIC clock, close to LHC clock)

- Protocol over optical link: FULL (256 bits/CLK or lpGBT (224 bits/CLK with FEC5)
- if lpGBT, likely used without e-link: "hybrid" mode à la ALICE/GBT
- space for DCS bus (SWT à la ALICE-ITS2)

DAM

- extract BC from bits 21-11
- extract geographic position from RDOID (DAM is link-aware) + FEBID (49-48) + AlcorCh (29-24): geo info → data pattern

dRICH data words

DISCLAIMER NOTICE: all this is VERY 

LEADING TIMESTAMP

TRAILING (OR SLEW RATE) TIMESTAMP

dRICH CHANNEL ID

CONTROL

63	62 50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
0	RDO ID	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Column ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

63	62 50	49 48	47 16	15 0
1	RDO ID	FEB ID	Slow Control Word (to be defined)	Slow control ID (include ALCOR K codes)

- when NN decision is reached, the DAM must add to the 51-bit word the 11 bits of the RDOID
- dRICH data words out in timeframes to SRO computing as 64-bit words over PCIe
- just data from “accepted bunch crossing” will be out + control words

To be worked out:

- full data encapsulation of orbits
- Slow Control Protocol / Word and related data format
- from ALCOR frame (= EIC orbit frame) to “ePIC streaming readout timeframe”

dRICH DAQ: on-going work

(more details in subsquent talks)

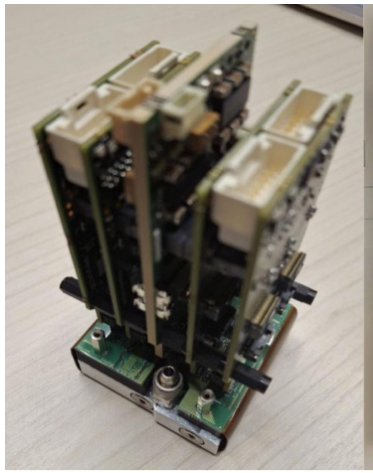
- irradiation tests → RDO → scrubbing (next 28 March!)
- by July → RDO – DAM protocol using ePIC FADE card
- by July → DAM – GTU protocol using ePIC FADE card + FLX-182
- September → RDO irradiation test (full scrubbing)
- December → RDO irradiation test (to choose between FULL/lpGBT protocols)
- by December: readout integration test RDO-DAM in Bologna (reading prototype)
- by December: start practicing on FLX-155 (depending on availability → see El&DAQ meeting tomorrow)

- two master thesis on RDO aspects (time data calibration [M. Dubovskov], recovered clock and data link protocol [M. Panza])
- one PhD thesis on RDO [S. Geminiani]
- one PhD thesis on DAM/neural nework algorithms [C. Rossi]

Conclusions and outlook

- dRICH DAQ building blocks almost on place
- a lot of firmware ahead of us!
- a good and challenging plan for 2026: (ALCOR64 unavailability in 2026 is not a stopper)

PDU



RDO

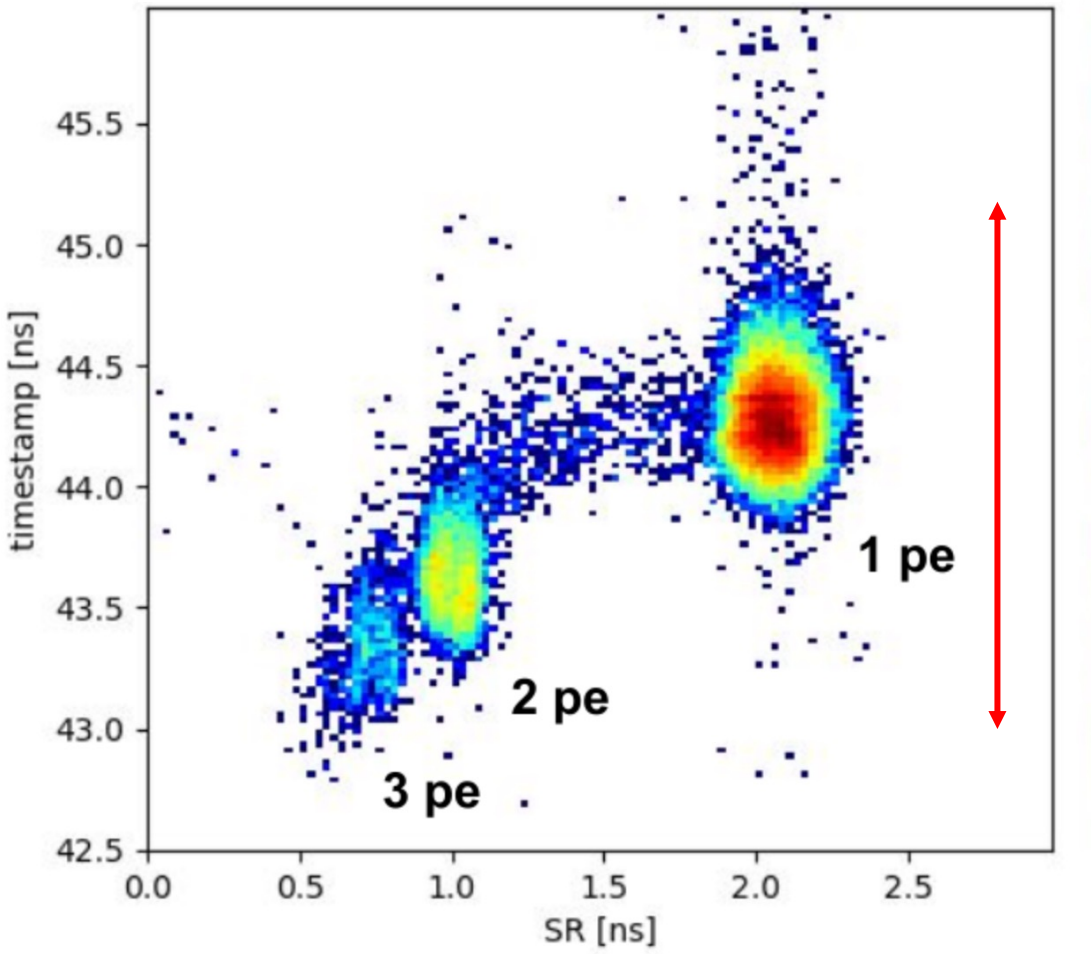
DAM

ALINX + FADE (mimicking GTU)


BACKUP

Further analysis: time slewing warning

Time slewing effect due to multiple photons



For the fraction of events when we will have > 1 pe we can expect an additional shift of ~ **2 ns**!

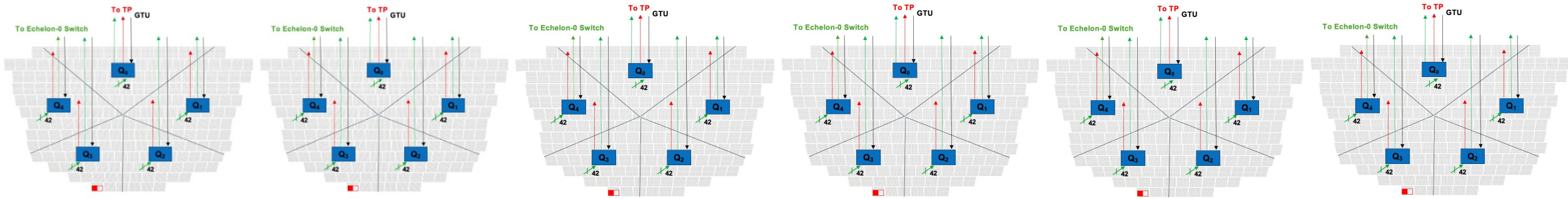
How many times we have more than 1 pe?
Note we have also SiPM-cross talk here.

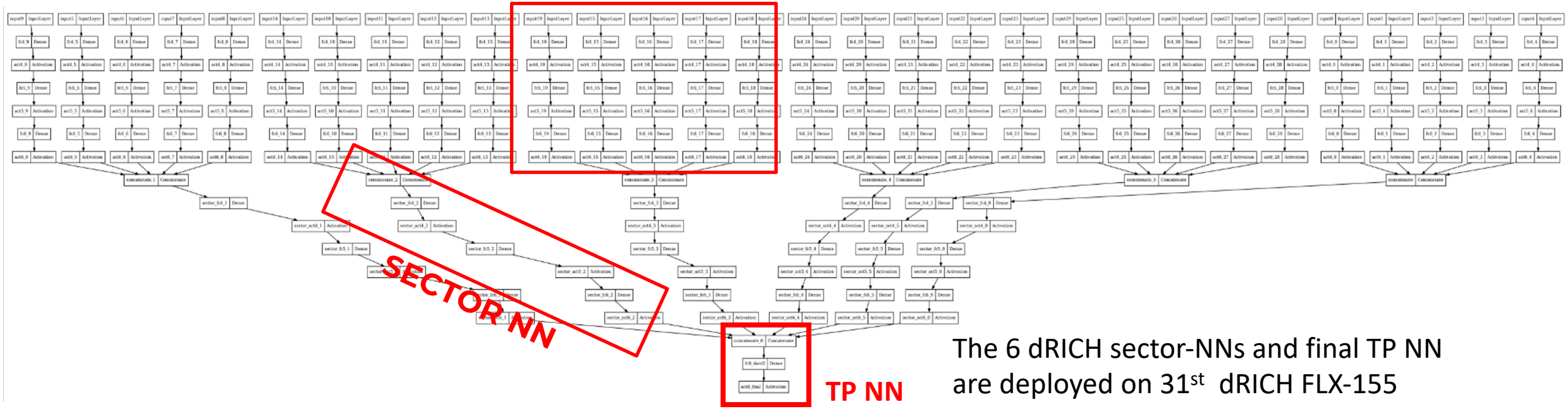
To be fully simulated.

Shutter could be “off” 5 – 3 ns
→ Shutter reduction factor 0.5 – 0.37

NN deployment model and DAMs

6 dRICH sectors – 5 DAMs/sectors





The 6 dRICH sector-NNs and final TP NN are deployed on 31st dRICH FLX-155

dRICH RDO requirements

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus towards FEBs
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- **opt. tranceiver** must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps