ALCOR simulations

studies on data time ordering

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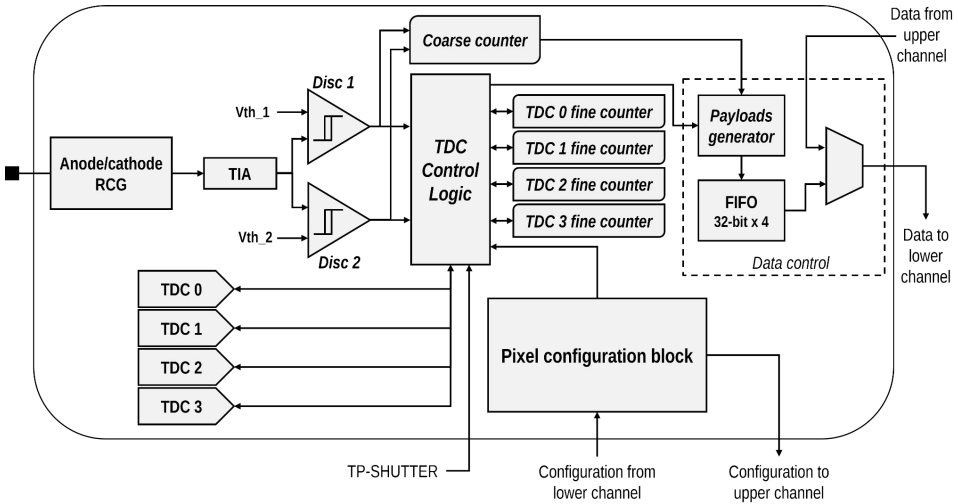
Motivations

ALCOR-64 pixel architecture



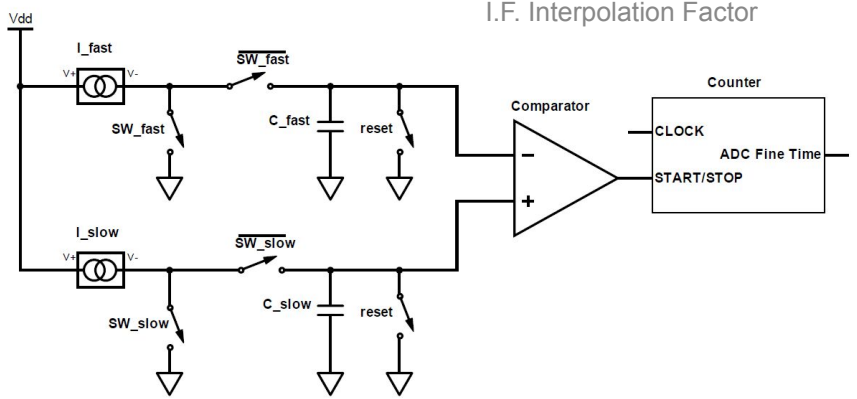
- Low impedance input stage + TIA + 2 leading edge discriminators
- **4 TDCs** based on **analogue interpolation** with **20-40 ps** time-bin (at **394 MHz clock** frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- TP-**Shutter** to inhibit events digitization (asynchronous with ns time window) and **suppress out-of-time SiPM DCR hits**

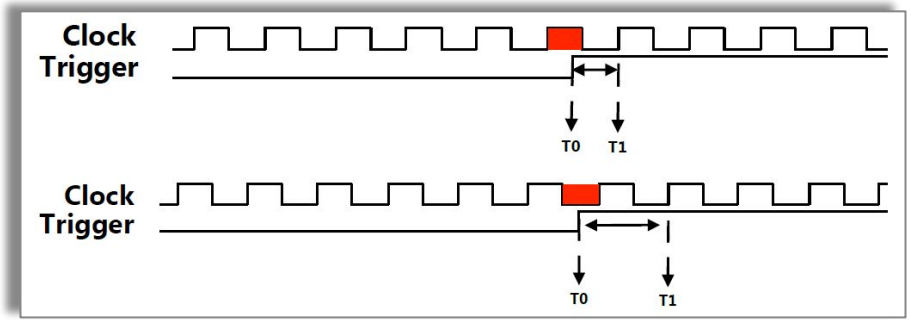
- Studies on the data output order are needed to understand how to handle data in the next stages (RDO + DAM)

Time to Digital Conversion

- **Coarse time**: 15-bit clock counter @400 MHz
  → T_{clk} = 2.5 ns
- **Fine time** measurement performed by TDC based on **analogue interpolation**:
  - Measure phase between asynchronous trigger (T_0) from discriminator and clock rising edge (T_1)
  - I.F. 64 or 128 → LSB = 2.5 / I.F. = 20-40 ps
  - Timestamp = T_{Coarse} * T_{Clk} - T_{Fine} * LSB
- Measured time interval: (0.5 - 1.5) T_{clk}
- 4 TDCs per pixel for event derandomization

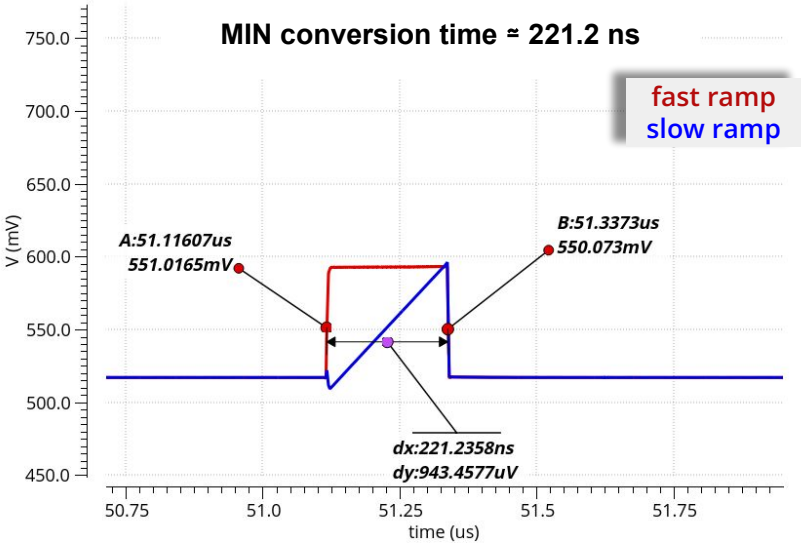
I.F. Interpolation Factor

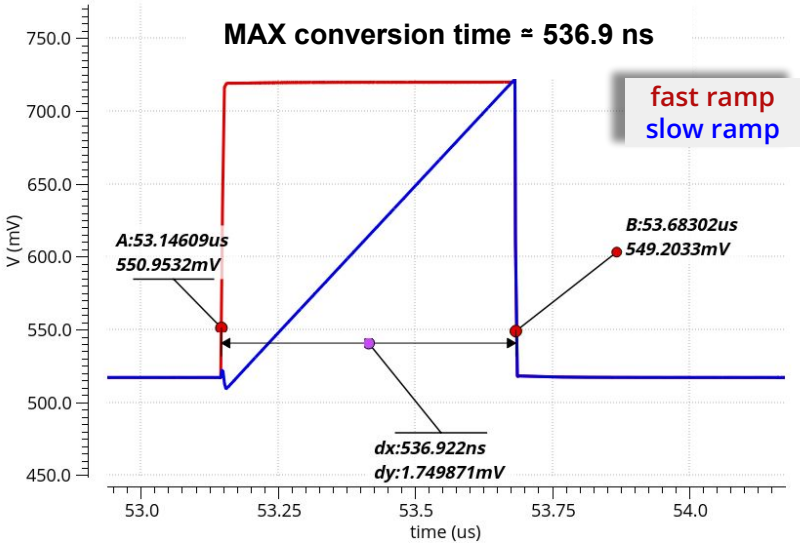




TDC conversion time

- TDC conversion time can vary, according to phase between asynchronous discriminator trigger and clock rising edge
- TDC conversion time range = I.F. · clk period → 64/128 clk cycles



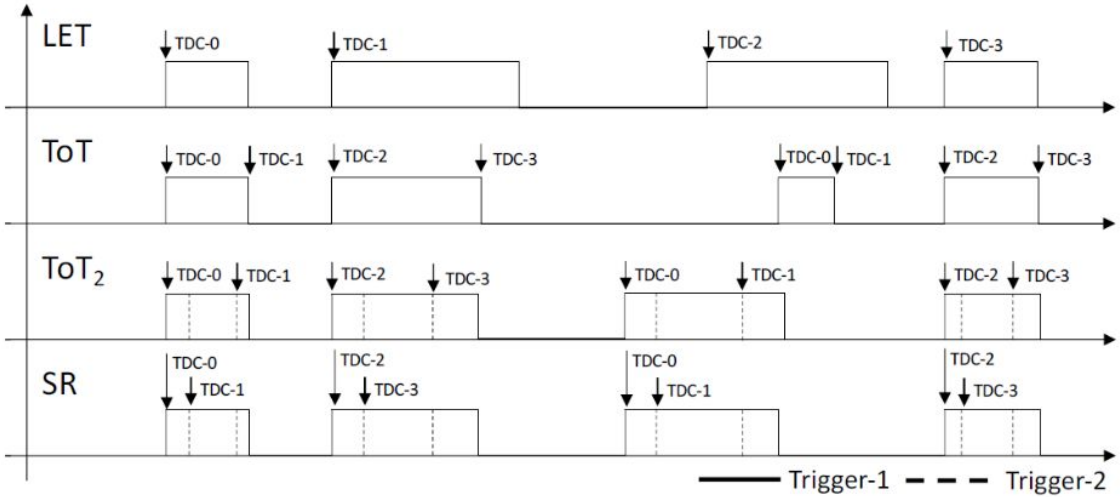


$T_{max} - T_{min}$ = 536.9 ns - 221.2 ns = 315.7 ns → 126 clk cycles

ALCOR output data format

31 29	28 26	25 24	23 9	8 0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter

32 bit event word



4 operation modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

ToT, ToT2, SR:
2x event word per event

Time inverted data: **TFine**

- Simulation in SR mode
  - DCR: 280 kHz/pixel
  - PHY: 0.5 kHz/pixel
- TDC **I.F. = 128**
- Selection of **time-inverted data outputs** → $T_{OA}[i] < T_{OA}[i-1]$
- $T_{fine}[i]$ vs $T_{fine}[i-1]$ for all the events with inversion

T_{coarse} = clk counter (2.5 ns) = coarse ToA

T_{fine} = TDC output = TDC conversion time

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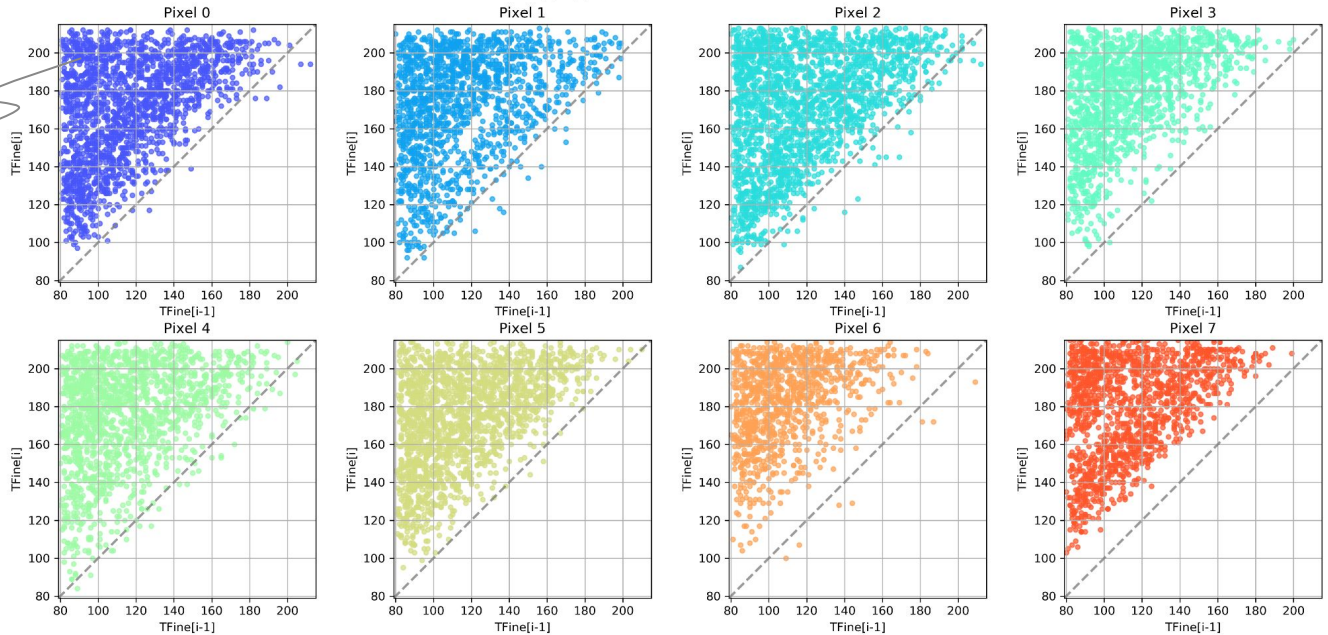
$T_{fine}[i]$ vs $T_{fine}[i-1]$

Almost all points have:
$T_{fine}[i] > T_{fine}[i-1]$

longer conversion time explains time-inverted data outputs

T_{fine} range ~ 128



Time inverted data: TFine

- Simulation in SR mode
  - DCR: 280 kHz/pixel
  - PHY: 0.5 kHz/pixel
- TDC **I.F. = 64**
- Selection of **time-inverted data outputs** → $T_{OA}[i] < T_{OA}[i-1]$
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T_{coarse} = clk counter (2.5 ns) = coarse ToA

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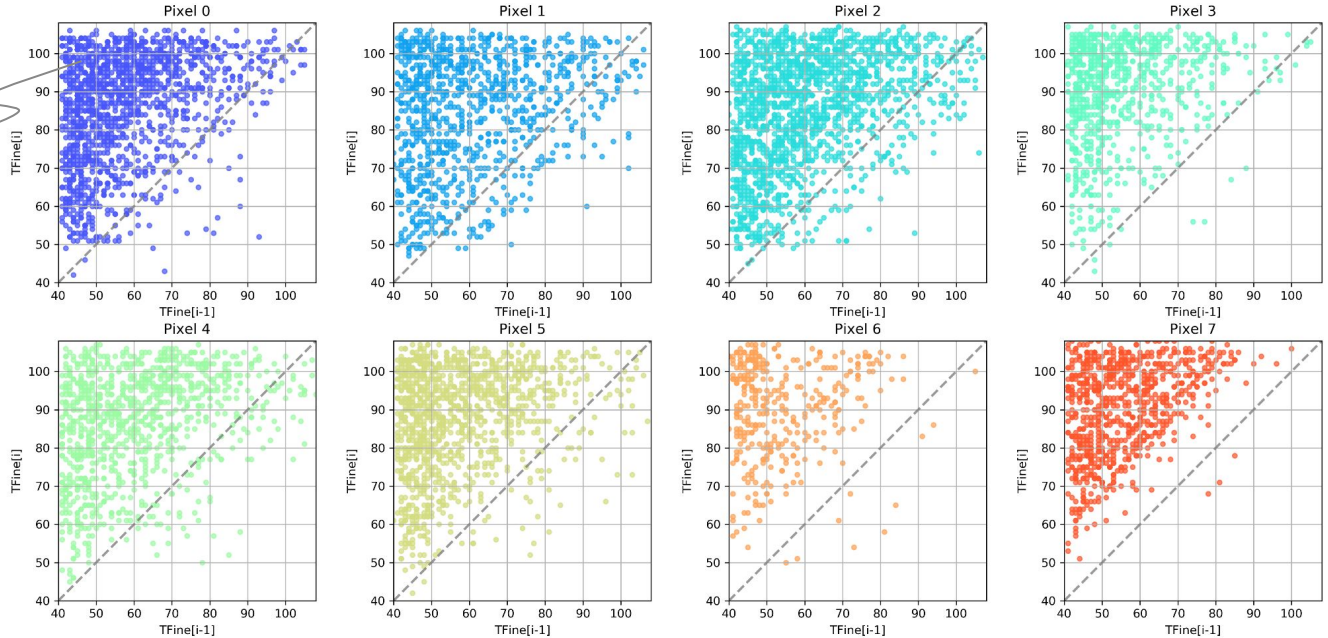
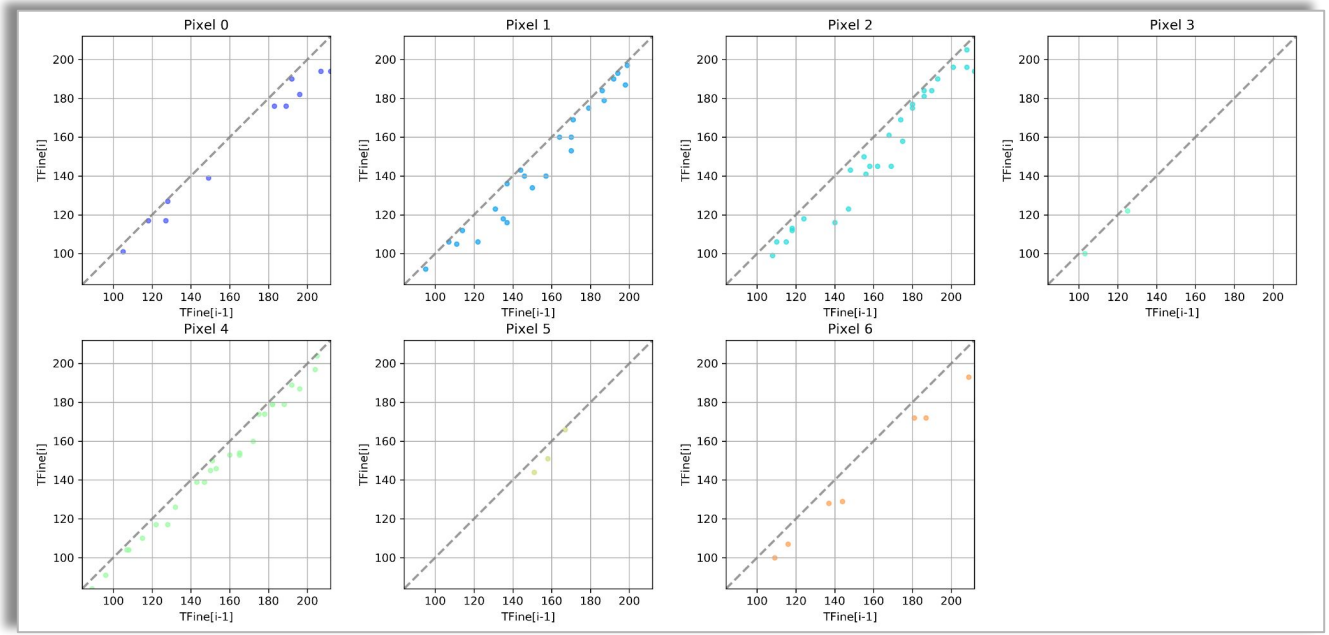
T_{fine} range ~ 64



Time inverted data: **TFine**

- Selection of **time-inverted data outputs** → $T_{OA}[i] < T_{OA}[i-1]$
- $T_{fine}[i]$ vs $T_{fine}[i-1]$ **only for the (rare) events with inversion and $T_{fine}[i] < T_{fine}[i-1]$**



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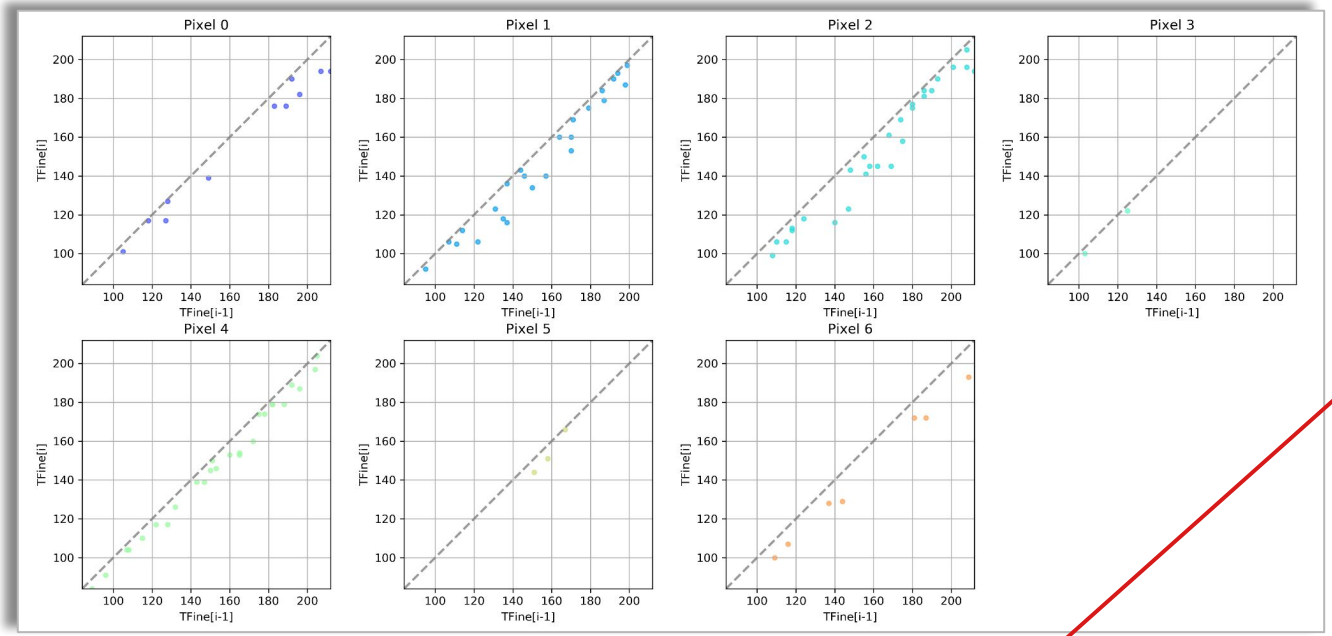
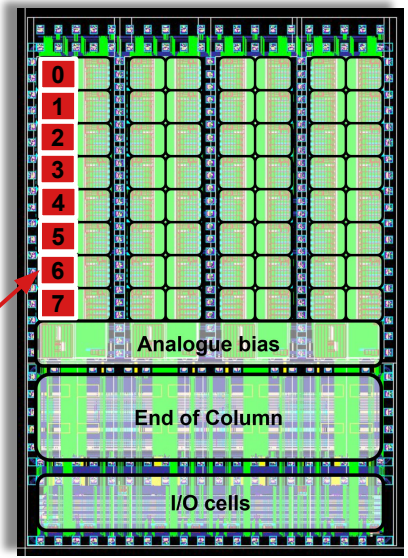




- Inversion can't be explained by the TDC conversion time
- Pixel 0-1-2 have more entries w.r.t. pixel 5-6-7
- This is due to **pixel readout priority** when more than one pixel has one data ready to be transmitted to the EoC

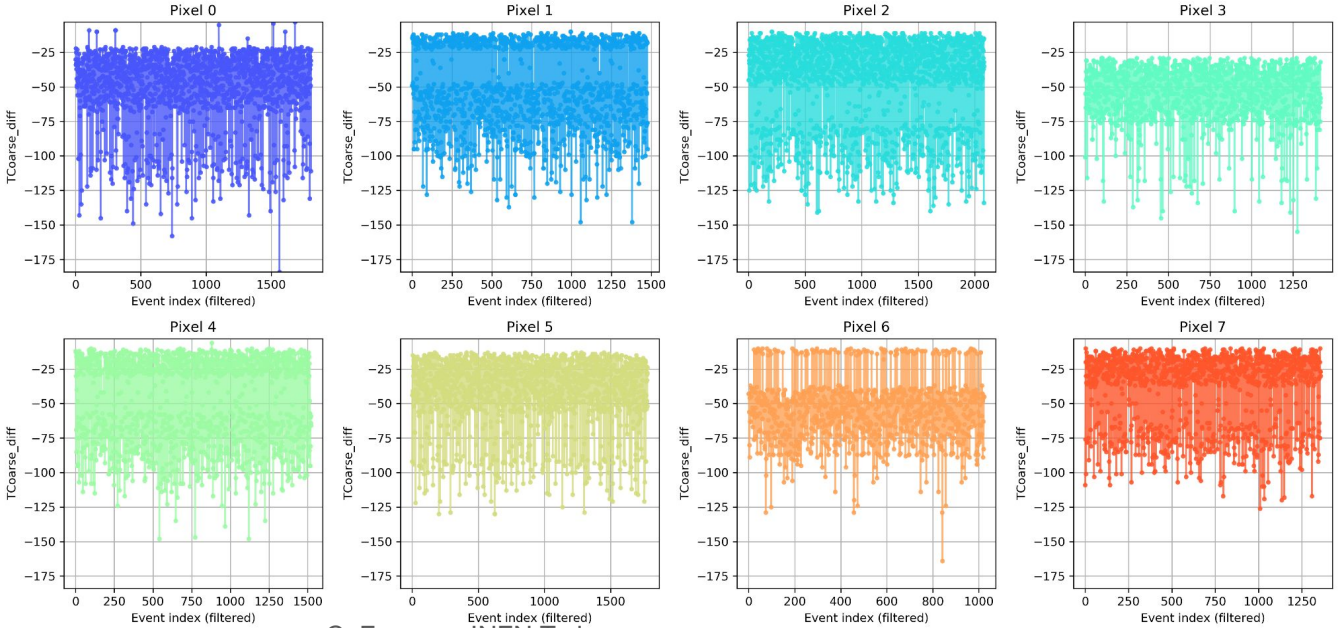
Time inverted data: **TCoarse**

- Simulation in SR mode
  - DCR: 280 kHz/pixel
  - PHY: 0.5 kHz/pixel
- TDC I.F. = 128
- Selection of time-inverted data outputs → $T_{OA}[i] < T_{OA}[i-1]$
- $T_{coarse}[i] - T_{coarse}[i-1]$ for all the events with inversion (all negative)

T_{coarse} = clk counter (2.5 ns) = coarse ToA

T_{fine} = TDC output = TDC conversion time

$T_{Coarse}[i] - T_{Coarse}[i-1]$



$T_{coarse\ diff}$ range ~ 128

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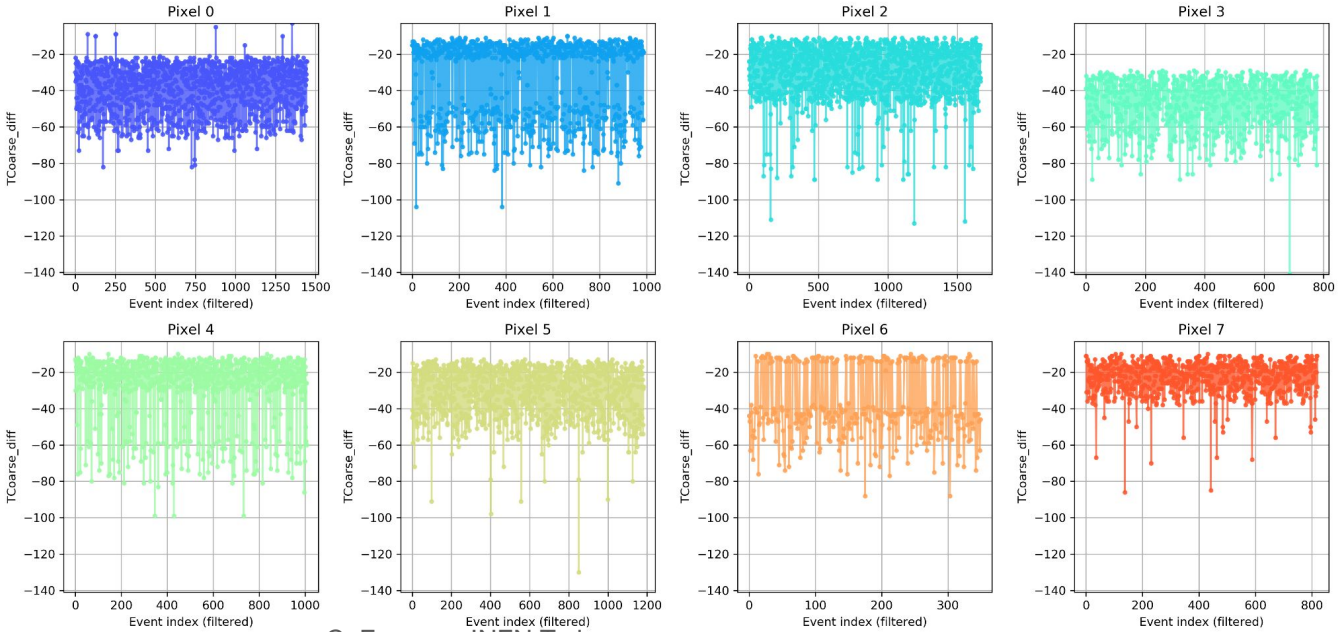
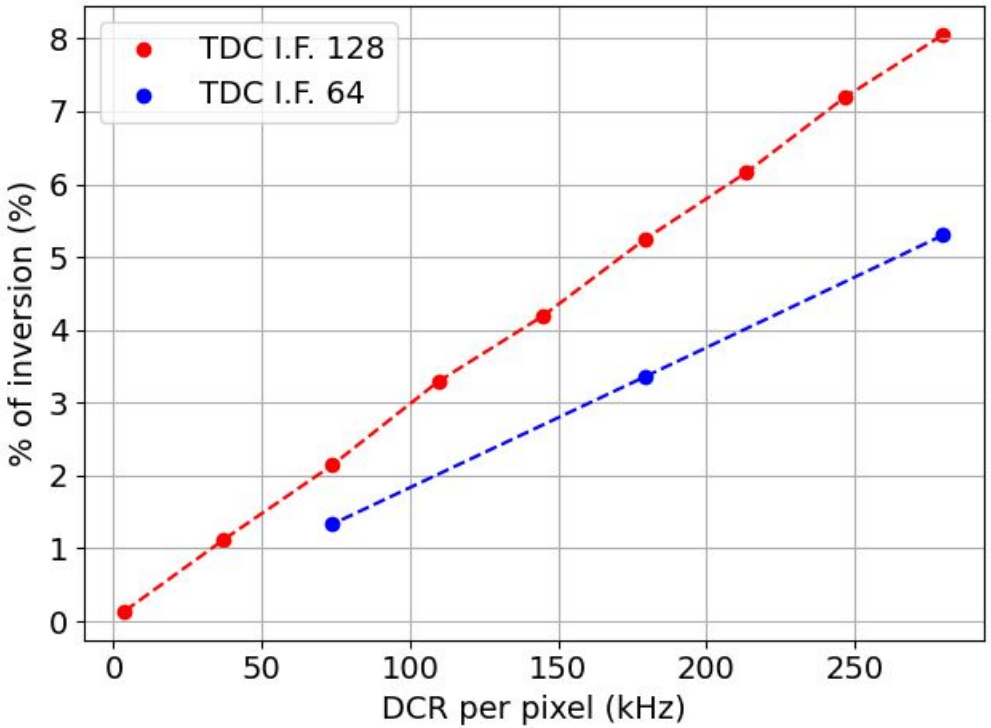


$T_{coarse\ diff}$ range ~ 64

Simulations recap

run name	n. events	PHY rate per column (kHz)	DCR per pixel (kHz)	DCR per column (kHz)	rec. events (per column)	% rec/sim	mode	shutter (ns)	% of ToA diff < 0	I.F.
SR_DC30kHz_PHY3kHz_shutter7.5ns	38708	3,66	3,74	29,9	61945	80,02	SR	7,5	0,14	128
SR_DC300kHz_PHY3kHz_shutter7.5ns	101232	3,66	37,13	297	157794	77,94	SR	7,5	1,12	128
SR_DC600kHz_PHY3kHz_shutter7.5ns	100621	3,66	73,63	589	156301	77,67	SR	7,5	2,14	128
SR_DC900kHz_PHY3kHz_shutter7.5ns	100418	3,66	109,5	876	155855	77,60	SR	7,5	3,29	128
SR_DC1200kHz_PHY3kHz_shutter7.5ns	100316	3,66	144,75	1158	155597	77,55	SR	7,5	4,19	128
SR_DC1500kHz_PHY3kHz_shutter7.5ns	100255	3,66	179,38	1435	155470	77,54	SR	7,5	5,25	128
SR_DC1800kHz_PHY3kHz_shutter7.5ns	100214	3,66	213,38	1707	155295	77,48	SR	7,5	6,16	128
SR_DC2100kHz_PHY3kHz_shutter7.5ns	100185	3,67	246,88	1975	155075	77,39	SR	7,5	7,2	128
SR_DC2400kHz_PHY3kHz_shutter7.5ns	100163	3,66	279,75	2238	155049	77,40	SR	7,5	8,05	128
IF_64/SR_DC2400kHz_PHY3kHz_shutter7.5ns	100163	3,66	279,75	2238	155494	77,62	SR	7,5	5,3	64
IF_64/SR_DC1500kHz_PHY3kHz_shutter7.5ns	100255	3,66	179,38	1435	155653	77,63	SR	7,5	3,36	64
IF_64/SR_DC600kHz_PHY3kHz_shutter7.5ns	100621	3,66	73,63	589	156341	77,69	SR	7,5	1,33	64

Inversion rate vs DCR



- The inversion rate has been quantitatively estimated as the % of events with $T_{OA}[i] < T_{OA}[i-1]$
- It increases linearly with DCR
- Simulations with TDC I.F. 64 show a lower inversion rate
- Shutter width: 7.5 ns

Summary

- **ALCOR data-push architecture** implies that events are not transmitted perfectly ordered by time
  - Data inverted in time mainly due to **TDC conversion time** (128 clk max delay)
  - The inversion rate has been quantitatively estimated to be lower than 10% (I.F. 128)
  - Simulations with TDC I.F. 64 show a lower inversion rate

- Can hits be time ordered by RDO to ease DAM work?
- Can 2 event words (ToT/SR mode) be merged by RDO to reduce data throughput?

see Sandro's talk