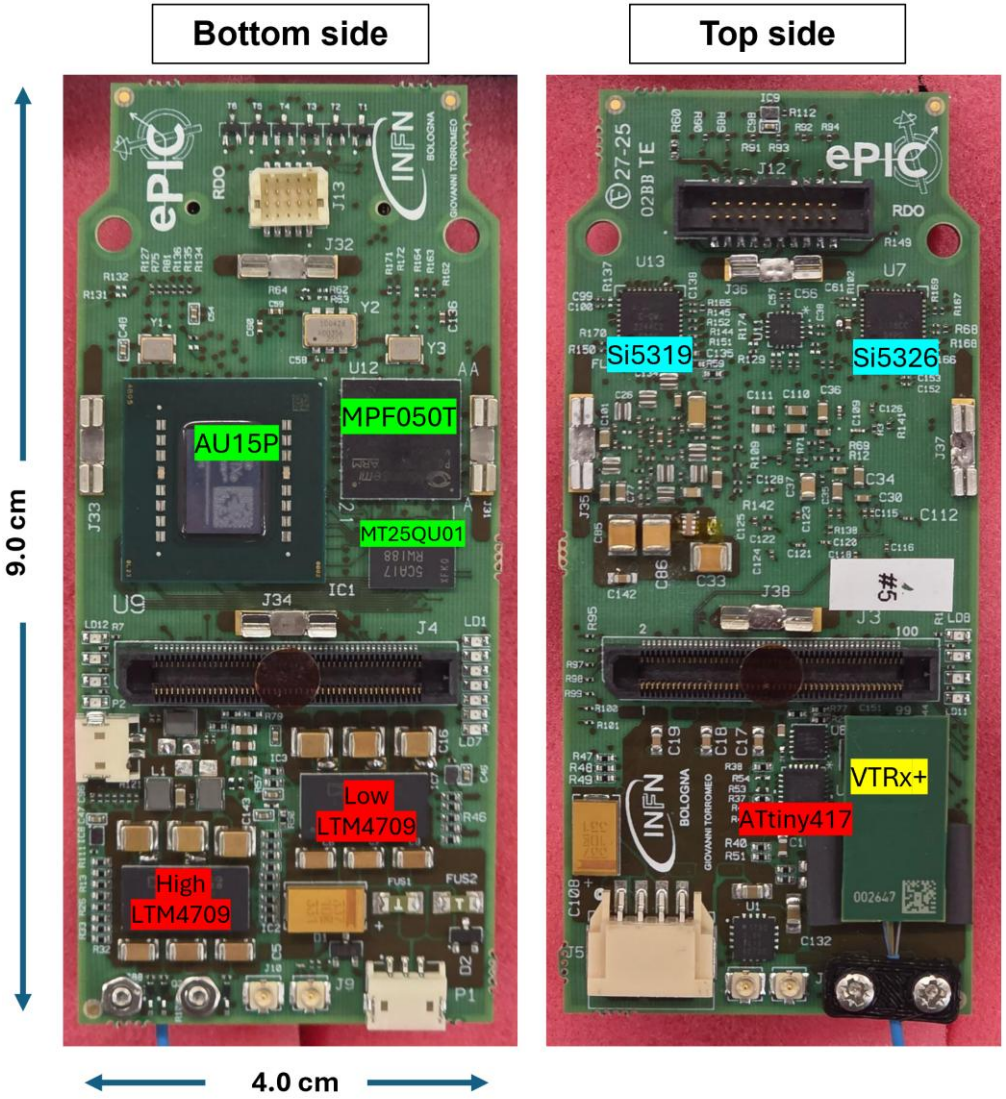
Update on the firmware design for the dRICH-RDO card

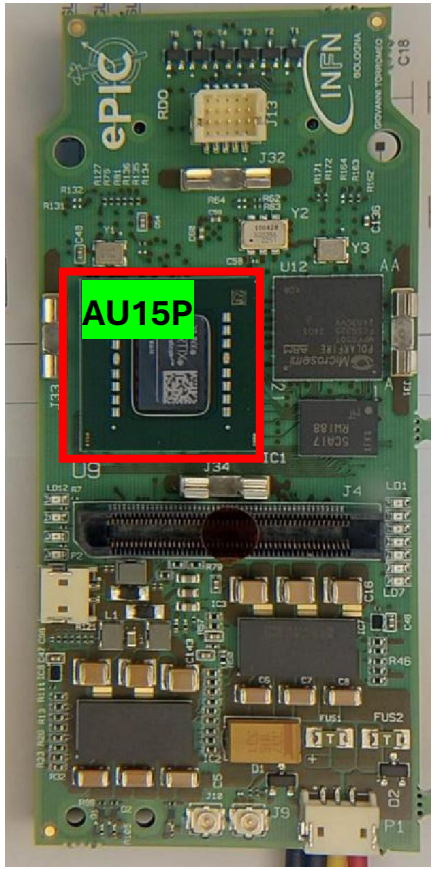
Sandro Geminiani on behalf of ePIC-dRICH DAQ group

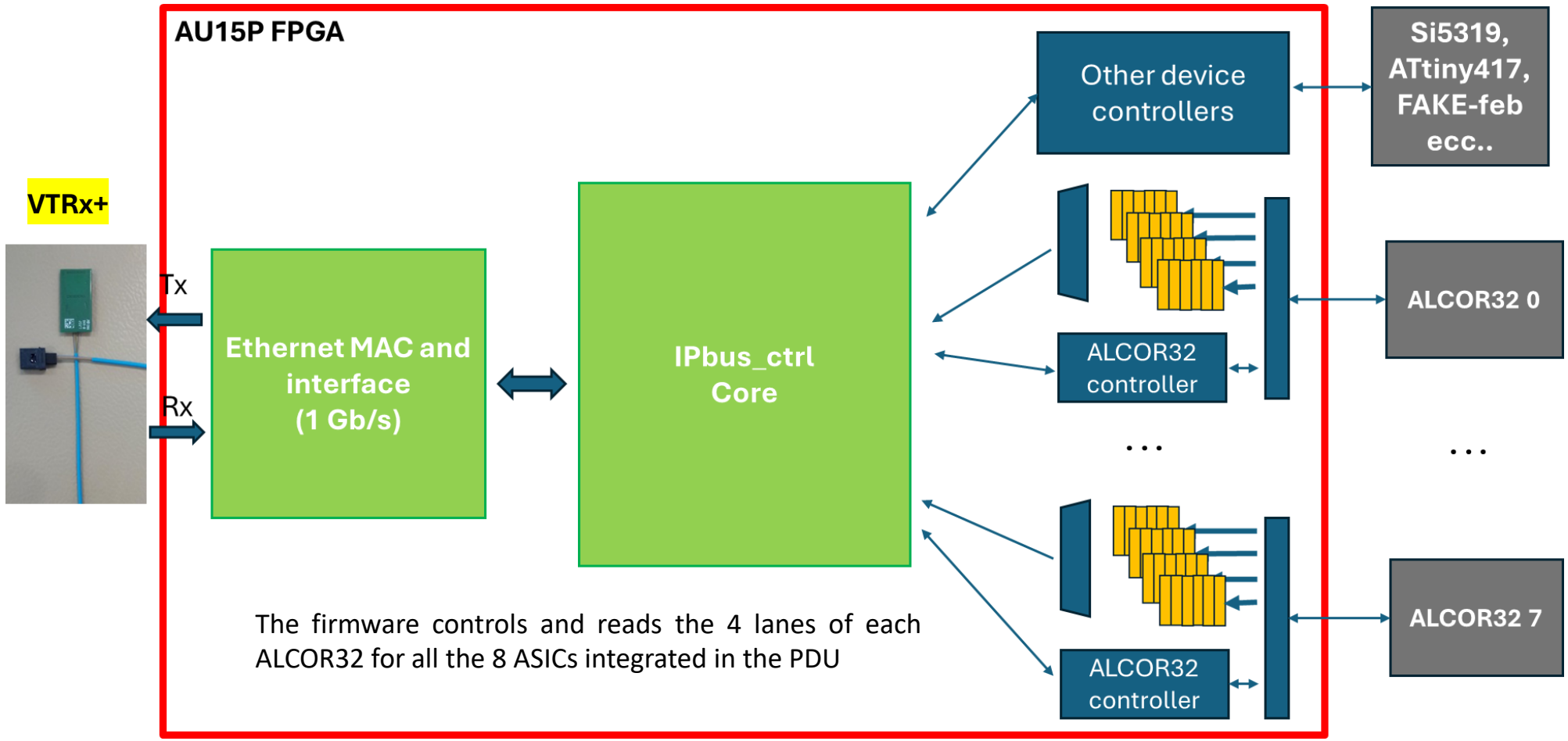
ePIC-dRICH meeting - 25/03/2026



AU15P current firmware design

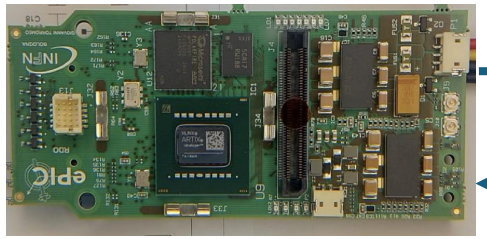
The current firmware is based on IPbus protocol, the AU15P FPGA implements a 1 Gb/s **UDP-IP link** to the Host PC.





RDO-DAM ePIC link

RDO card



Uplink: RDO-to-DAM

Downlink: DAM-to-RDO

DAM board

The link between Front-end and Back-end systems of the ePIC-dRICH DAQ will consider 2 possible flavors:

- **Up:FULL** (9.6 Gb/s) and **Down:GBT** (4.8 Gb/s) protocols
- **lpGBT** protocol (Up: 10.24 Gb/s and Down: 2.56 Gb/s)

Uplink: streaming frames of **256 bits** including data payload and slow control information.

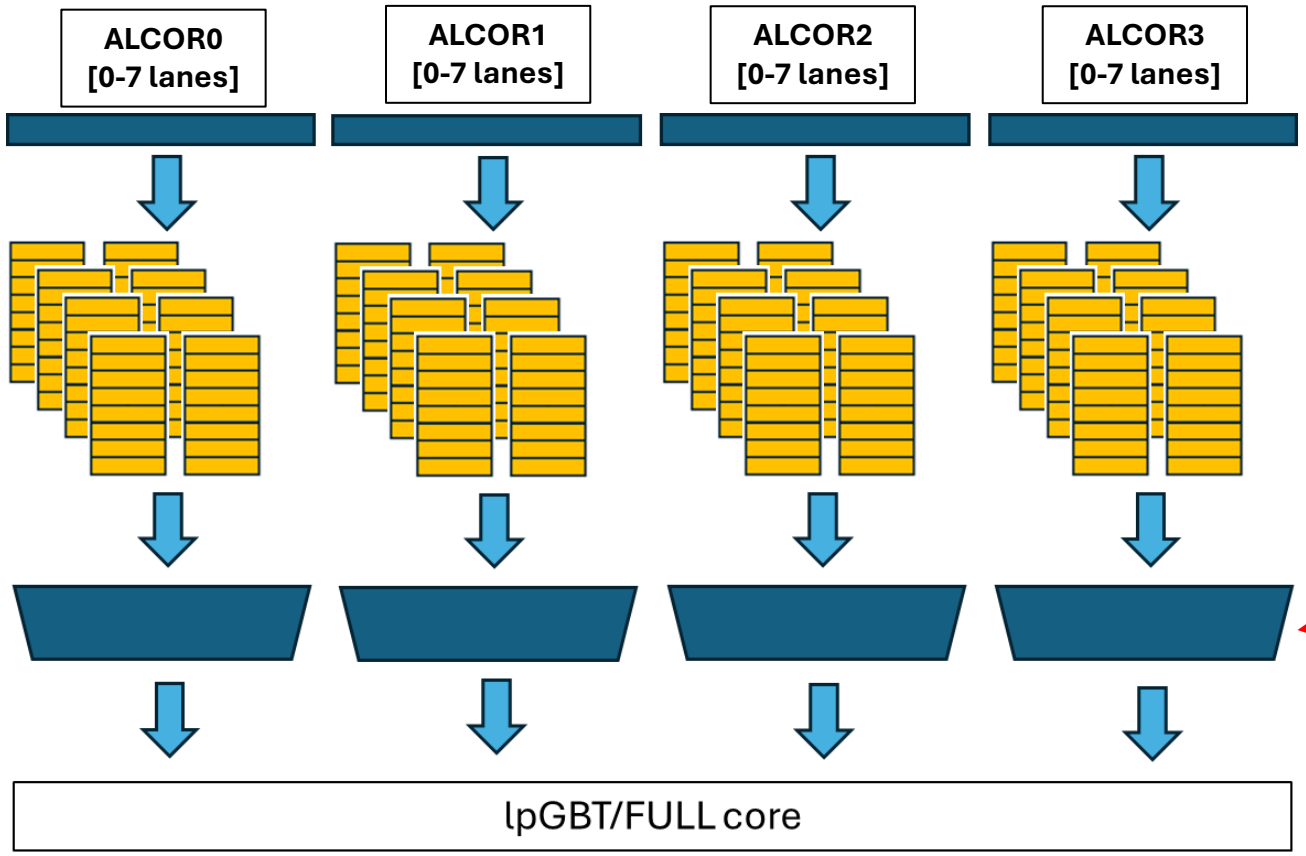
Downlink: streaming frames of **120/64 bits** used to manage front-end configuration and slow control. **The EIC-clock is reconstructed on the RDO from the downlink data.**

How to implement the format in the firmware is still to be defined

Uplink implementation

The current firmware structure would be preserved

Each ALCOR64 lane (8 ch readout) is connected to a buffer!



- The buffer depth is now set to 1024 words (max: 5.1 Mbit of BRAM in the AU15P to buffer data and slow control information).

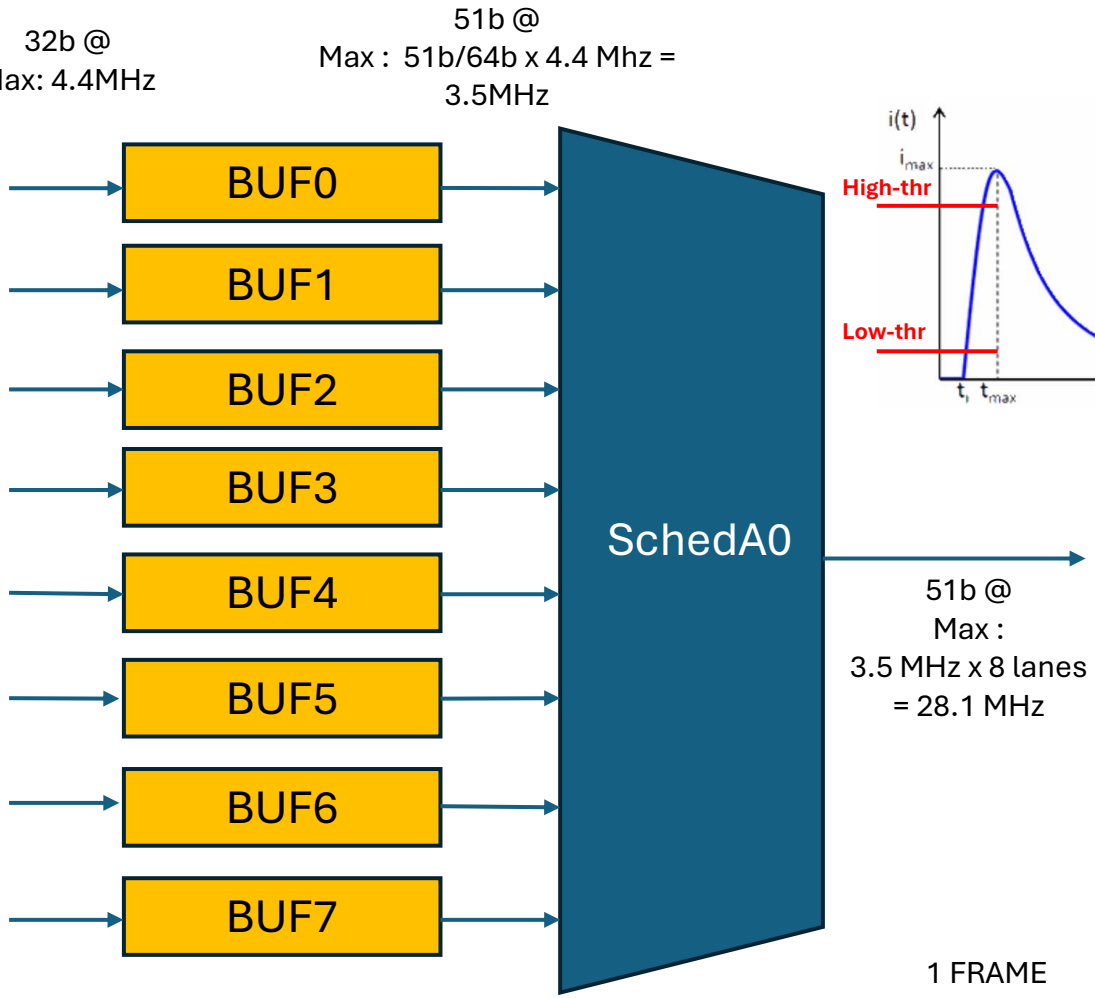
32b word from each ALCOR64 lane

31 29	28 26	25 24	23 9	8 0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter

- Each buffer must provide a specific architecture for **time ordering.**
- **Final scheduler must be designed to interface with the lpGBT/FULL core!**

Scheduler/ALCOR64

ALCOR64 readout



Max data rate per lane (slew rate mode):

300 kHz (DCR) x orbit efficiency (0.92) × 8 (chs) × 2 (32b word per hit) = 4.4 MHz

BUF#:

- Two independent buffers (512 words each) one for low-thr 32b word and the other for high-thr 32b word.
- Coupling of the 2 32b words per channel to generate a 51b ALCOR word:

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

- Lower in time ALCOR word is the first read.
- Protection mechanism for buffer occupancy

SchedA#:

- Choose which lane must be read considering the AWORD lower in time and the occupancy of the BUFs:

						SchedA3		SchedA2		SchedA1		SchedA0
	DF3	DF2	DF1	DF0	DCS (free)	AWORD		AWORD		AWORD		AWORD
FULL	255	254	253	252	251 204	203	153	152	102	101	51	50 0
lpGBT	223	222	221	220	219 204	203	153	152	102	101	51	50 0

dRICH timing calibration

- Each ALCOR channel implements 4 TDCs which must be calibrated, considering the **slew rate mode**.
  - → **Event pulses calibration**
  - → Managed at **RDO level**

→ **8 parameters/channel**

- An offset can be added due to the **path of each channel** to the ALCOR discriminator (PCB traces + ALCOR routing).
  - → **Pulsed laser light calibration**
  - → Managed at **RDO level**

→ **1 parameter/channel**

- **Time-walk effect** due to cross-talk of different channels (correction up to ~800 ps)
  - → **Pulsed laser light calibration**
  - → Still to be discussed

→ **5 parameters/channel**

↓

Total: 3584 parameters/RDO

RDO timing calibration

ALCOR 32 bit word

31 29	28 26	25 24	23 9	8 0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter

The **9 bits of Fine Counter (T_{TDC})** depend on the 4 TDC inside the chip.
Using pulser events it is possible to find a calibration **linear relation** for each of the 4 TDCs:

$$T_{calib} = a \times T_{TDC} + \mathrm{b}$$

For each channel the offset for the **electronics skew** has to be added:

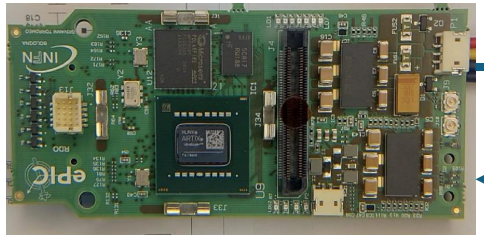
$$T_{total} = T_{calib} + \mathrm{c}$$

All these parameters will be loaded inside the RDO AU15P **and applied to the timestamps before each BUF core**:

Memory: (8 + 1) par x 256 ch x 9 bit = **21 kb**

ALINX+FADE communication

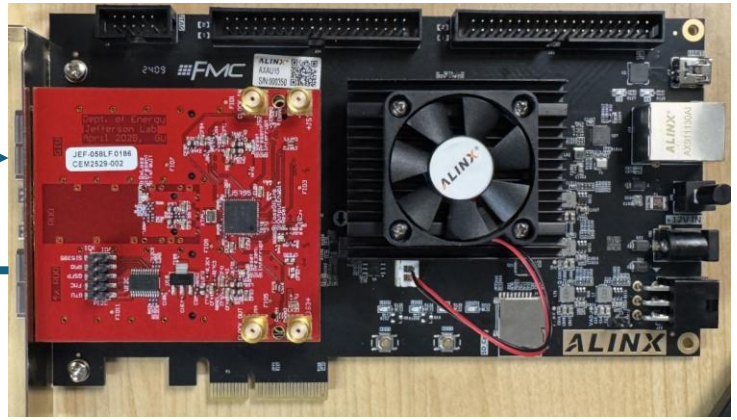
RDO card



Uplink: RDO-to-FADE

Downlink: FADE-to-RDO

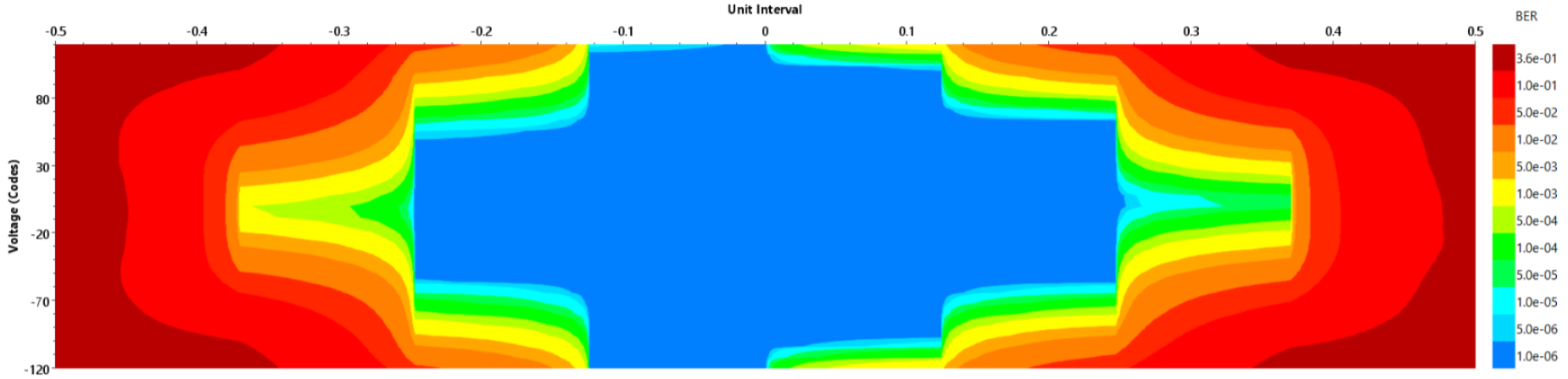
ALINX+FADE card



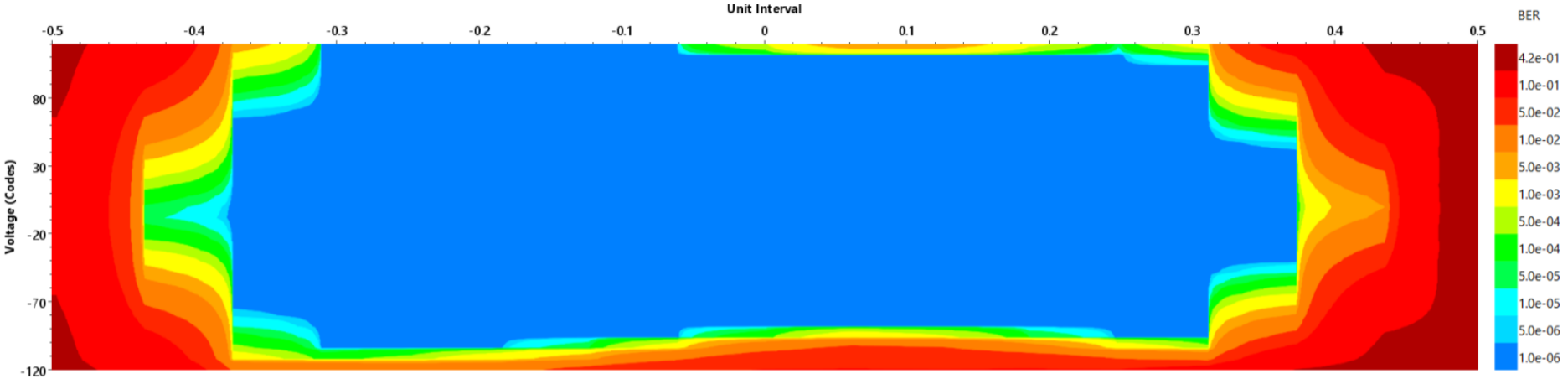
- **ALINX+FADE acts as DAM** communicating to the RDO via an optical fiber.
- Communication between two *In-System IBERT* AMD IP cores (**BER analysis**) to test the hardware:
  «*The IP uses data from the design to plot the eye-scan of the transceivers in real time while they interact with the rest of the system*”
- Progressive configuration of Down/Up link rate up to the **GBT/FULL configuration** (D: 4.8 Gb/s U: 9.6 Gb/s).
- The test proved the RDO **link stability** and was used for **jitter measurements of the reconstructed clock.**

Eye diagrams and BER analysis

ALINX+FADE eye diagram



RDO eye diagram

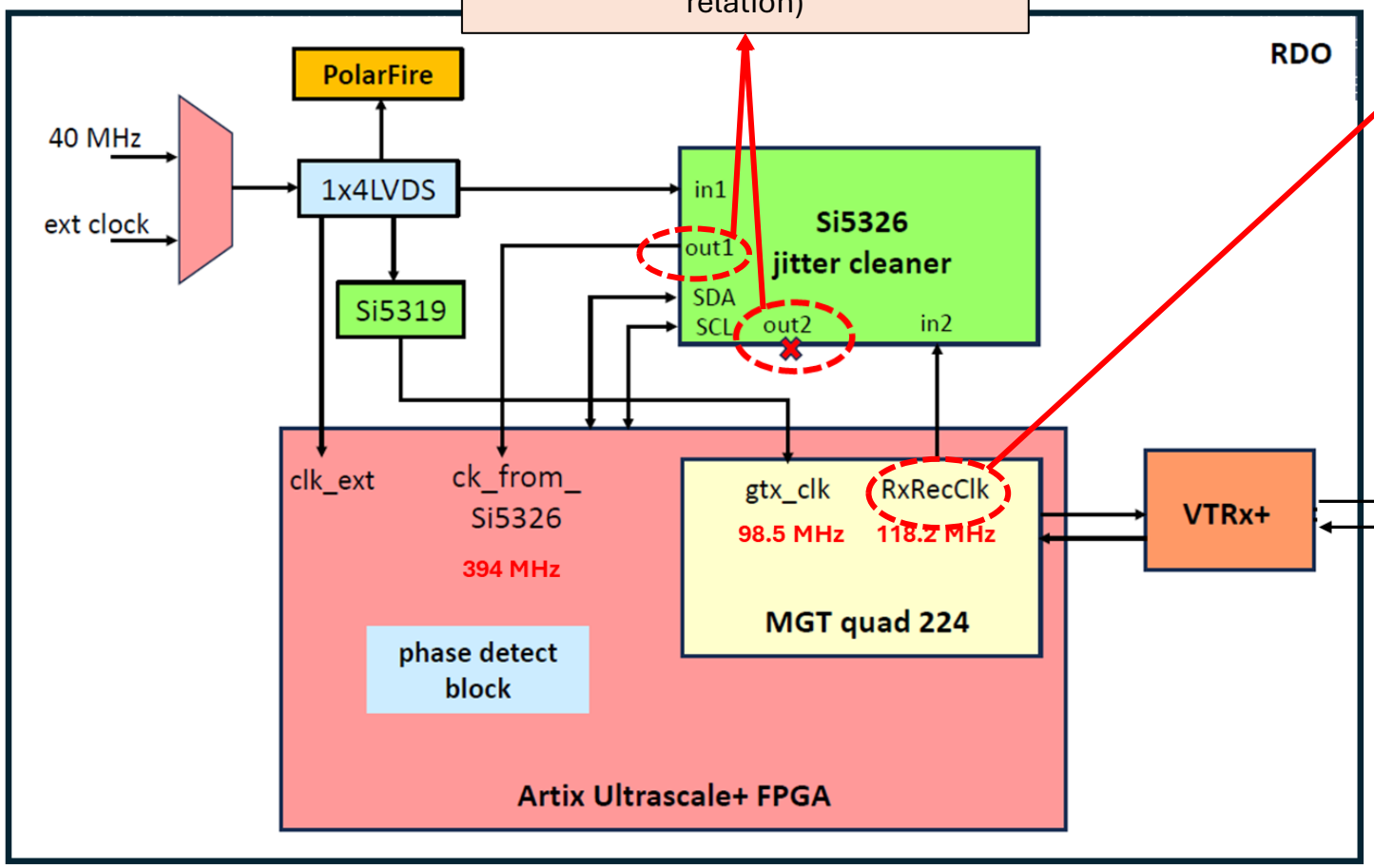


Using a **U:9.5Gb/s – D:4.7 Gb/s** configuration the link was **stable**:

BER << 10^{-6}
(BER would be tested, looking for lower values)

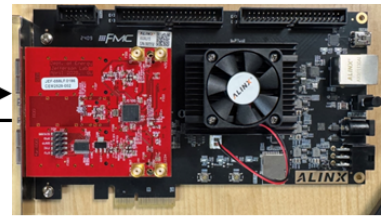
Clock network on the RDO

From out1 (394 MHz) and out2 (39.4 MHz) clocks would be generated, synchronous to the EIC-clock (same frequency and deterministic phase relation)



CDR mechanism: **from data transition** received from VTRx+ lines (1-to-0 or 0-to-1), knowing in advance the protocol, it is possible to **reconstruct a clock with a given frequency and a deterministic phase** respect to transmitter clock.

Jitter and phase measurements of the clocks before and after the jitter cleaner!

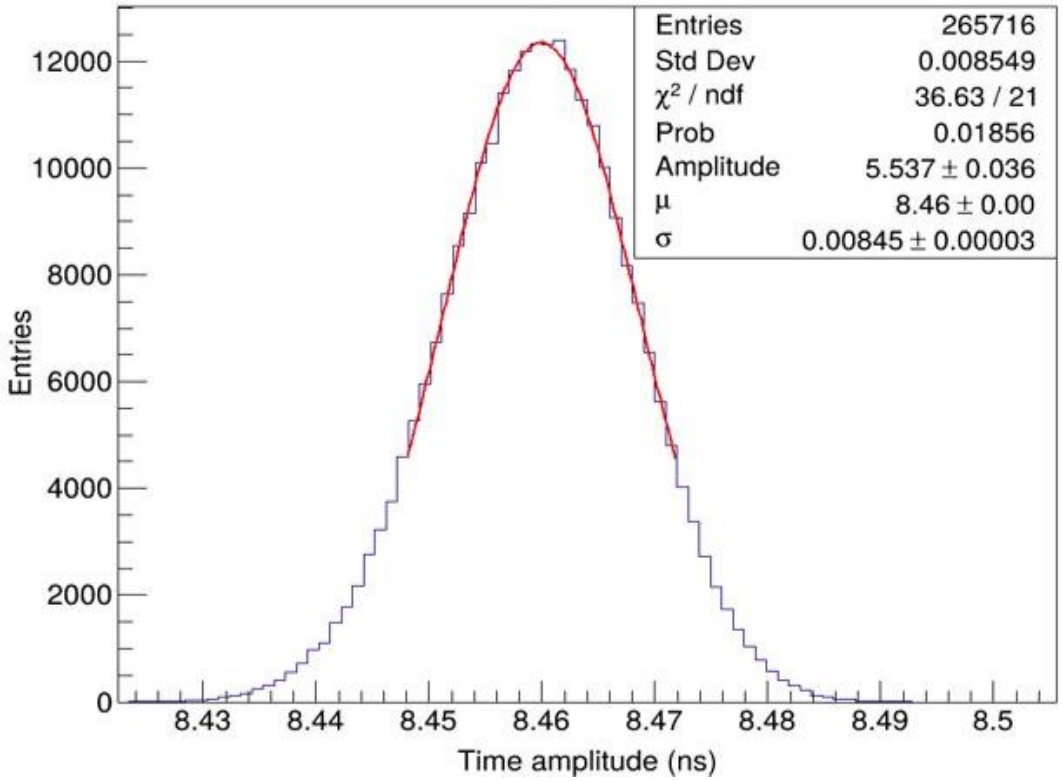


ALINX+FADE card

Period-jitter before the Si5326

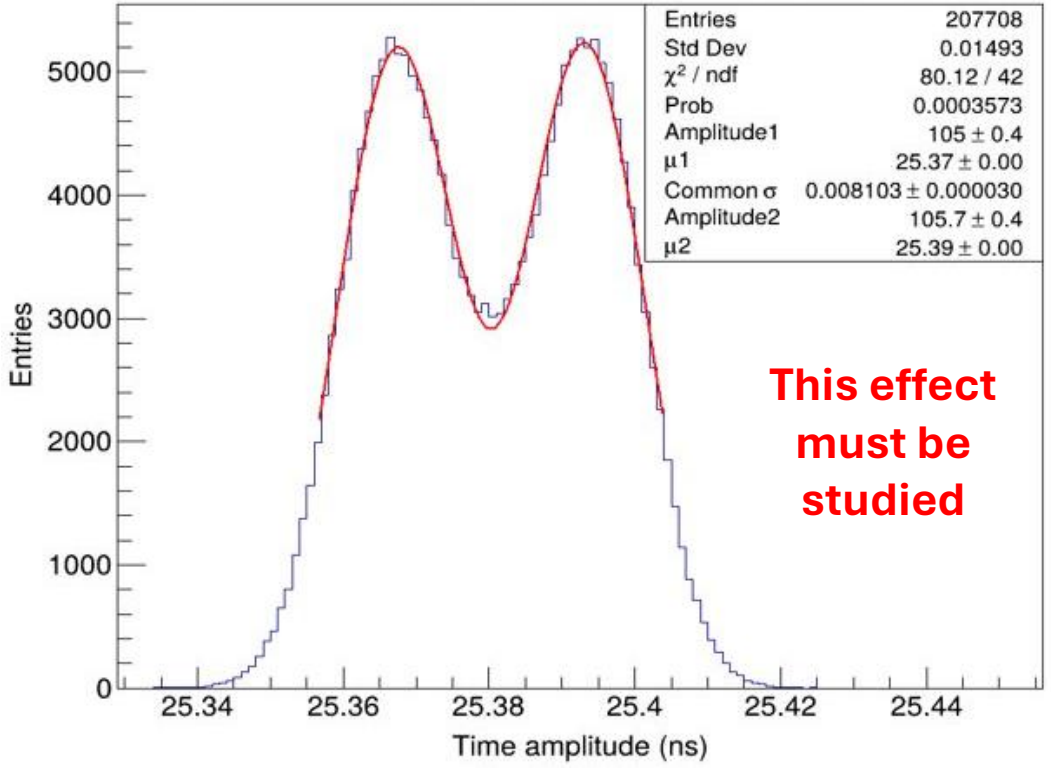
- 40 GS/s
- **118.2 MHz** of RxRecClk (rx: 4.7 Gb/s)
- Gaussian fit
- Period-jitter:

Ran Jitter = 8.45 ± 0.03 (stat.) ps



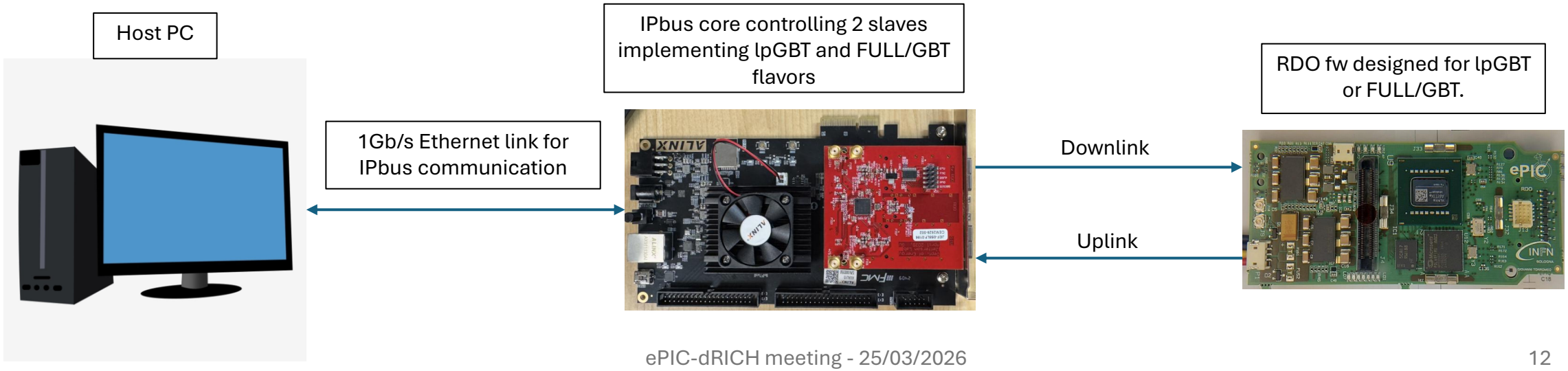
- 40 GS/s
- **39.4 MHz** of RxRecClk (rx: 1.6 Gb/s)
- Double-Dirac fit
- Two jitter components:

Det Jitt = $\mu_2 - \mu_1$ = 25.83 ± 0.09 (stat.) ps
Ran Jitt = σ = 8.10 ± 0.03 (stat.) ps

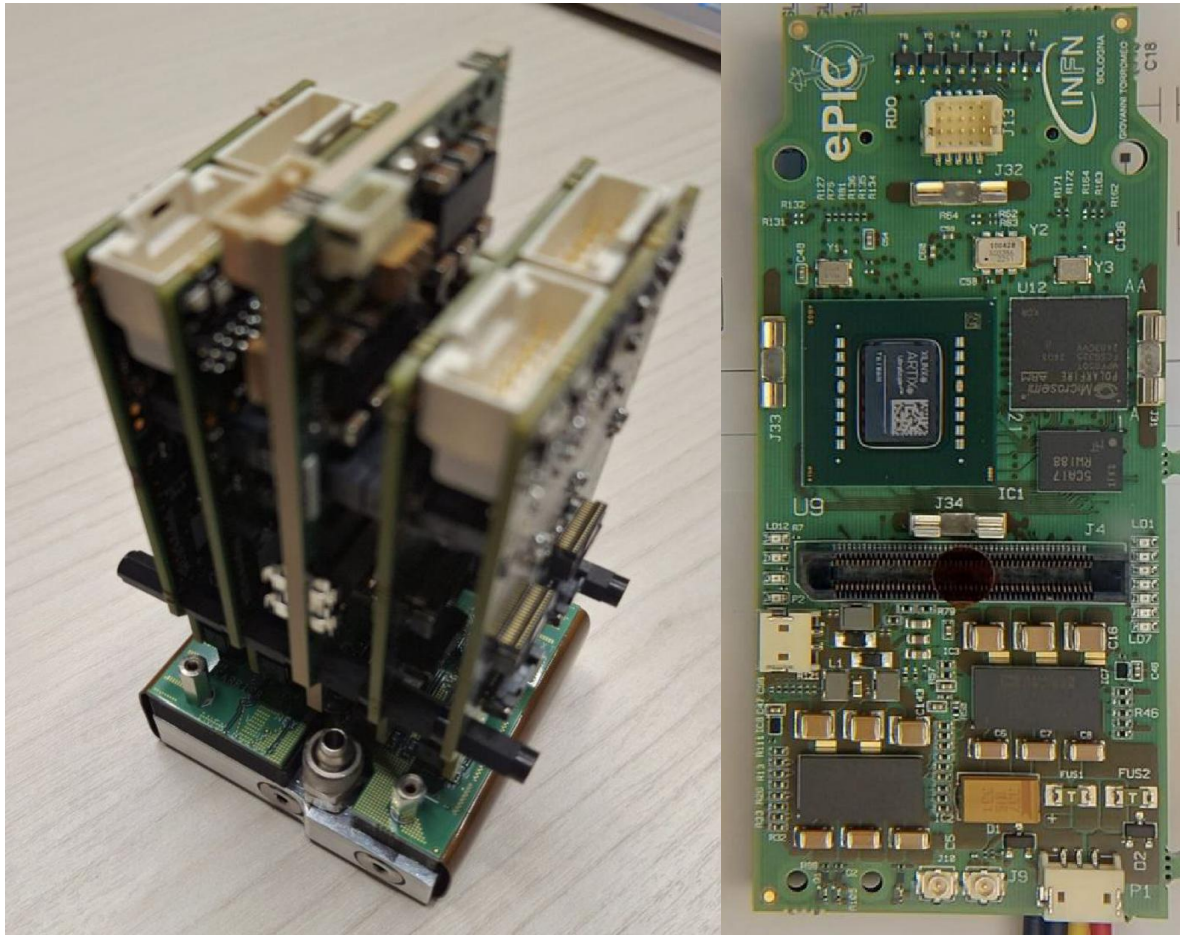


Conclusions and Outlook

1. Uplink format and firmware structure defined → simulation for buffer depth under development
2. Online calibration of the system → Studying the feasibility
3. Downlink format implementation still to be discussed
4. Stable communication of RDO to ALINX+FADE using **U:9.5Gb/s – D:4.7 Gb/s** configuration of the link
5. Jitter measurement of RxRecClk : ~8.5 ps → Future measurement of phase and jitter including jitter cleaner
6. New system setup to test both lpGBT and FULL/GBT flavors:

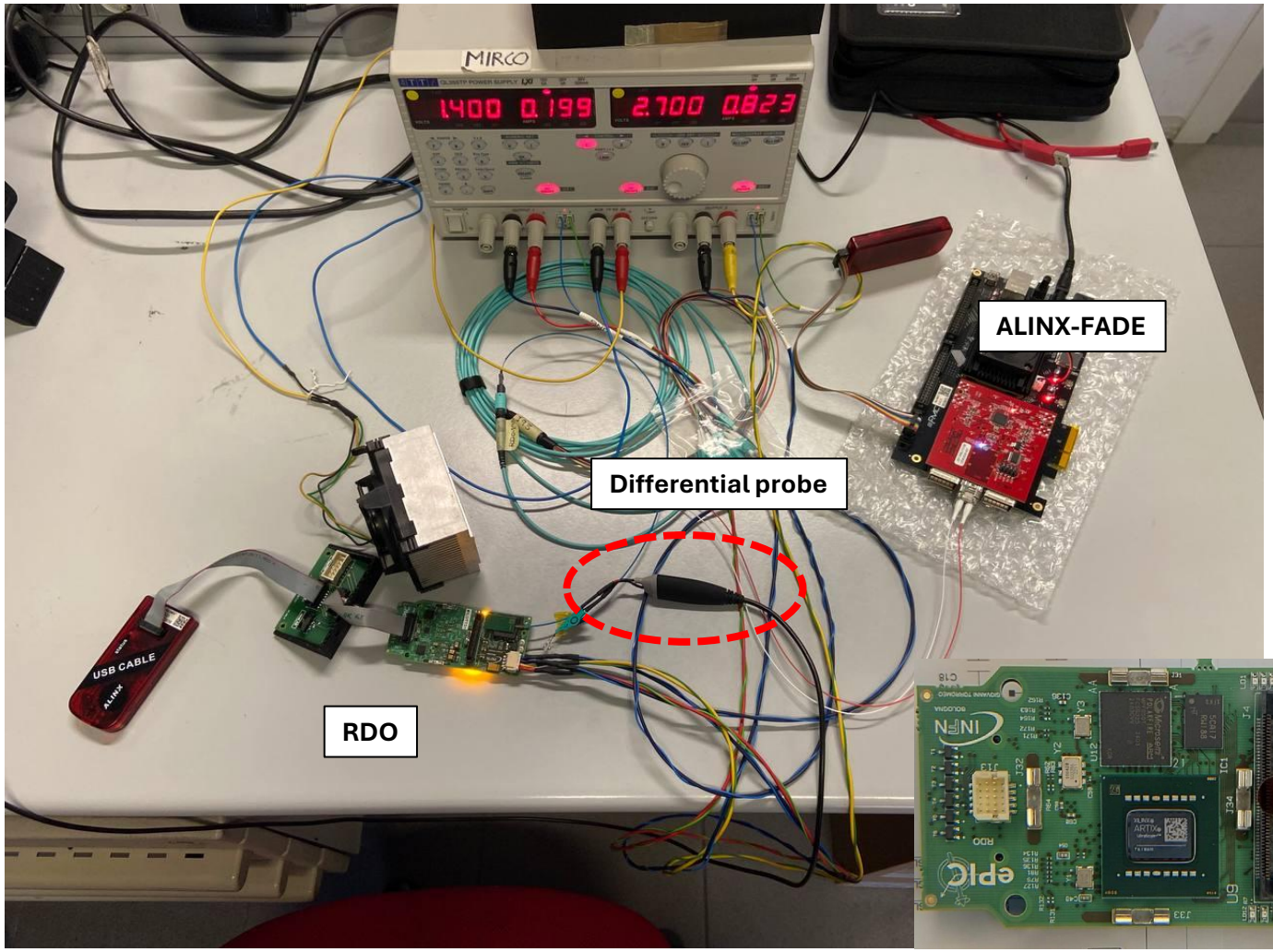


Thank You for the attention!



Backup

Jitter measurement setup



RxRecClk

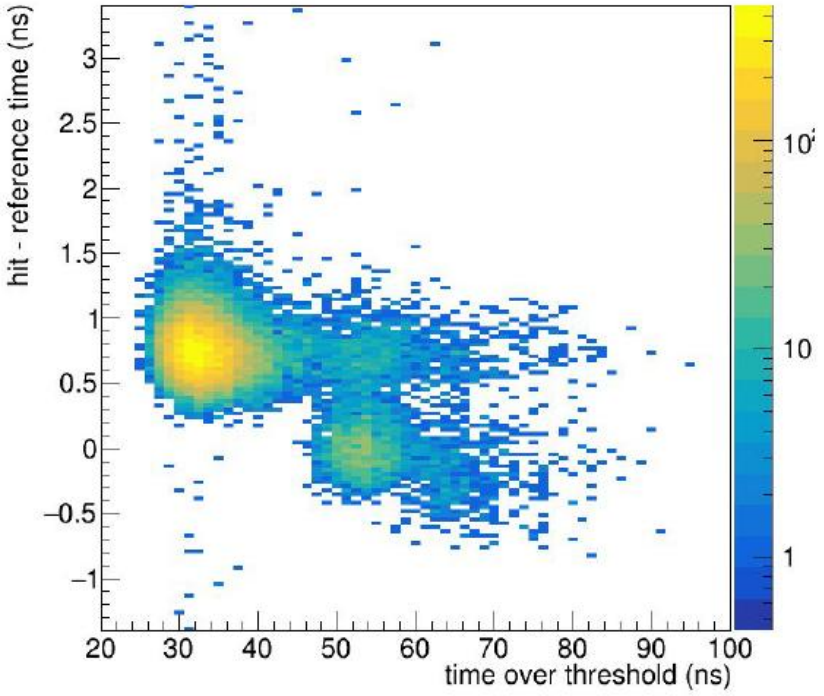
- Optical link between FADE and RDO card:
  Reconstructed clock : 118.2 MHz
- LVCMOS25 clock as output to a scope using a **differential probe.**
- Caveat: the reconstructed clock is not yet sent to the Si5326 jitter cleaner.

Time walk

Slew-rate vs. ToT mode

working with fixed threshold electronics

ALCOR ToT mode



ALCOR slew-rate mode