Fermilab

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Optimization of FCFD for Integration into Detector System

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U.S. DEPARTMENT of ENERGY
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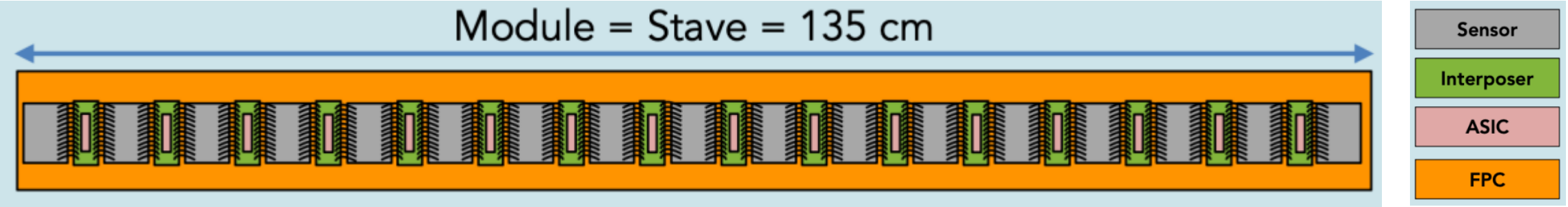
Baseline Detector Concept

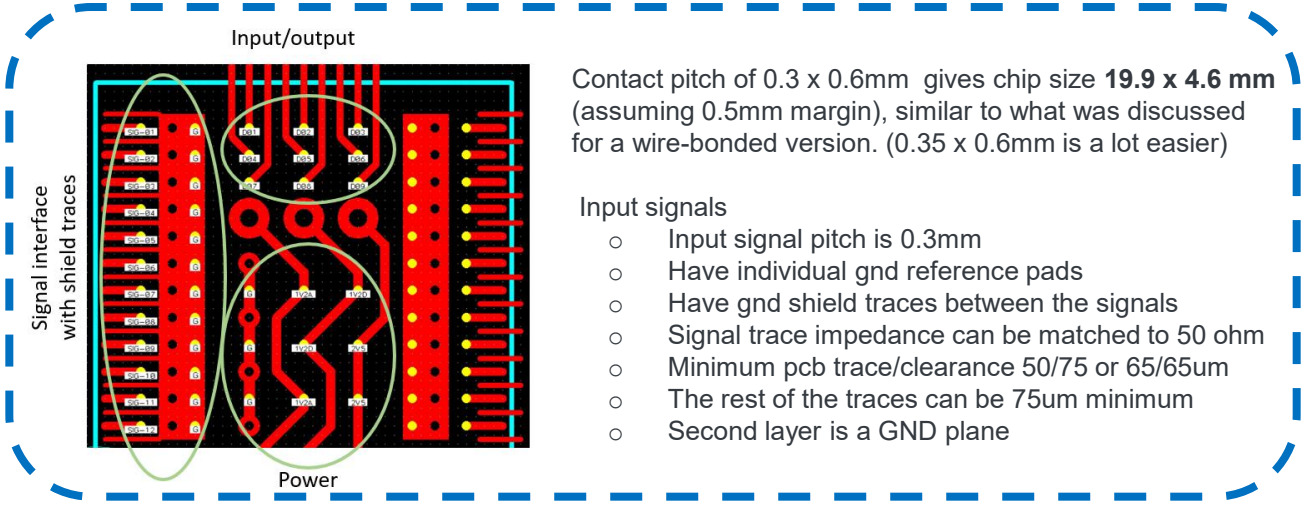


- Sensor
  - Two columns of 10mm-long strips
  - 500um wide strips, x64
  - Effective coverage 20x32mm^2
- ASIC
  - Inputs on left and right
  - 2x64=128 channels
  - Maybe BGA?
- Interposer
  - HDI to fan-in sensor signals
  - Sensor wire-bonded
  - ASIC wire-bonded or flip-chiped
- FPC
  - Power distribution
  - Communication

Assessment of the Original Concept

We considered flip-chip and wire-bonded options for the ASIC

- Both option seemed feasible
- Main concerns
  - HDI parasitics / antennas for sensor signals
  - Heavy fanning-out for direct wire-bonding
  - Potential problems with I/O signal count and ASIC power planning

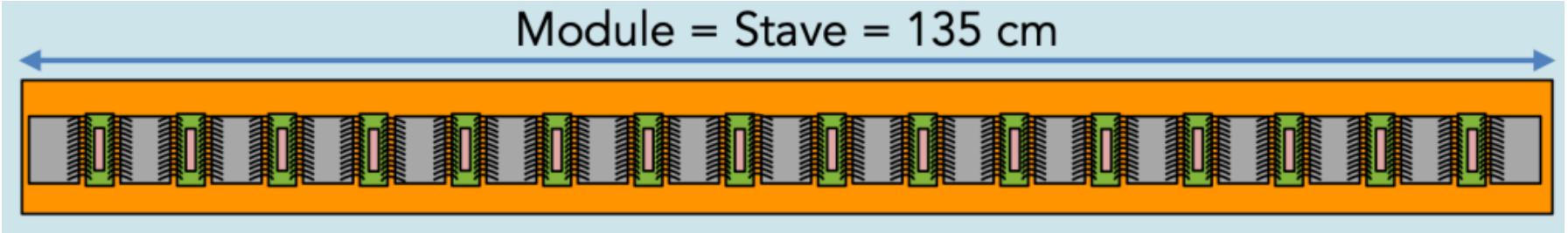


Contact pitch of 0.3 x 0.6mm gives chip size **19.9 x 4.6 mm** (assuming 0.5mm margin), similar to what was discussed for a wire-bonded version. (0.35 x 0.6mm is a lot easier)

Input signals
- Input signal pitch is 0.3mm
- Have individual gnd reference pads
- Have gnd shield traces between the signals
- Signal trace impedance can be matched to 50 ohm
- Minimum pcb trace/clearance 50/75 or 65/65um
- The rest of the traces can be 75um minimum
- Second layer is a GND plane

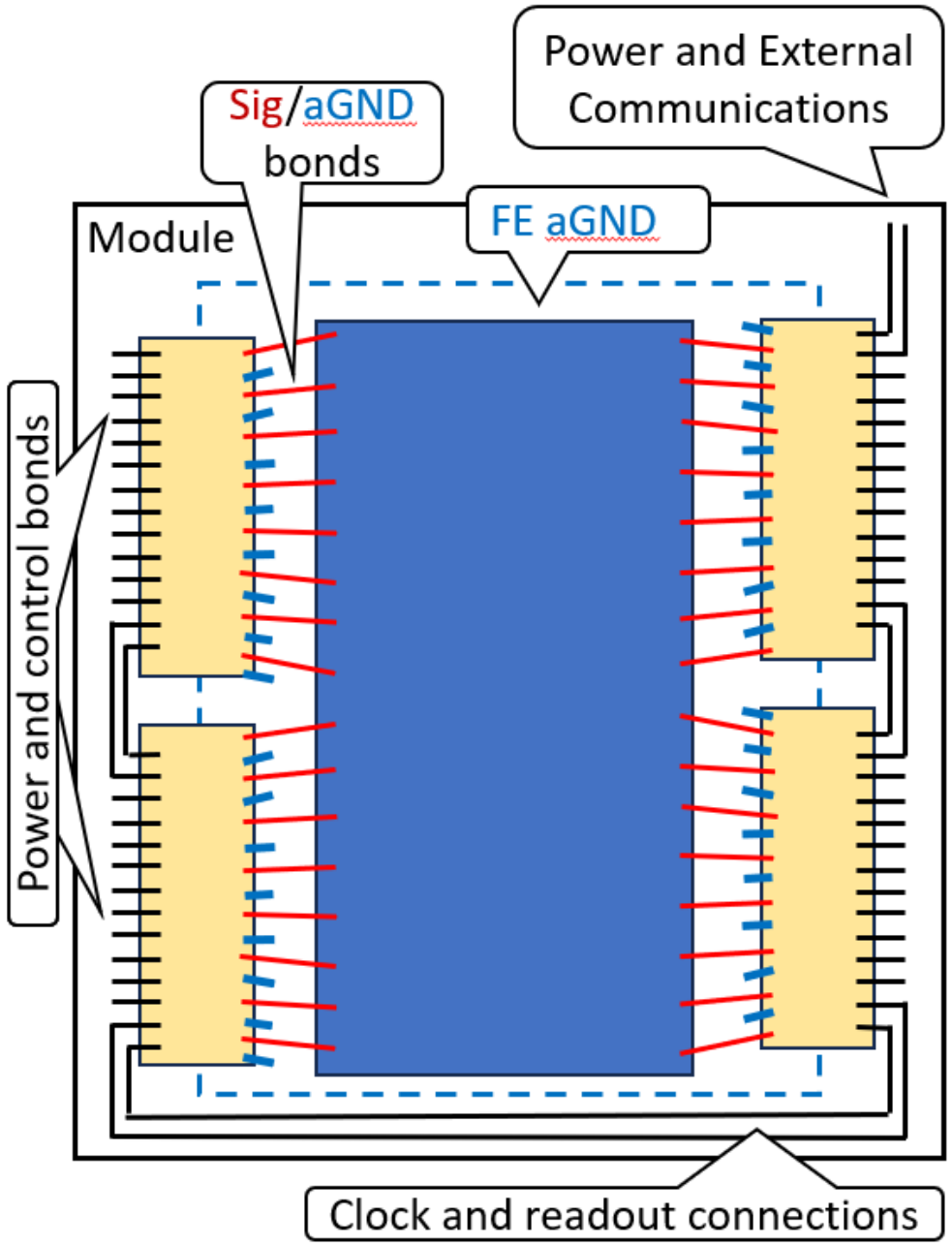
The system issues were realized a bit later

- It's hard to isolate the aGND from the dGND
  - Two haves of the sensor share same aGND (while connected to different ASICs)
  - ASIC should have two separate sets of aGND/aPWR
  - Mounting Sensors on a Flex is risky
- The whole stave is the minimal assembly unit
  - Assembly is difficult
  - Wire-bonding is difficult
  - Repairs are difficult
  - Testing is difficult



One-sided ASIC Design

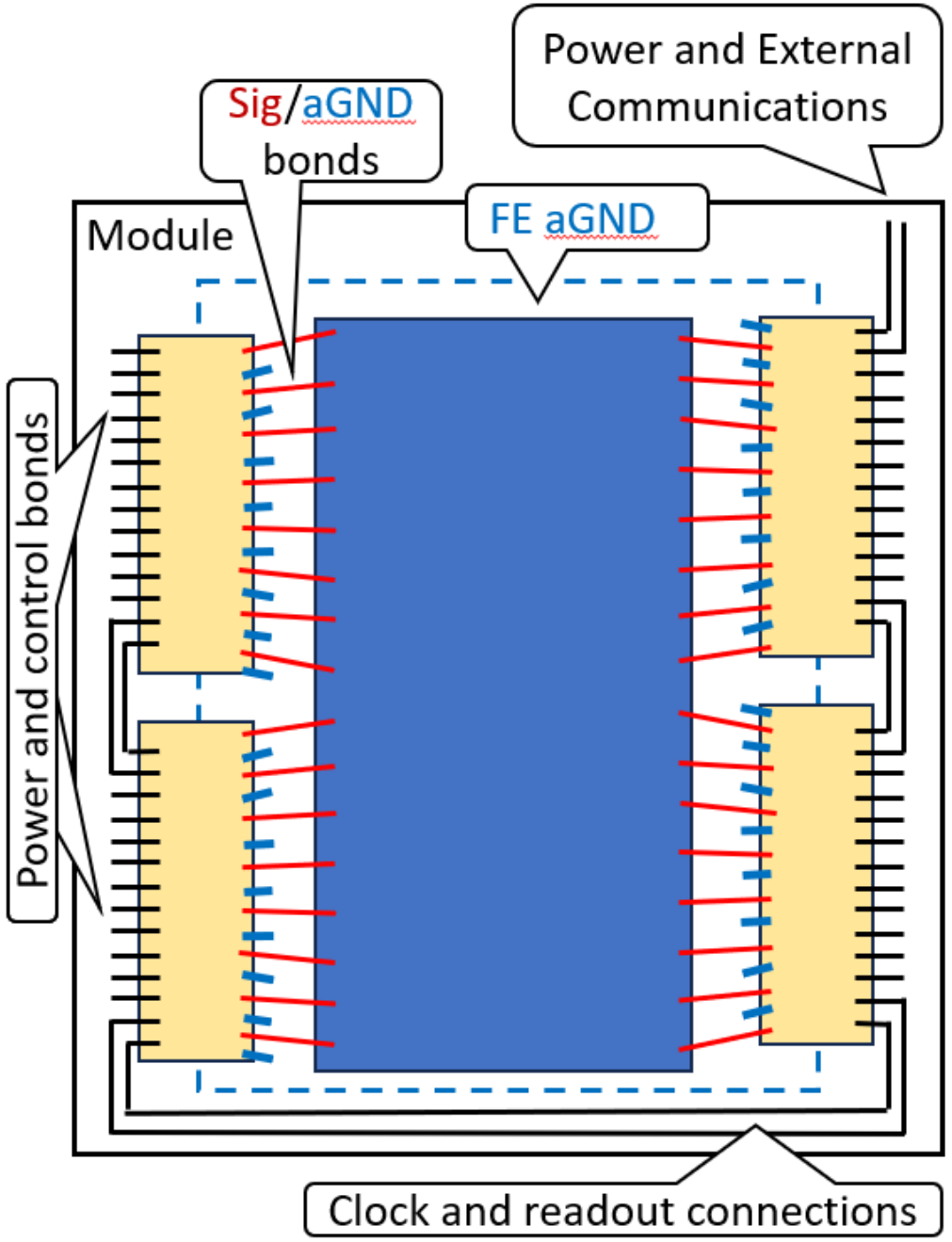
- **Each sensor has dedicated readout ASICs**
  - Simple modules for testing
  - Easy aGND/dGND separation
  - Plenty of real estate for i/o and power
  - No need for half-sensors
- **32-channel ASIC selected**
  - Practical chip size and aspect ratio 14-15 by 2-3 mm
  - Direct wire-bonding to the sensor
  - Channel pitch is slightly less than that of the Sensor (0.5mm) so to butt two chips along the Sensor, allowing for a small gap between them. That will cause some fanning of the signal wire-bonds, but not significantly affecting bond length
  - Reasonable fan-out angles (1mm shift for 3-4mm long bonds)
  - All 4 ASICs are connected in a single readout chain



Stand-alone Module

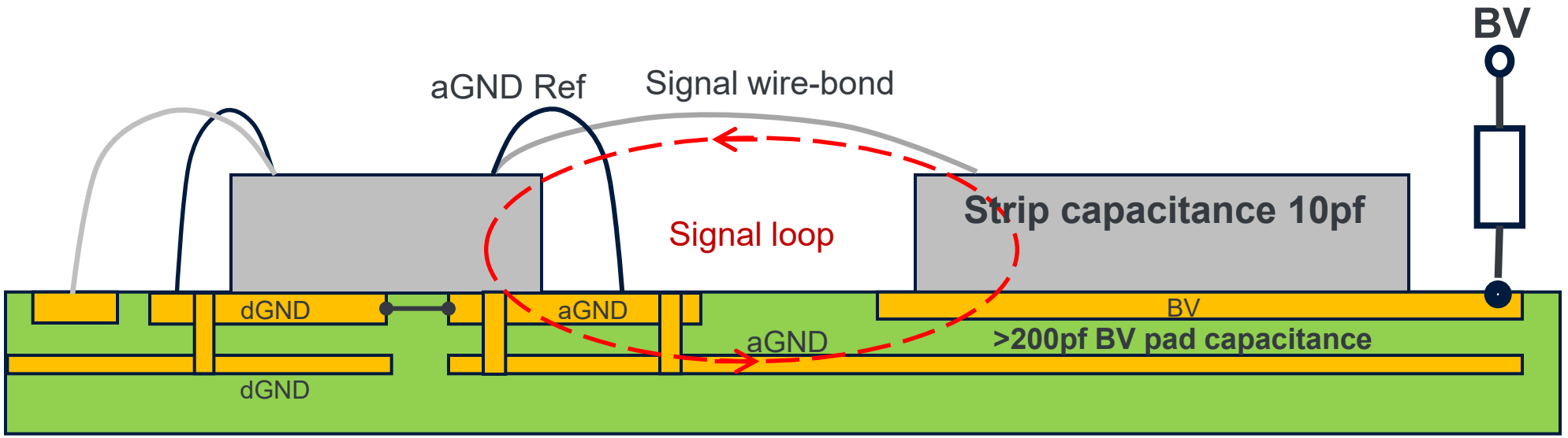
- **Benefits**
  - Direct wire-bonding between the Sensor and FCFD
  - Smaller chip, higher yield
  - Ample real estate for power and control signals
  - Local analog ground improves ground loop immunity
  - Easy to combine multiple modules in a single assembly
  - No need to have half-size sensors
- **Things to watch**
  - Module width <40mm to allow for full coverage in two layers
  - That is about 9.5mm for FCFD on each side:
    - Chip 3mm
    - Sensor-ASIC gap 2-3mm
    - Back-side bonds 1mm
    - Extra routing area 2mm
    - pcb edge clearance 0.5mm

    - **Total** **8.5-9.5mm**



Bias Voltage and Signal Return

- **Minimizing Signal Loop**
  - Sensor is mounted on a pcb BV pad
  - FE part of the ASIC is over a pcb aGND pad
  - aGND Ref pads are directly bonded to the pcb aGND pad
  - Second layer copper connects the ASIC aGND to the BV pad using inter-layer capacitance
  - Such layout provides the minimum impedance signal return path



FCFD Power
(last moment addition)

- **There are two power voltages being planned so far**
  - 2.5V for the PreAmp
  - 1.2V for the FE / TDC / Digital / IO

  - Common 1.2V source can be used for all 1.2V destinations
  - There are independent 1.2V pads (multiple) for each destination
  - It should be possible to sufficiently bypass and decouple the 1.2V destinations using an appropriate pcb layout