Inner MPGD CyMBaL Status

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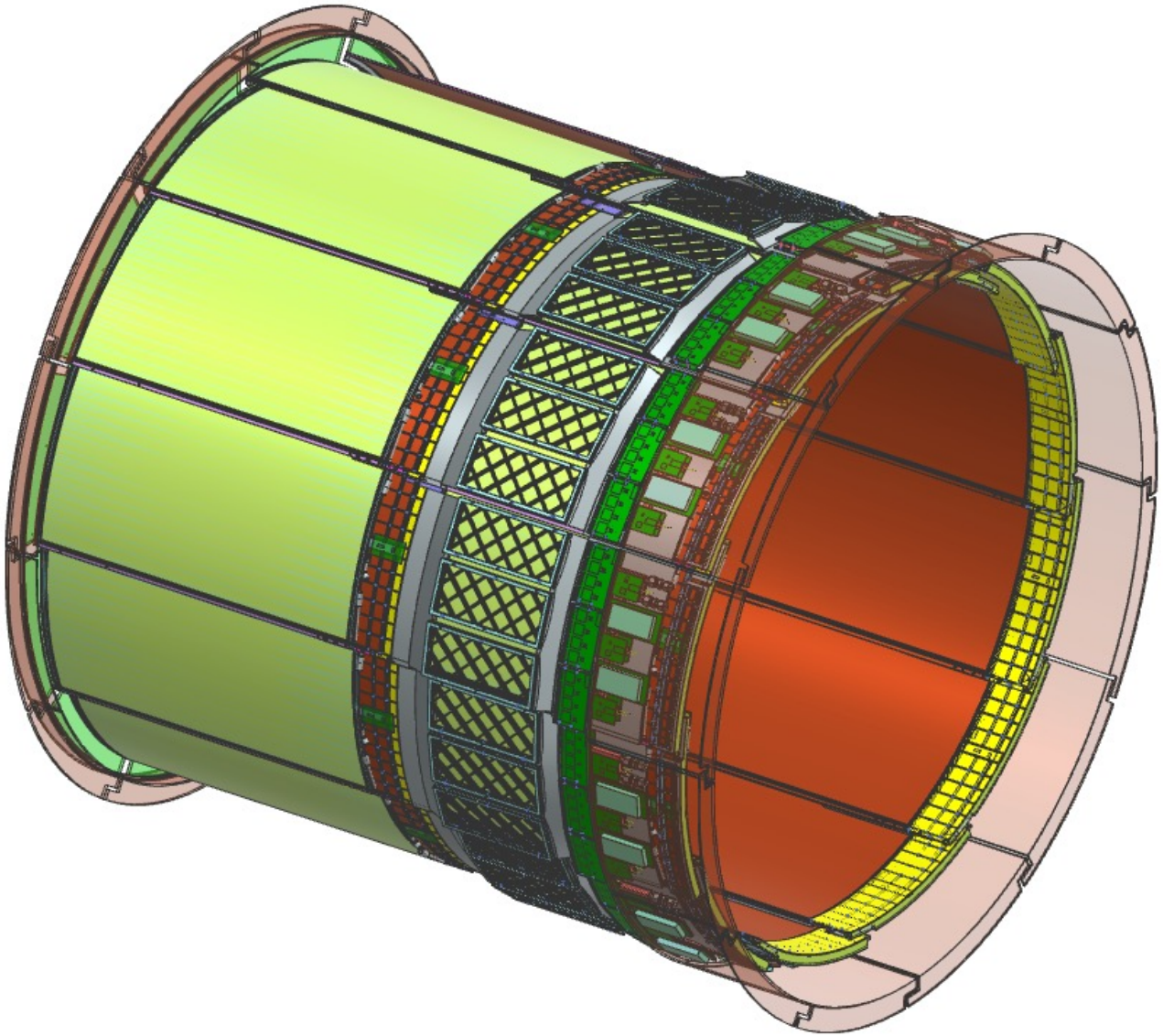
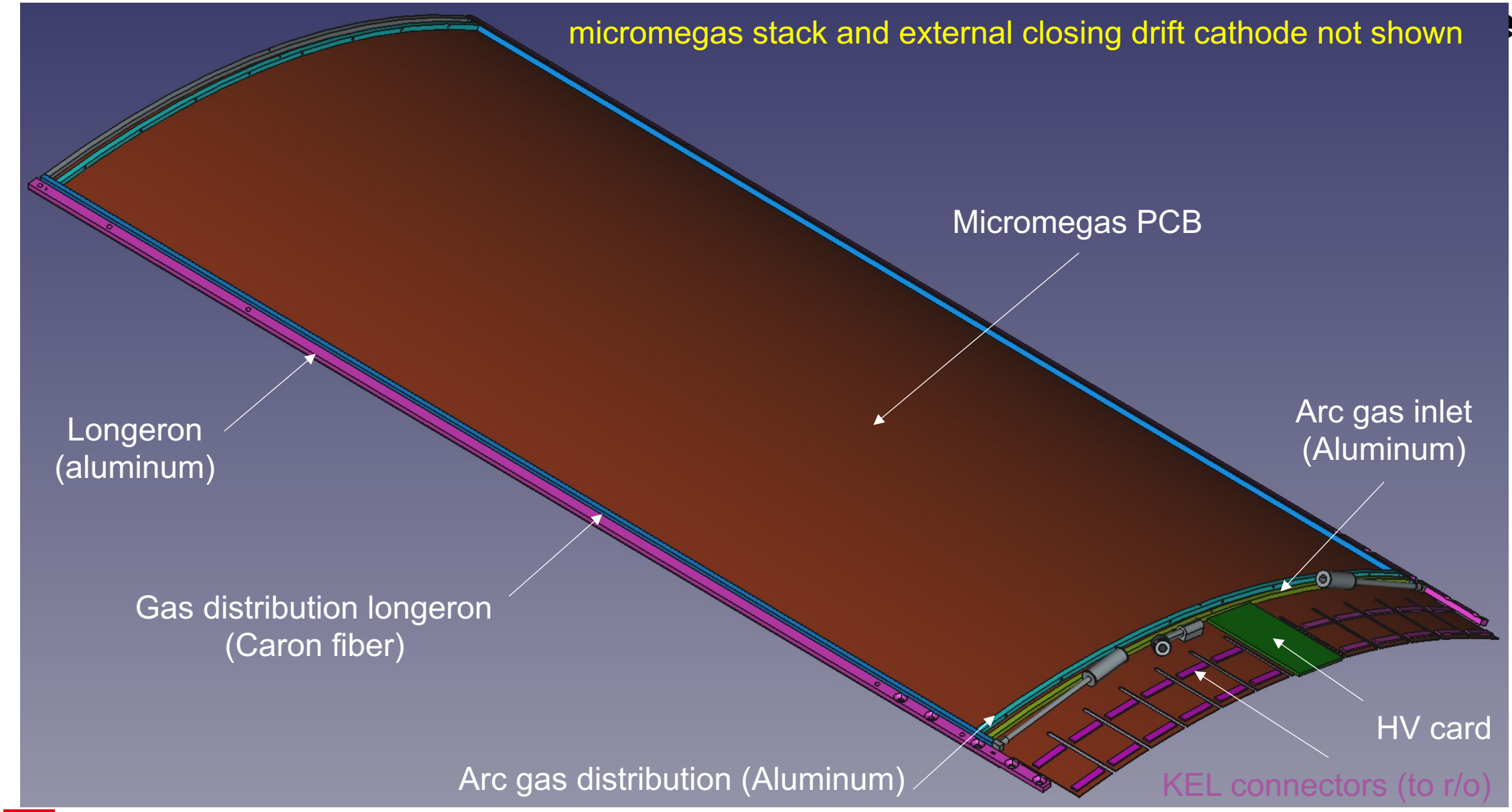
for the CEA/Saclay IRFU team

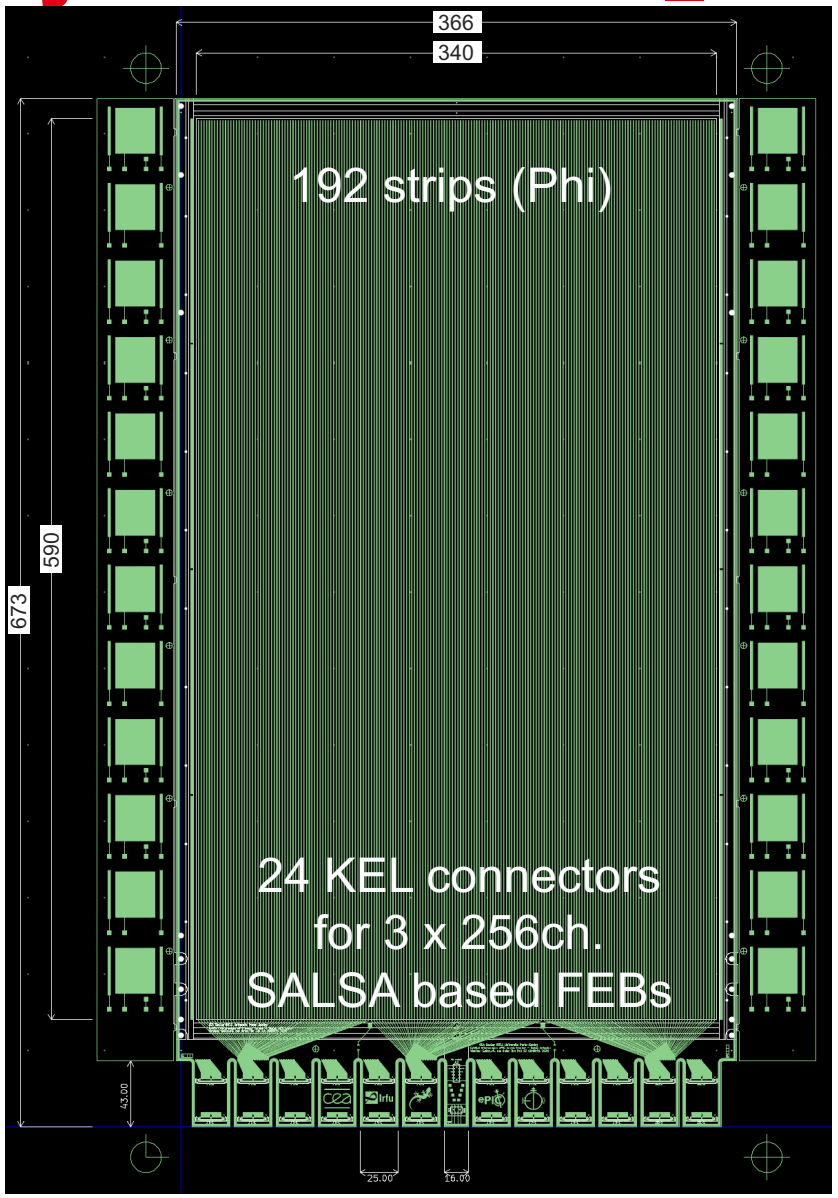


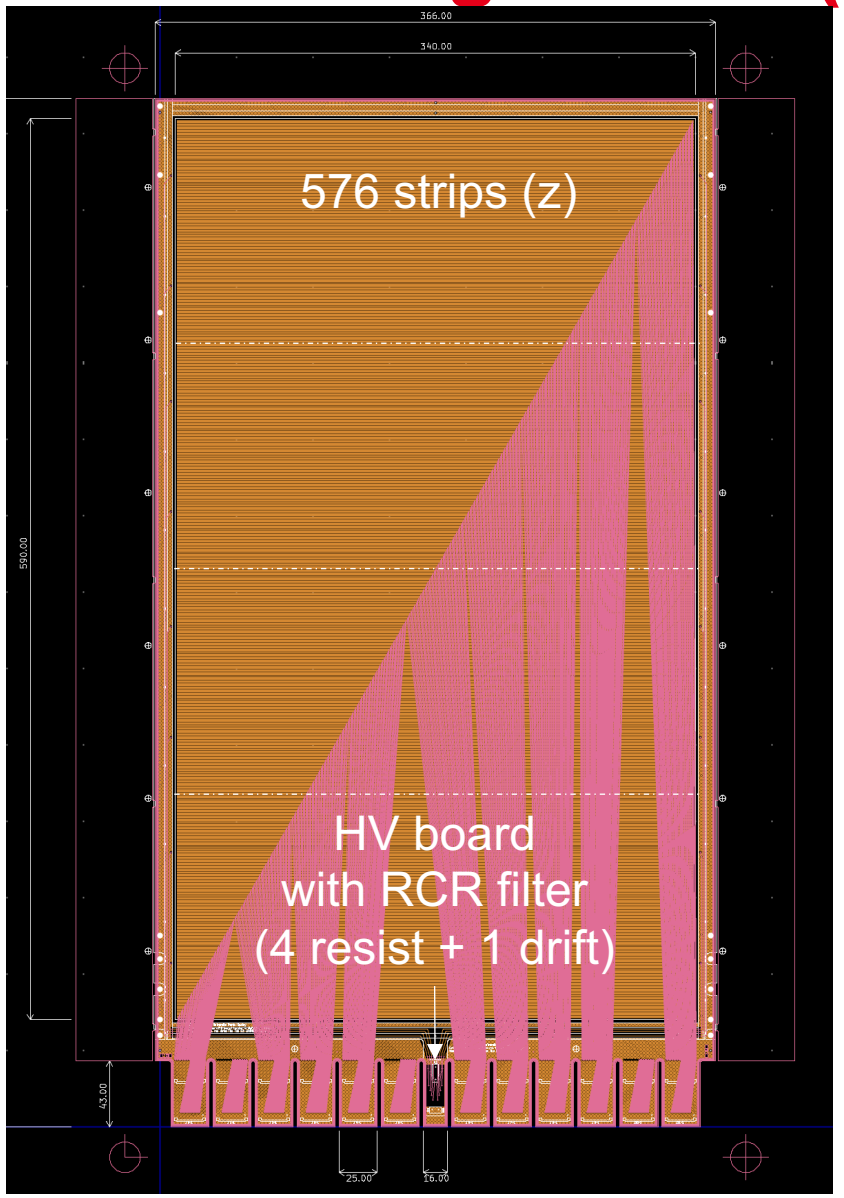
EIC/EPIC 3I meeting, 13 April 2026

CyMBaL « GEIC0_V0 » tile (under production)



CyMBaL « GEIC0_V0 » : Micromegas PCB (Version 0.8)





Drift cathode @ 3mm above MM mesh & ~-500 V

Coverlay	25 µm
copper platting	0 µm
Copper	12 µm
FR4	100 µm
Copper	12 µm
copper platting	0 µm

MM mesh @ GND

Dynamask pillars @~450V

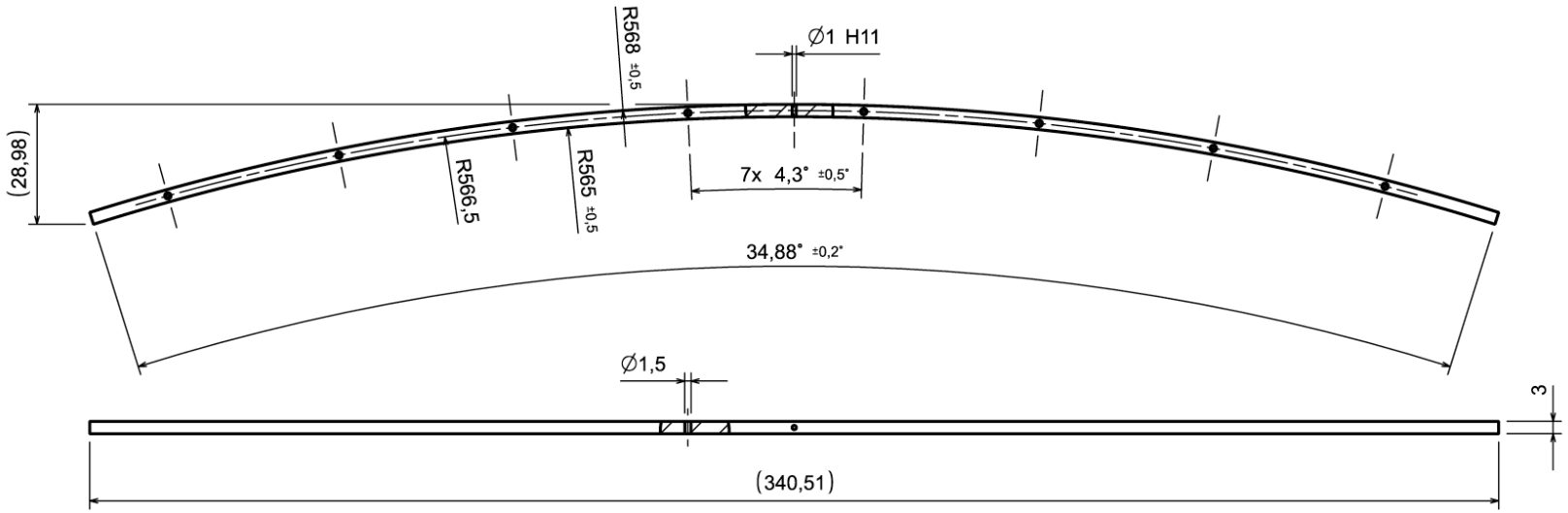
Coverlay	25 µm
Adhesive	25 µm
copper platting	0 µm
Copper	12µm
Polyimide	25 µm
Adhesive	25 µm
Copper	12 µm
Polyimide	50 µm
Copper	12 µm
Adhesive	25 µm
Polyimide	25 µm
Copper	12 µm
copper platting	0 µm
Adhesive	25 µm
FR4	100 µm
Adhesive	25 µm
Coverlay	25 µm

~300 µm total PCB thickness

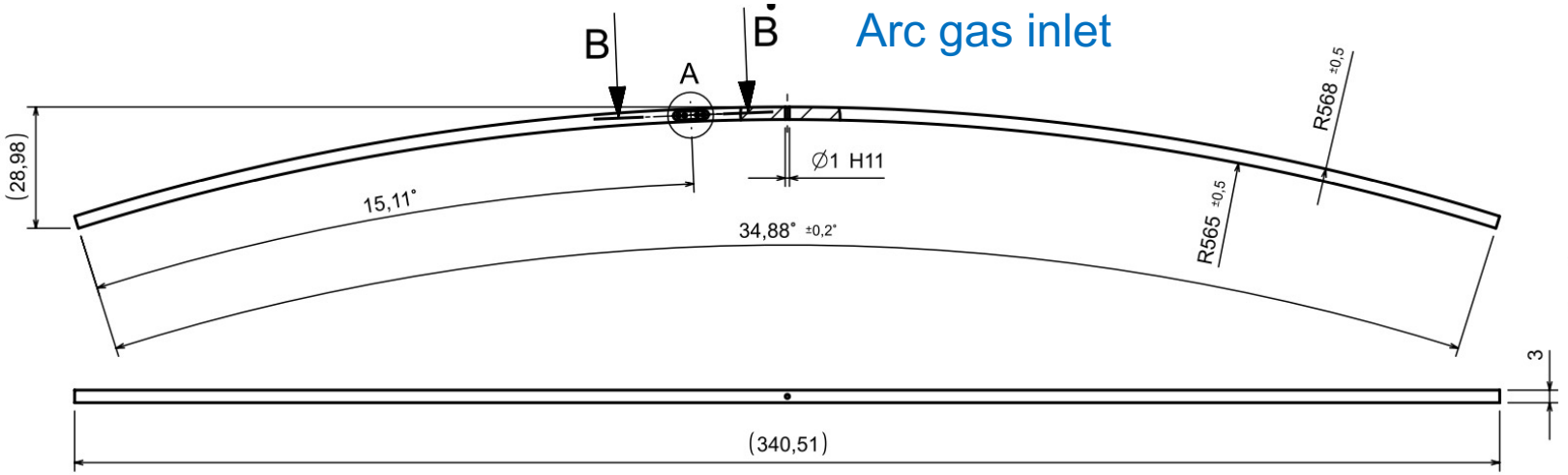
→ under production

CyMBaL « GEIC0_V0 » : Mechanicals for tile assembly

Arc gas distribution

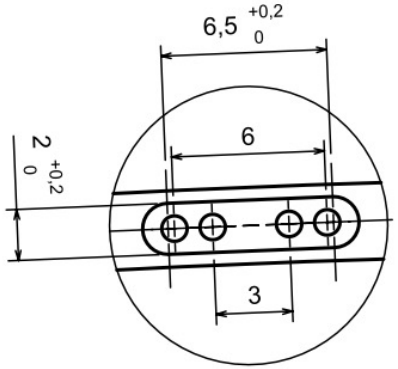


Arc gas inlet

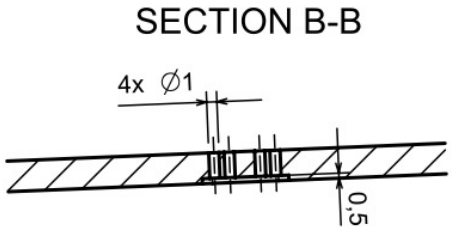


- Production drawings for mechanicals and for the flat tile and cylindrical tile assembly toolings are done.

- Production (incl. 3D pointing) in external companies and in internal workshop.

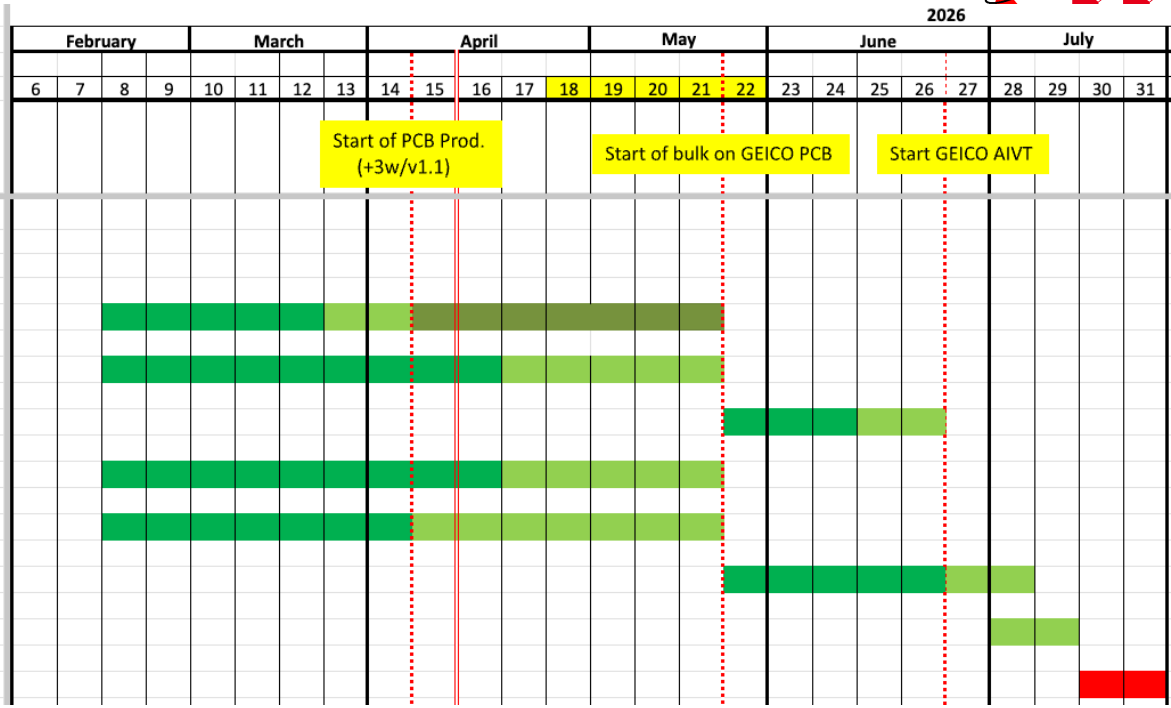


DETAIL A
ECHELLE 5:1



« GEIC0_V0 » production & AIVT timeline

A. Delbart	EIC-EPIC CyMBaL Module prototype PBS 13000		
4/10/2026	V1.5		
PBS#/WBS	**ITEM**	**Resp.**	
1 3000	**CyMBaL Module Prototype (GEICO#0)**		
	GEIC0V0 design/order/production		
	Tile assembly toolings (design-production)		
	Bulk MM (Trials on "mechanical PCBs" & final GEICO#0)		
	Cathode (design-production)		
	Mechanicals (design-production)		
	GEICO#0 assembly (trials/final Assembly)		
	GEICO#0 lab tests		
	CERN/SPS DRD1 test beam		



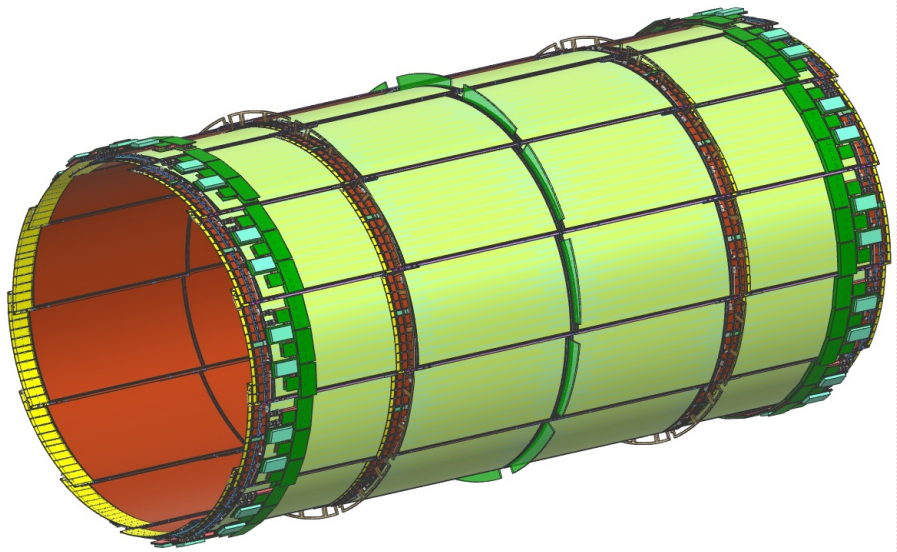
- Critical path is still the PCB production. First order (10 pces, version 0.8) placed on 4/3/2026.
- Expected delivery of 7 weeks for ~beginning of june.
- Second order for 10 PCBs to another supplier expected next week.
- Cathode order to be placed within 2 weeks (file for production done, discussions with suppliers are on-going).
- KEL connectors and KEL-KEL cables for the 768 ch. readout coupling were received.
- KEL-Mech8 adapter card(for DREAM r/o electronics) and HV card design are about to be finished.

→ No margin ! ~2 weeks margin could be recovered only by :

  - reducing to minimum the final tile performance tests
  - descoping from cylindrical to flat tile (backup mechanicals could easily be produced)

CyMBaL tiles integration & test article design

CyMBaL: Current design



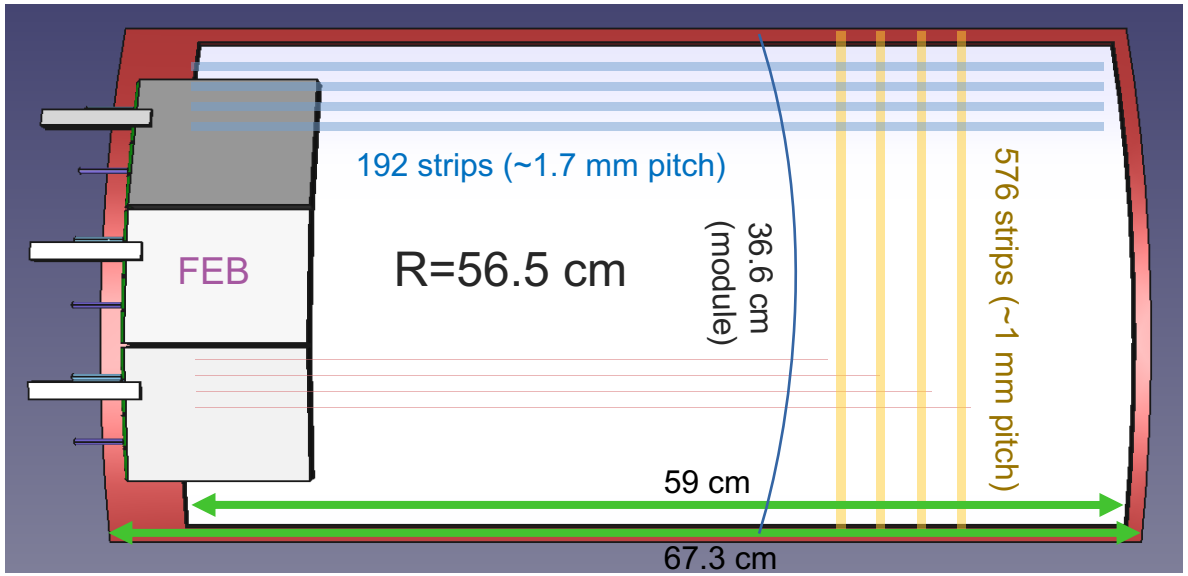
Services
via patch panel(s)

- 3 OF (to DAM)
- 5 HV cables
- 3 LV cables (1 tile)
- Gas I/O (2 tiles)
- FEB cooling I/O

2 tiles – 6 FEBs+DC/DC

few l/min of 18°C water

Design of a tile / **test article** (Cylindrical)



48 tiles: 12 in ϕ × 4 in z (integration in GST in "fish scale")

- R_{min} = 55.5 cm; R_{max} = 61.5 cm
- Overlaps in ϕ and in z for hermeticity (~2-4 cm)
- 768 readout channels/tile
- **36K readout channels in 3 FEBs/tile**

Module dimensions

Z = 673 mm / R*phi = 366 mm

Active zone dimensions

Z = 590 mm / R*phi = 340 mm

Weigh estimates

~1 kg / tile + ~0,6 kg / FEB

Expected performances

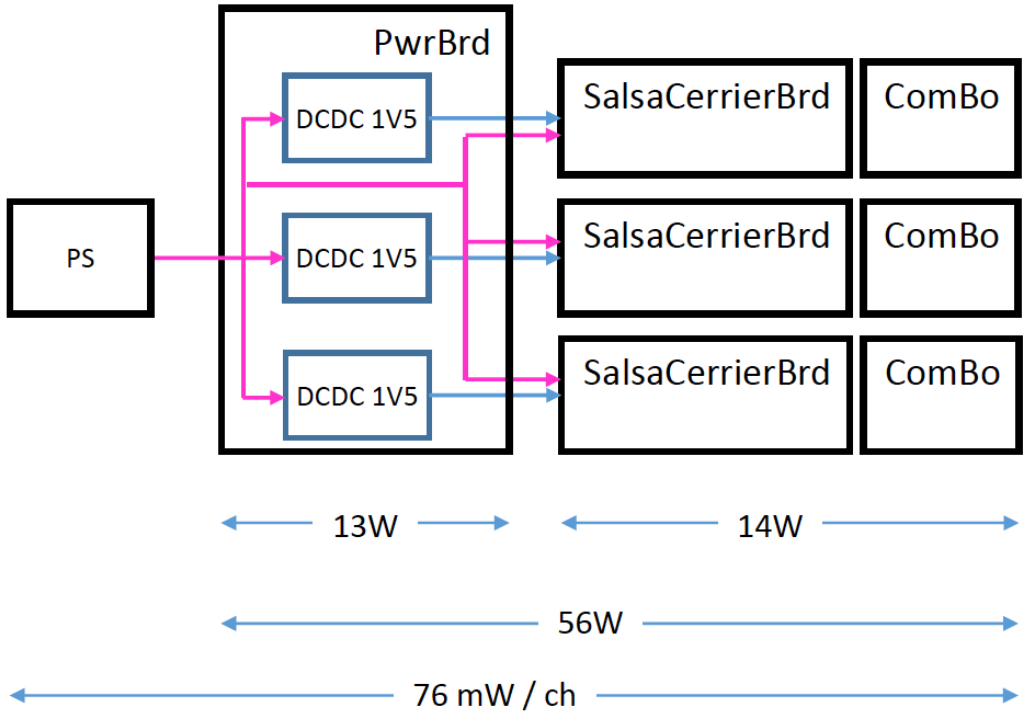
- Spatial resolution: < 300 (500) µm in Z (r*phi)
- Time resolution ~20ns
- Efficiency ≥ 98%
- Material budget ~0.5% X0

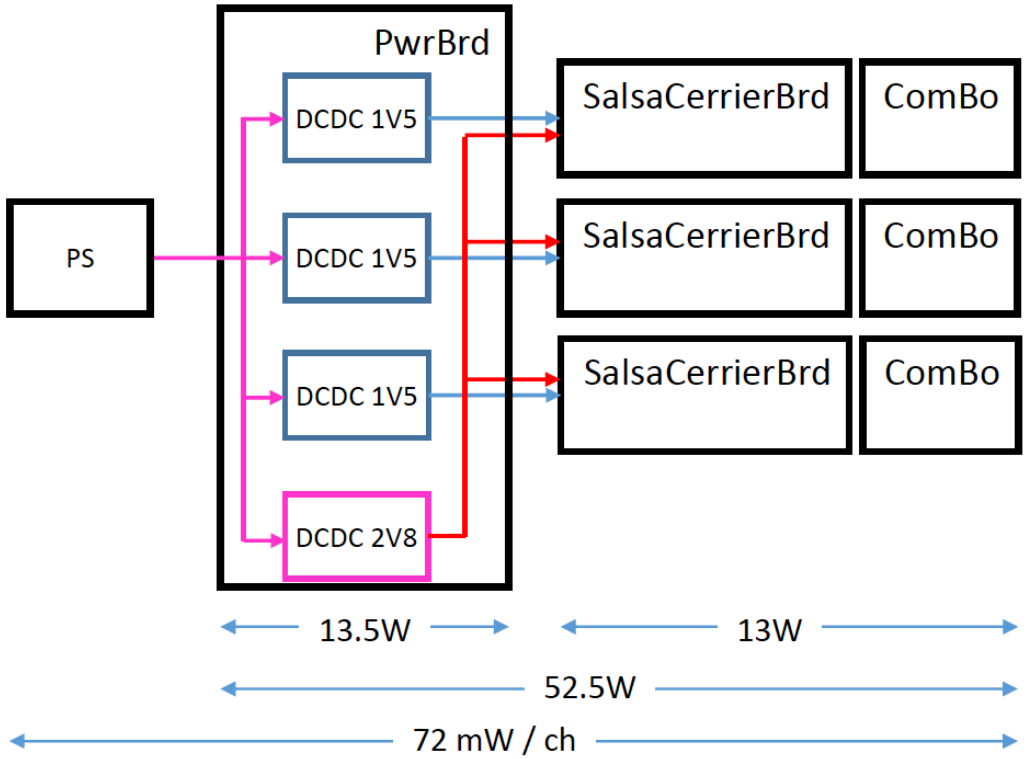
18-20°C water cooling for the CyMBaL Front-End of **updated estimate of max 58 W / Tile (2.8 kW total for CyMBaL)**

Low-Voltage power distribution on-going studies

From I. Mandjavidze slides (2026/04/07)

- Is it worth to have 4th shared DCDC converter as a source of 2.5V ?
- Comparison is given for Salsa current of 2A (baseline)





- Comparable power consumption and heat dissipation wise
- Scheme on the left seems easier to implement

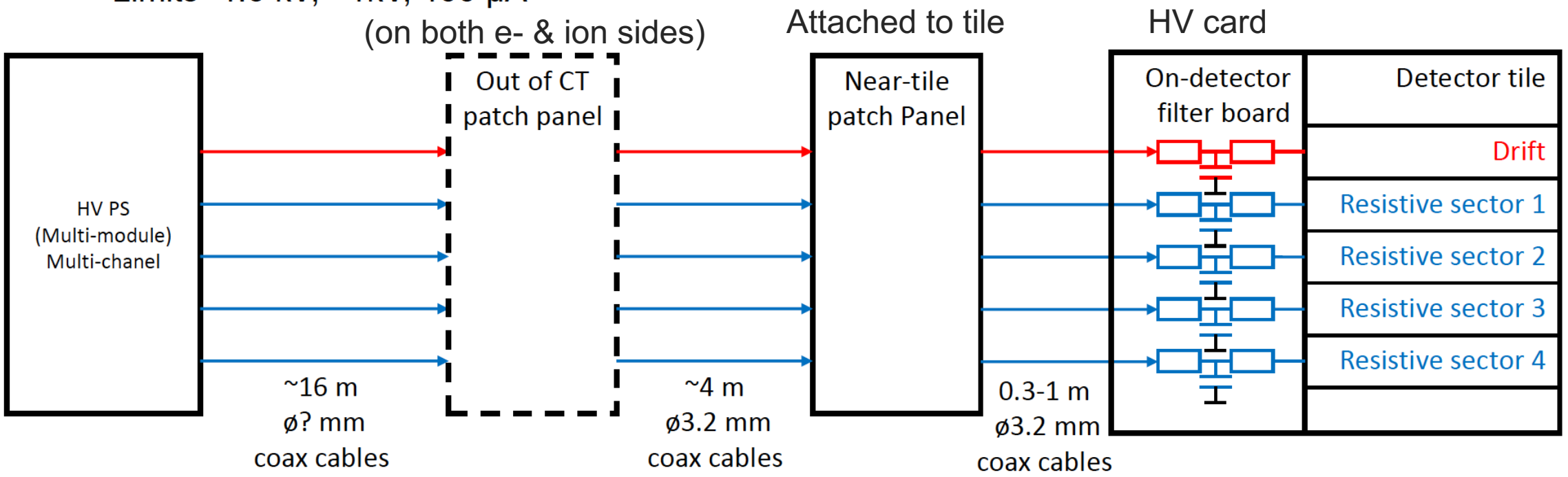
→ To be discussed at next 16 april E&DAQ WG meeting

Possible synergies / card sharing with AC-LGAD TOF LV power distribution ?

High-Voltage distribution proposal

From I. Mandjavidze slides (2026/04/07)

- 5 HV power lines per detector tile
  - → 4 independent resistive segments at O(+500V)
  - → 1 Drift electrode at O(-1 000V)
  - → Limits -1.5 kV, +1kV, 100 µA
    (on both e- & ion sides)



- Reminder : 48 detector tiles
  - → Groups of 24 tiles powered from electron and ion sides

Status of CyMBaL barrel design

BNL-Purdue-Saclay bi-weekly meetings. First concept of CyMBaL – AC-LGAD TOF interface to work on.