FCFD status

Artur Apresyan

EPIC Electronics & DAQ WG meeting : eRD109 Monthly Progress Reports

Mar 19, 2026

Design review held on

- Performed an in-depth design review of the FCFD with an external review team
  - Review committee : Troy England (FNAL), Jim Hirschauer (FNAL) (chair), Ron Lipton (FNAL), Tonko Ljubicic (Rice), Bojan Markovic (SLAC), Larry Ruckman (SLAC)

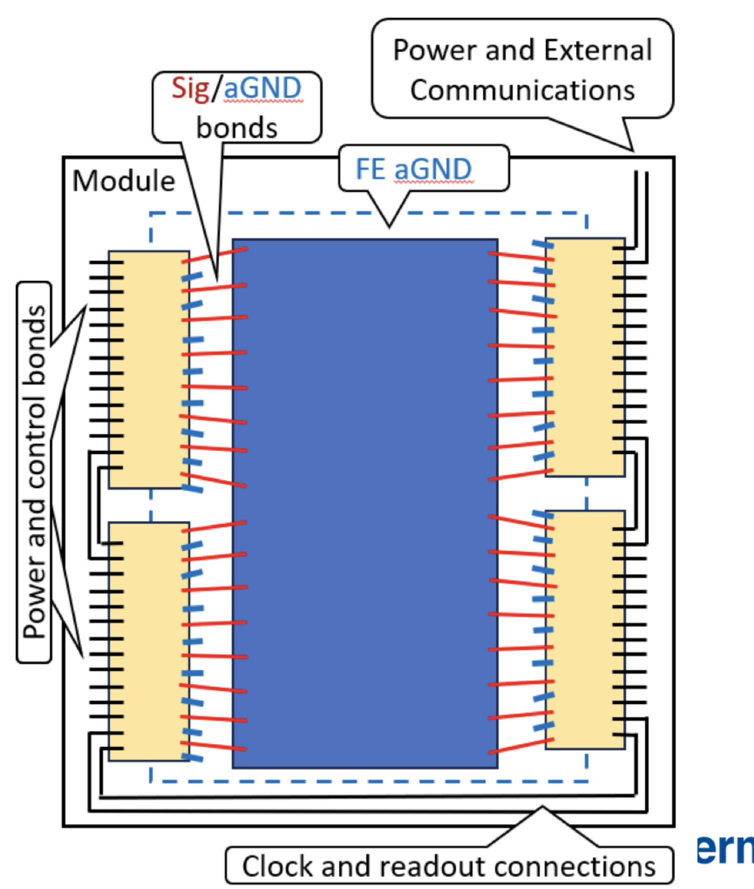
- The review committee recommends to proceed with submission, and based on the review of the technical aspects of the chip design, the review committee finds that the technical risk associated with this chip submission is low.
- The most significant recommendation is to seek sign off for the stave design proposed by the FCFD team

Stave design proposal

- We presented the proposal to the ePIC AC-LGAD TOF DSC Weekly Meeting on March 12, requesting sign-off
  - https://indico.bnl.gov/event/32008/

One-sided ASIC Design

- **Each sensor has dedicated readout ASICs**
  - Simple modules for testing
  - Easy aGND/dGND separation
  - Plenty of real estate for i/o and power
  - No need for half-sensors
- **32-channel ASIC selected**
  - Practical chip size and aspect ratio 14-15 by 2-3 mm
  - Direct wire-bonding to the sensor
  - Channel pitch is slightly less than that of the Sensor (0.5mm) so to butt two chips along the Sensor, allowing for a small gap between them. That will cause some fanning of the signal wire-bonds, but not significantly affecting bond length
  - Reasonable fan-out angles (1mm shift for 3-4mm long bonds)
  - All 4 ASICs are connected in a single readout chain

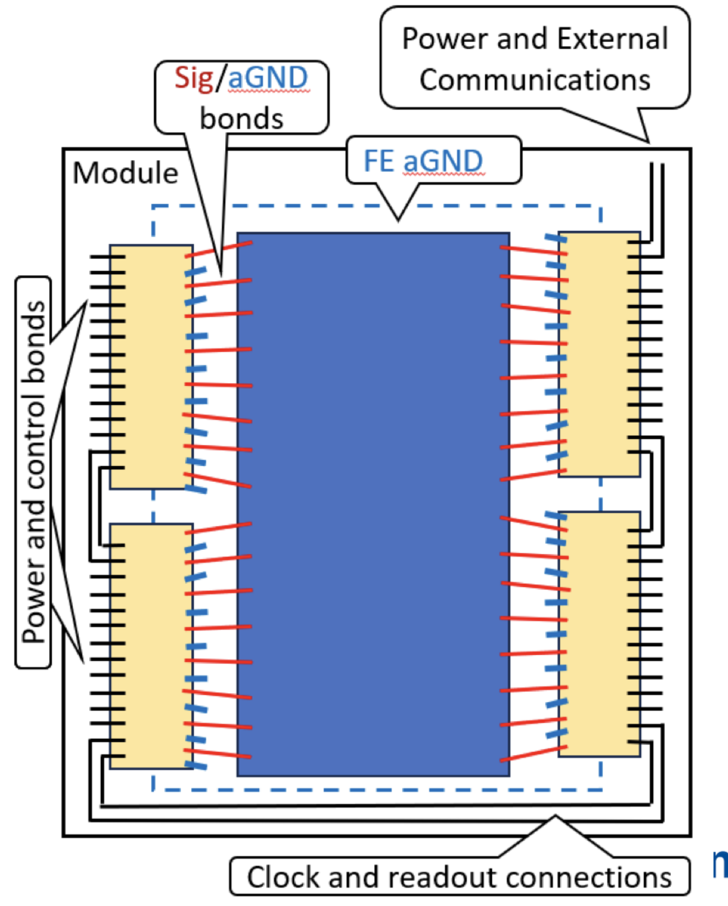


Stave design proposal

- We presented the proposal to the ePIC AC-LGAD TOF DSC Weekly Meeting on March 12, requesting sign-off
  - https://indico.bnl.gov/event/32008/

- **Benefits**
  - Direct wire-bonding between the Sensor and FCFD
  - Smaller chip, higher yield
  - Ample real estate for power and control signals
  - Local analog ground improves ground loop immunity
  - Easy to combine multiple modules in a single assembly
  - No need to have half-size sensors
- **Things to watch**
  - Module width <40mm to allow for full coverage in two layers
  - That is about 9.5mm for FCFD on each side:
    - Chip 3mm
    - Sensor-ASIC gap 2-3mm
    - Back-side bonds 1mm
    - Extra routing area 2mm
    - pcb edge clearance 0.5mm

    - **Total 8.5-9.5mm**



FCFD1.2 design status

- Final stretch : focusing on full integration and verification work
- First draft GDS submission on March 25:
- Tape-out on on April 21
- All parts are included
- Current focus to make sure all testbenches pass testing
- After submission will work on the test-board design and preparations for the characterization campaign
- And switch gears towards the FCFD variant design