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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting
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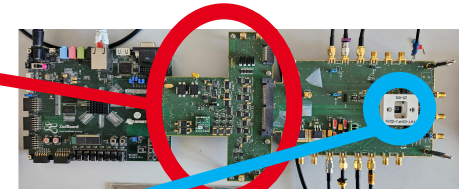
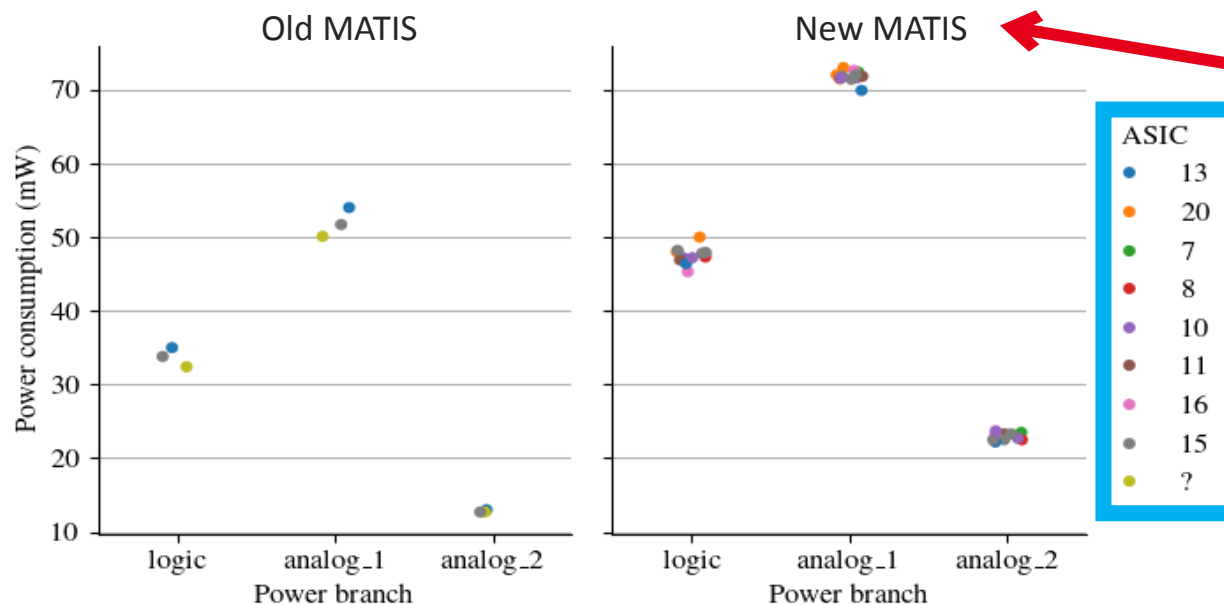


PRISMEv1 prototype (PLL test chip)

- Used to do tests of high-speed links and CDR decoding (implemented in PLL)
- Radiation tests postponed again by CERN → May-June (idem for SALSA1). Also searching for another radiation facility but not easy to find calibrated gamma source

SALSA1 prototype

- New power consumption measurements
- 3 power consumers: front-end incl. buffer before ADC; ADC; and PLL + logic; powered at 1.2V
- Discrepancies between measurements with 2 different MATIS test cards due to different resistor
- Results: logic ~48mW, front-end ~72mW, ADC ~22mW → ~21mW per channel (without counting bias contribution in front-end consumption)



ASIC	
●	13
●	20
●	7
●	8
●	10
●	11
●	16
●	15
●	?

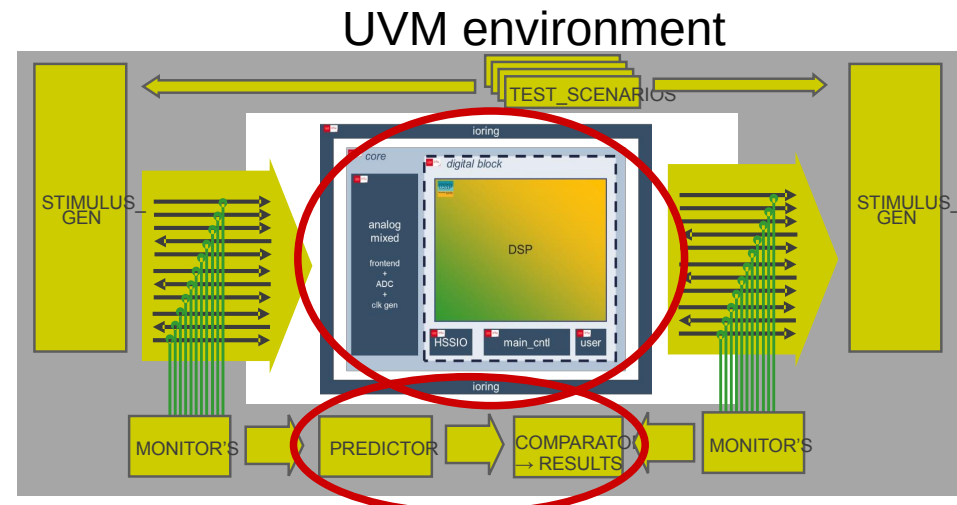


SALSA2 development status

- Front-end: done and tested, but layout ongoing to groups the channels together with bump connection. Also block with biases, probes, injection, etc... ongoing
- DSP: integration ongoing, some modules still not finished (calibrations, fast commands). Also tests of DSP synthesis ongoing to have firsts estimations of size and power consumption
- I/O: most modules done. Work ongoing on PLL integration, monitoring registers. Tests of synthesis to be done to evaluate size and power consumption
- Control core: some modules still under development, like fast command decoding, state machine, monitor data packets, some slow-control registers
- Some features dropped to speed-up verifications: unified input interface, long information packets
- Floor plan: integration of analog part ongoing; evolution ongoing on pin-out definition
- UVM environment: workspaces created for each block, 1st version done for each, integration of golden models ongoing, advanced scenarios to be done

Timeline

- Still a lot of works ahead:
 - code validation and integration
 - digital layout generation and validation
 - assembly of all blocks
 - simulations of the whole chip
- Chip submission foreseen 1st semester 2026, but optimistic
- Tests from beginning 2027
- Distribution to users in 2027





■ eRD109 FY23 project milestones

- Specifications of SALSA1 design → done
- Production of SALSA1 prototypes → done
- Test card production → done
- Performance evaluation → done (excepted radiation)

■ Milestones of generic R&D program for EIC project (new 65nm PLL block)

- PRISME prototype submission → done July 19th 2023
- Packaging and test card production → done February 2024
- Radiation tests → done November 2024

■ RD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → aiming 1st semester 2026
- Beginning of SALSA2 tests → beginning of 2027

■ eRD109 FY25 project milestones

- SALSA3 design specifications → aiming 1st or 2nd semester 2026 (after SALSA2 submission)
- SALSA3 submission → 1st semester 2027
- Performance evaluation → 2nd semester 2027 - 1st semester 2028

■ Very next steps

- SALSA1 tests → TID tests in May or June hopefully...
- PRISMEv1 chip → TID tests in May or June
- SALSA2 development → in progress