

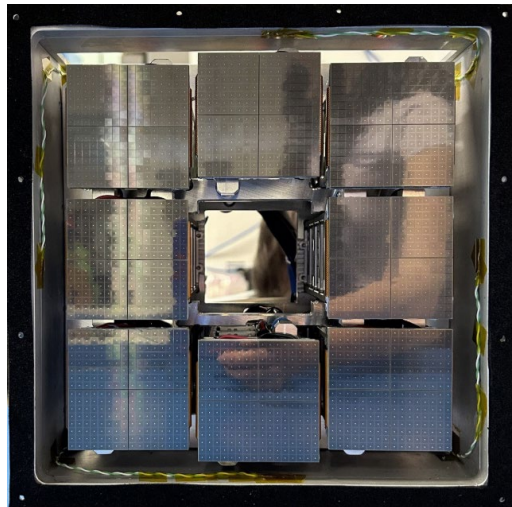
eRD109 update: dRICH RDO

D. Falchieri (INFN Bologna) for the RDO team:
Pietro Antonioli, Sandro Geminiani, Matilda Panza,
Luigi Rignanese, Giovanni Torromeo

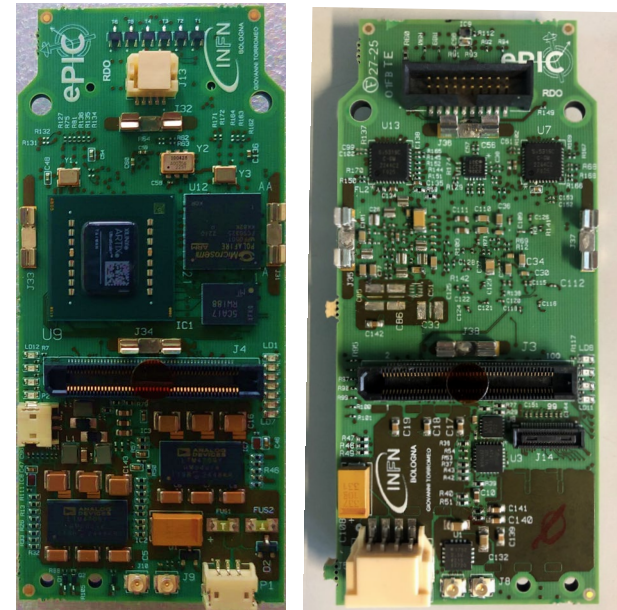
ePIC DAQ meeting
19 March 2026

RDO boards status

- We currently have **8 working RDO boards**:
 - one is currently used to debug the scrubbing,
 - one is used to test the high-speed link in connection to the Alinx-FADE DAM-like boards
 - 6 RDO boards are currently used with the SiPM prototype
- we are not planning to have other RDO manufactured in the coming months
- 7 RDO boards will be available for the May and June test beams (the one in use at Trento will not be available in the coming months)

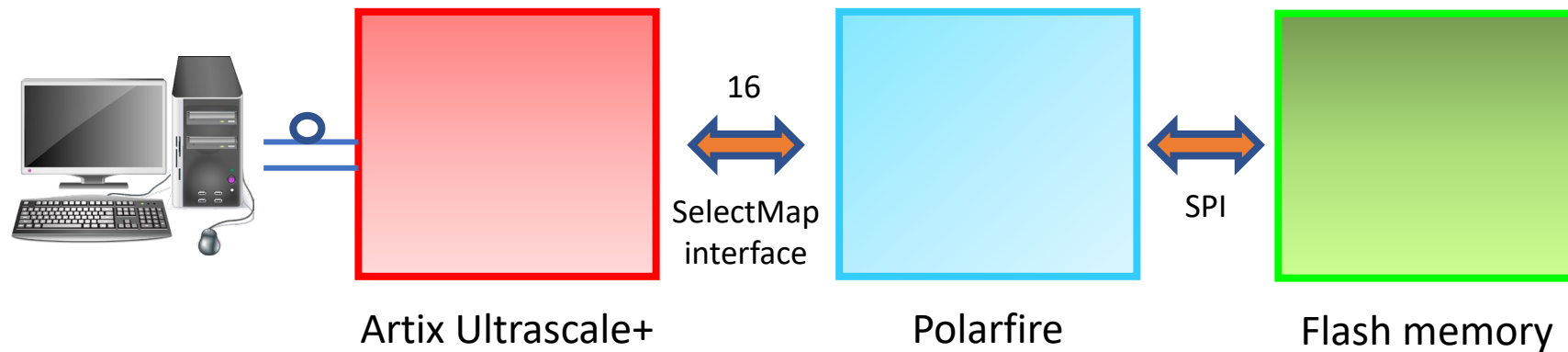


SiPM prototype

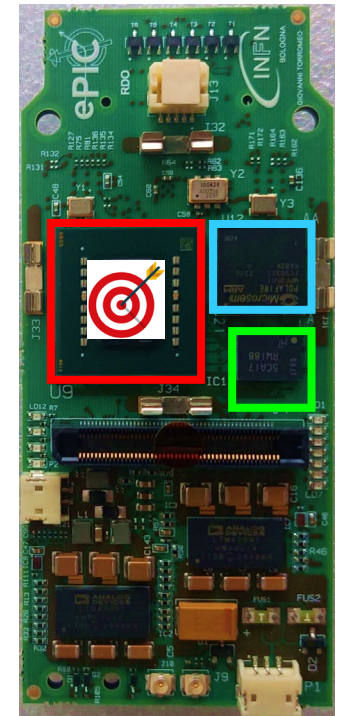


RDO: scrubbing

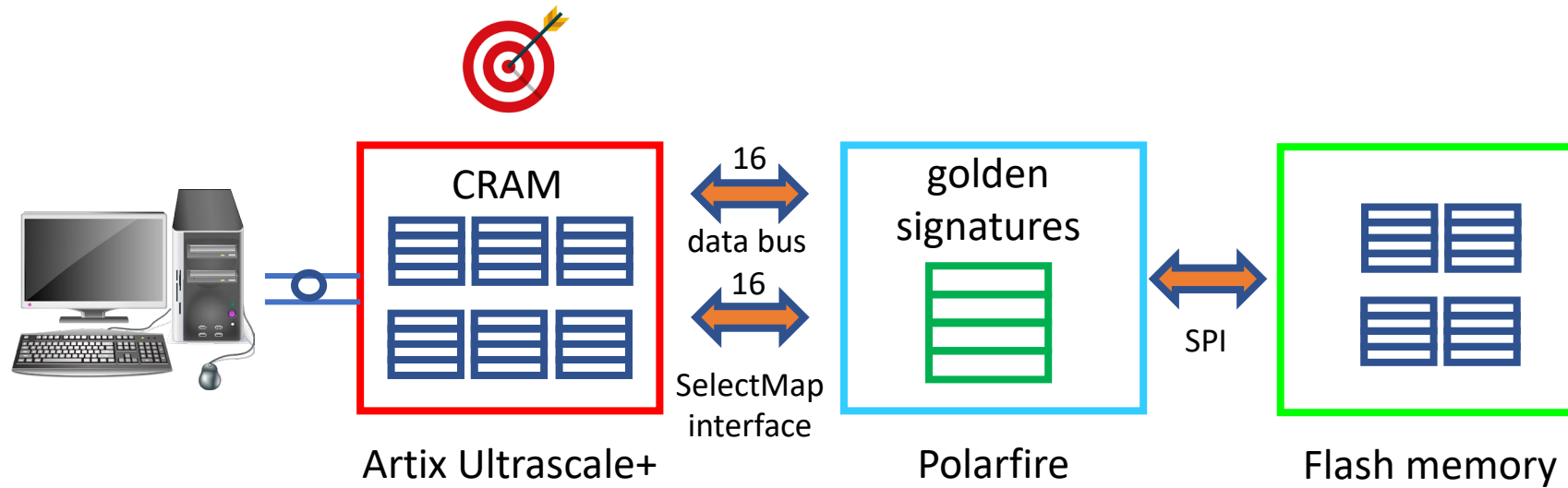
- We are preparing an irradiation test with protons in Trento (Centro di ProtonTerapia) for next week:
 - **28 March 2026**
- First goal is to irradiate the Artix Ultrascale+ with Polarfire-based scrubbing in place



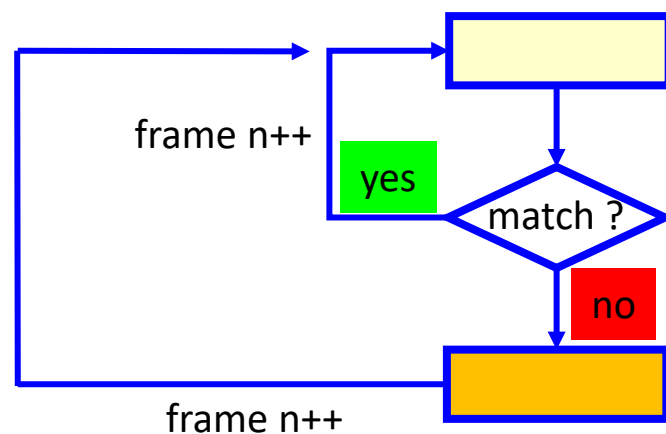
The goal of the scrubbing is to keep the CRAM of the Artix US+ clean



RDO: scrubbing



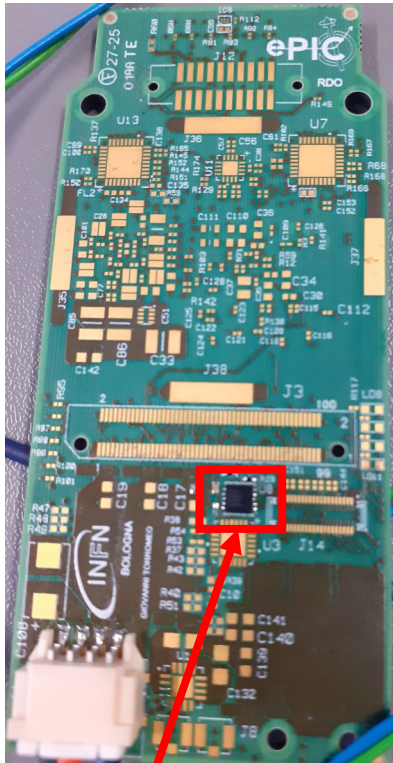
The Artix US+ CRAM features ~14500 frames (each one contains 93 words of 32 bits each)



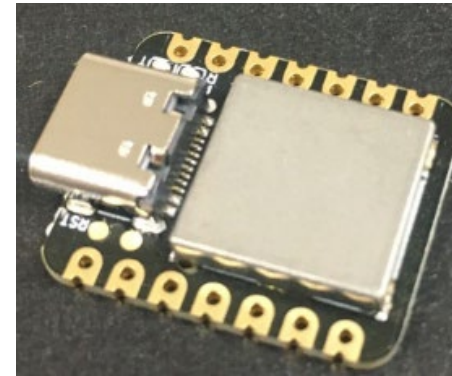
the Polarfire reads frame **n**, calculates a signature on the fly and compares it to a golden signature stored in a BRAM

the Polarfire reads frame **n** from the FLASH and writes it to the Artix US+ via the SelectMap bus

Other irradiation targets



charge pump chip



SAMD21:
 low power 32-bit ARM
 Cortex microcontroller
 from Microchip with
 256 Kbytes of Flash and
 32 Kbytes of SRAM

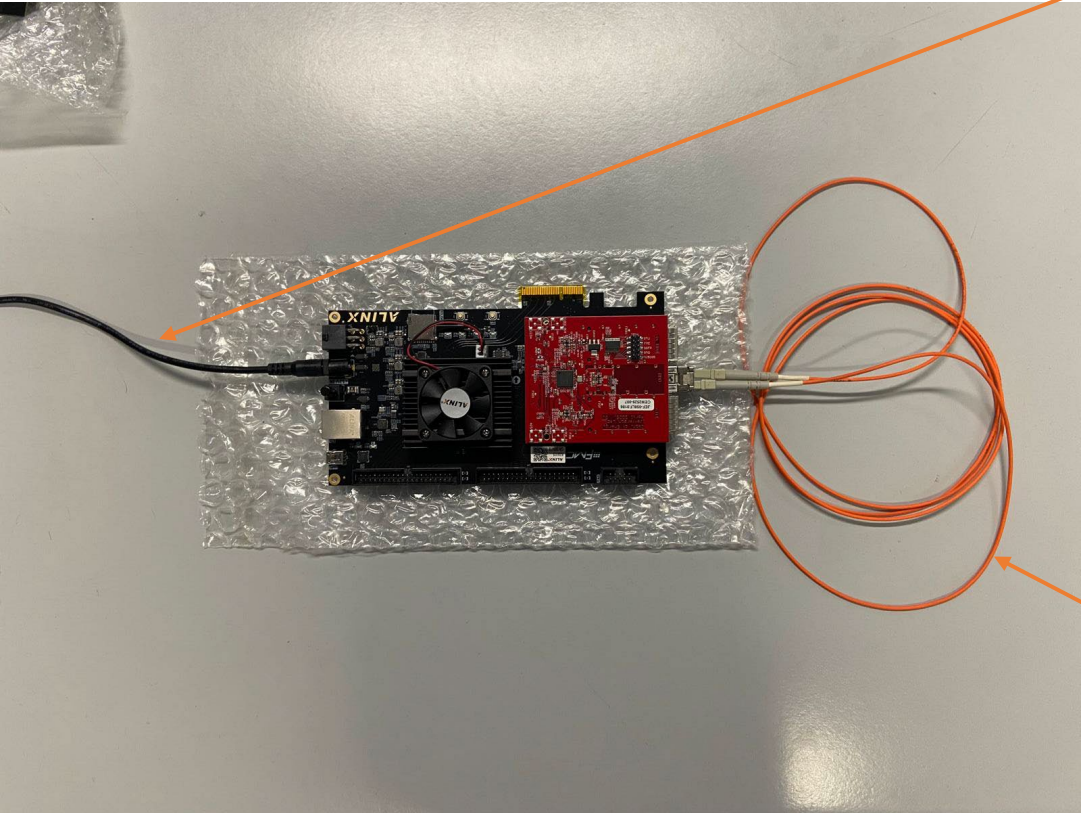
from January 2026 report about last irradiation session of SAMD21

Full analysis in progress, however:

- SEU c.s. (RAM) $\sim 3\text{-}4\text{E-}14 \text{ cm}^2/\text{bit}$
- TID \rightarrow worked ok up to 8 krad (~ 16 times TID expected at dRICH)
- failed at very high doserate (124 rad/s) \rightarrow next run will be tested not powered when at high doserate

Towards RDO – Alinx setup

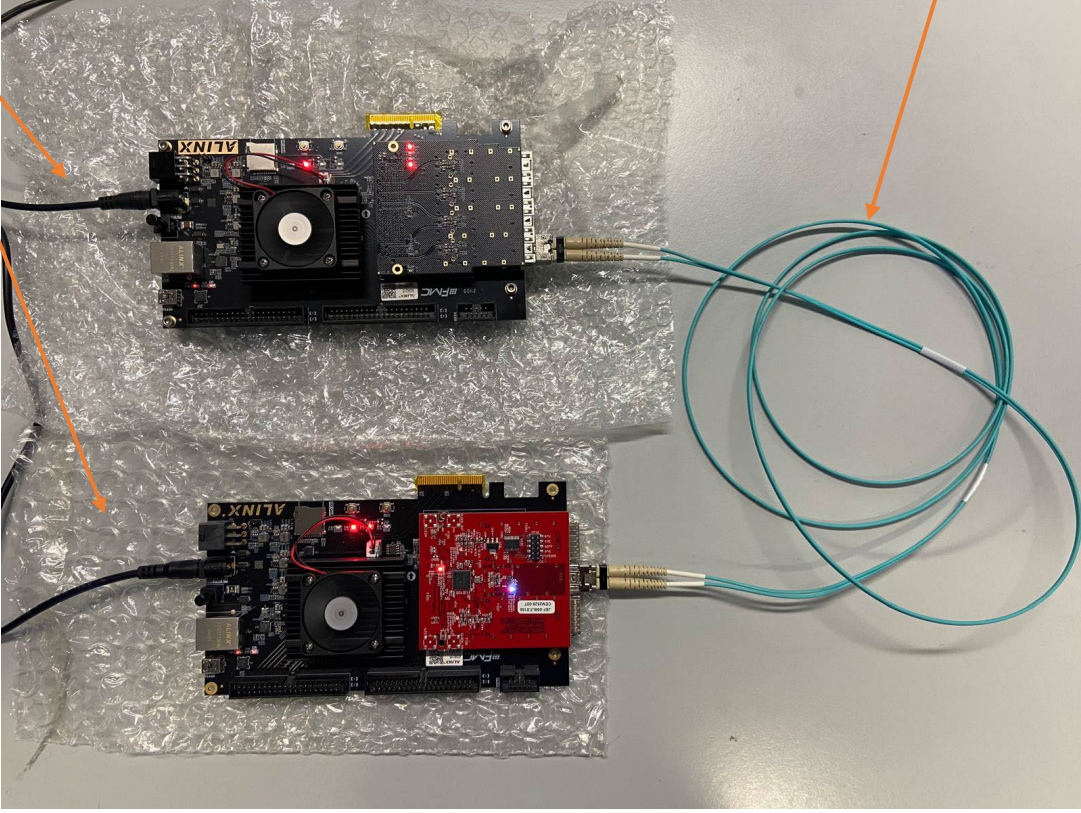
1. FADE loopback configuration:



power supply

optical fiber

2. FADE-To-ALINX configuration:

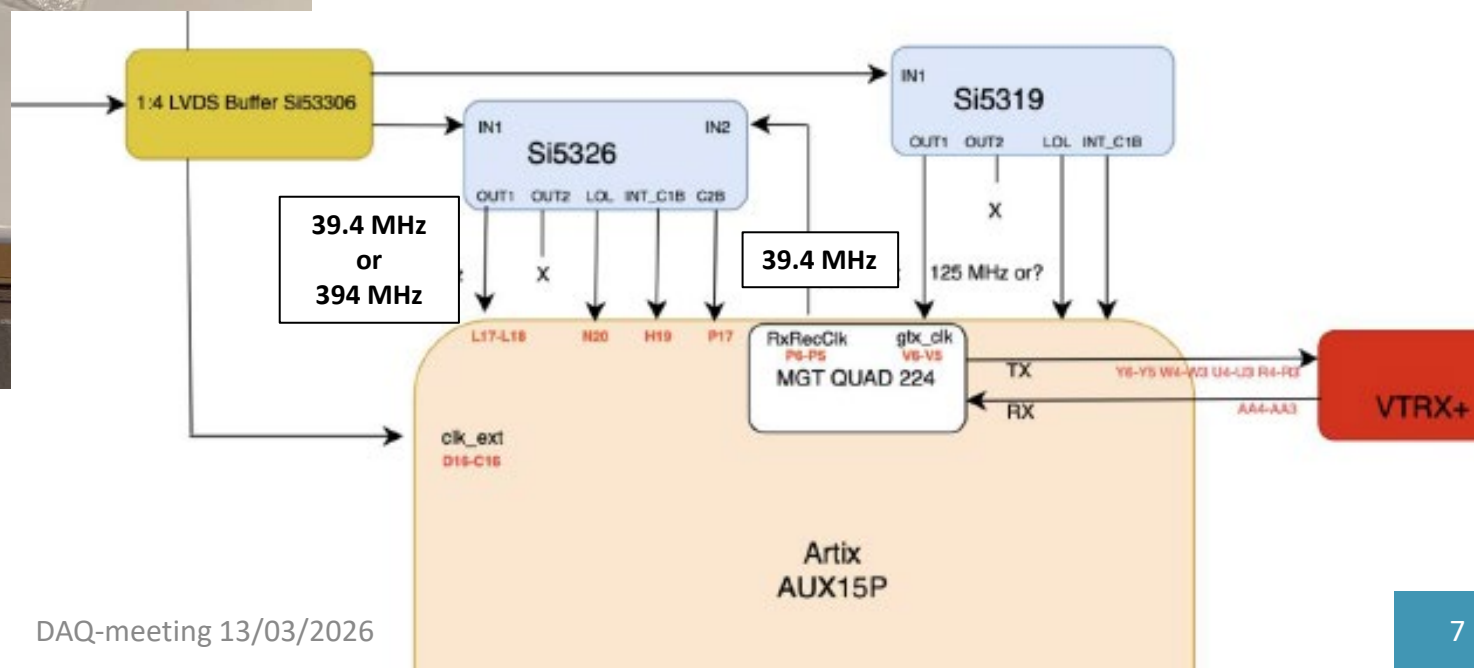
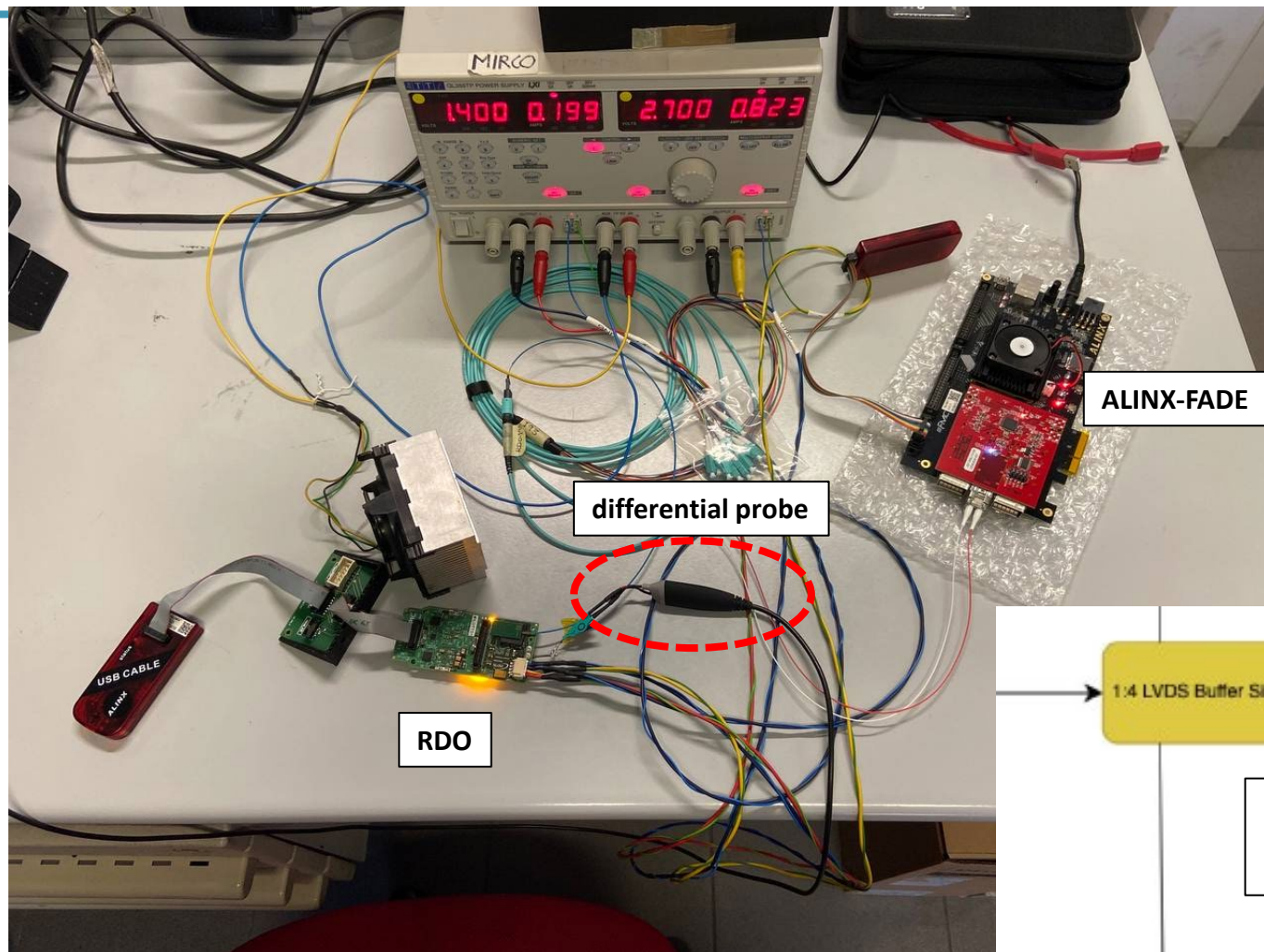


optical fiber

First tests with the Xilinx IBERT IP core

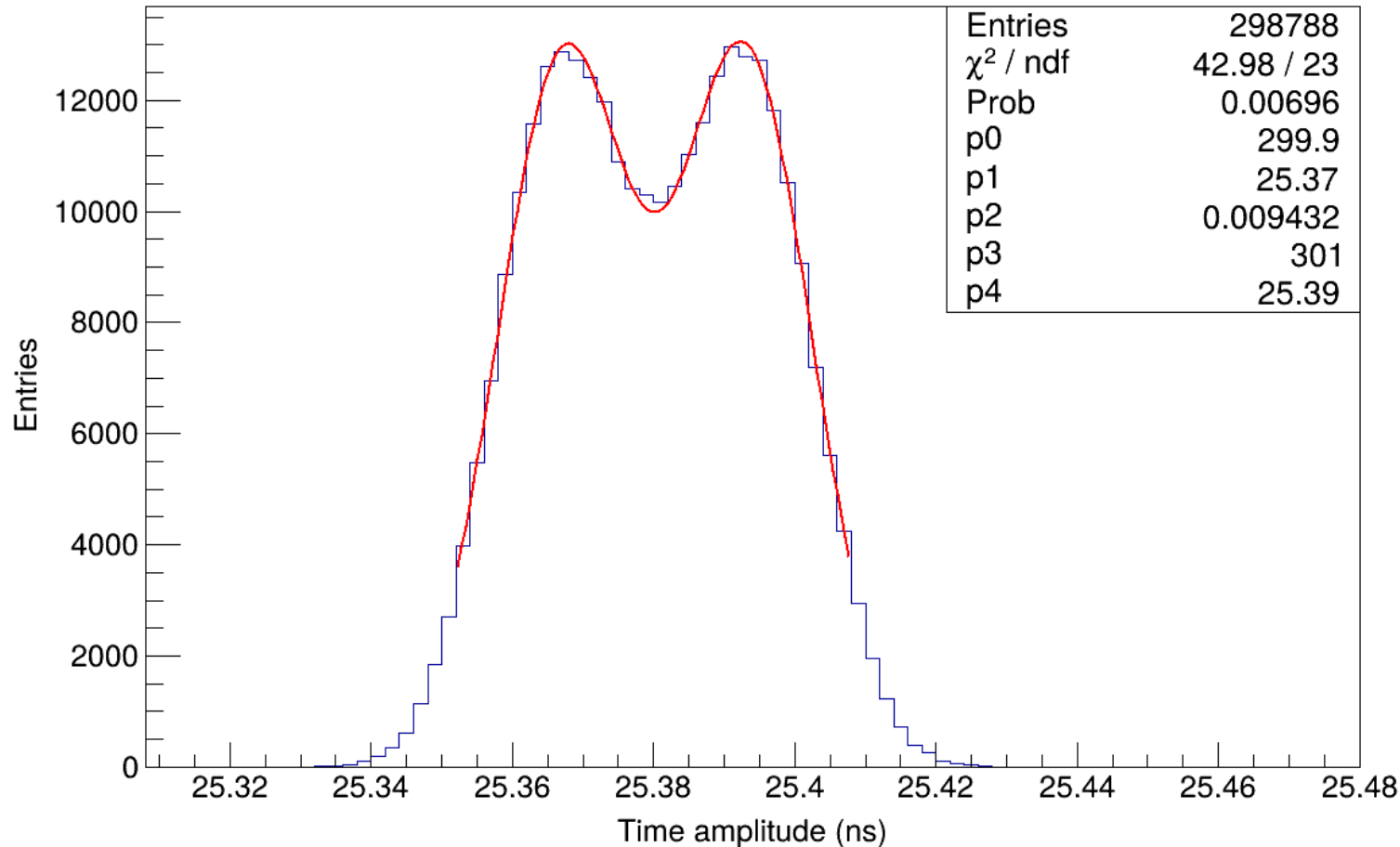
RDO – Alinx setup

- optical link between FADE and RDO card with a ~ 1.5 Gb/s throughput:
reconstructed clock : 39.4 MHz
- LVCMOS25 clock in output to a scope using a differential probe
- **caveat: the reconstructed clock is not yet sent to the Si5326 jitter cleaner.**



Jitter measurements

RDO rec_clk jitter measurements



- **p1**: first peak mean
- **p2**: random Jitter
- **p4**: second peak mean

deterministic Jitter = $p4 - p1$
DJ = 25.79 ± 0.09 (stat.) ps

random Jitter = p2
RJ = 9.43 ± 0.03 (stat.) ps



good estimate, but still a preliminary result!

- finalize the scrubbing mechanisms
- begin studying IpGBT/full protocols
- implement the remote programming of the Artix US+