HRPPD Meeting #15 Update

2026-03-24

Raymond Dawson

Jefferson Lab

U.S. DEPARTMENT of ENERGY

Current Status

Tasks:

- Kyocera 10-layer quote
- High priority tasks before HRPPD order
  - Perimeter dimension confirmation: 119.23 mm vs 119.126 mm
  - Additional crosses if not visible in screw holes
  - HV backplane layout
  - Final simulations – 15-layer and 10-layer
- Upcoming items
  - FCFD testing
  - Interposer design and order by mid-April
    - Thickness dependent on spacer pull testing and design
- Open items:
  - Mounting hardware – is titanium a requirement?
  - 1mm vs 3mm spacer – tied to interposer thickness
  - Mechanical envelope and VTRX+ requirements
  - Review action item list

- FCFD Test Board
  - Received FCFD boards Wed 3/11
  - Regulators arriving 3/25

No update

- Spacer thickness
  - TBD Will send ceramic and PCB 3D models to Alex once complete for spacer mockup
- Backplane Changes
  - See action item list

Kyocera File Updates

These changes have not been communicated, will be sent with final files

- 10-layer ODB++ files
- Outline reduction to 119.126 mm
- New cross locations at corners
- Cross thickness reduction to 5mil from 8mil
- Moved HV contact pad locations*
  - Depending on following HV discussion

HV Spacing Rules

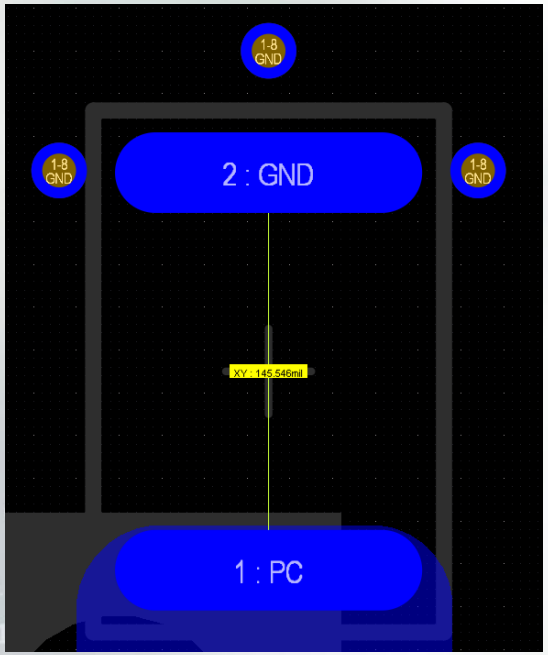
- HRPPD rules derived from Incom + Gerard testing: 1kV/mm for bare copper on surfaces
  - Tim HV board uses ??? 4kV capacitor 
- IPC2221C from standard – at sea level (no vacuum), very conservative
- Picked the minimum of HRPPD rules or IPC
  - All rules but internal conductors Exit Bottom to GND use HRPPD rules
- Clearances must be observed both horizontally and vertically
  - Will add additional safety factor to account for board tolerances ~25%

External Conductors			Spacing (mils)	Spacing (mils)	
Voltage		Max Vdiff	Final Rule	HRPPD group	IPC-2221C
PC	from GND	-2500	98.4	98.4	492.1
	from ExB	-2000	78.7	78.7	393.7
EnT	from GND	-2100	82.7	82.7	413.4
	from ExB	-1600	63.0	63.0	315.0
EnB	from GND	-1450	57.1	57.1	285.4
	from ExB	-950	37.4	37.4	187.0
ExT	from GND	-1250	49.2	49.2	246.1
	from ExB	-750	29.5	29.5	147.6
ExB	from GND	-500	19.7	19.7	98.4

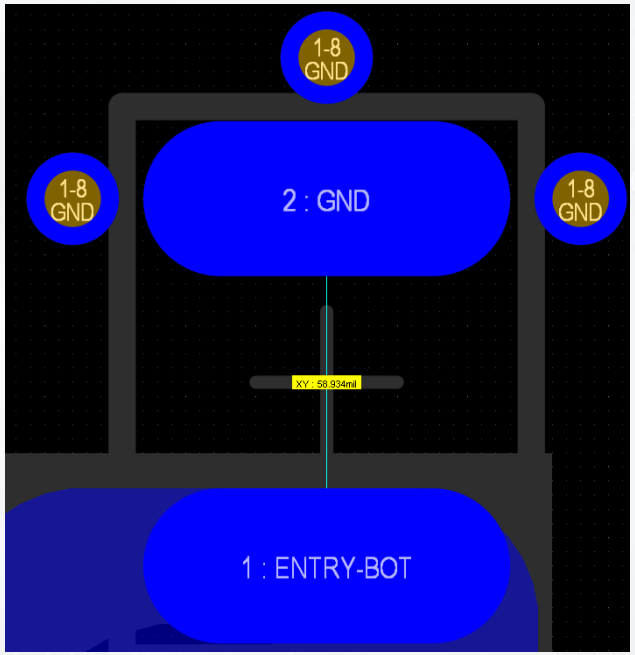
Internal Conductors			Spacing (mils)	Spacing (mils)	
Voltage		Max Vdiff	Final Rule	HRPPD group	IPC-2221C
PC	from GND	-2500	98.4	98.4	206.7
	from ExB	-2000	78.7	78.7	157.5
EnT	from GND	-2100	82.7	82.7	167.3
	from ExB	-1600	63.0	63.0	118.1
EnB	from GND	-1450	57.1	57.1	103.3
	from ExB	-950	37.4	37.4	54.1
ExT	from GND	-1250	49.2	49.2	83.7
	from ExB	-750	29.5	29.5	34.4
ExB	from GND	-500	9.8	19.7	9.8

Capacitor Selection and Placement

- For PC and Entry Top connections, 1812 capacitor selected @ 3kV rating
  - 100 mil spacing for PC
- For all others, 1210 capacitor selected
  - 57.1 mil spacing required for Entry Bottom
- Placed capacitors on bottom layer due to unknown connector selection
  - Requires moving HV pogos and cutout for capacitors in spacer
  - Limits spacer thickness



1812 capacitor



1210 capacitor

Layout Demo

- Notes
  - VERY rough draft of layout!
  - Pogo pins
  - Capacitor placement
  - Exit Bottom plane routing
- Questions
  - Need separate caps for each of the 4x bottom of exit MCP connections?
    - Yes
  - Need a resistor for ringing?
    - If space available, may not be needed until board is tested
  - How to size capacitors based off bottom MCP?
    - ~10x size of exit of bottom MCP to GND
  - Safety resistor placement here or distro board?
    - Place on backplane is space available

Appendix

Stackup

- Isola FR4 406 or Isola FR 370HR

8-layer

Layer	Spacing (mils)	
1		Sig
	8	
2		Gnd
	8	
3		Sig
	8	
4		Gnd / HV
	15 - 70.1	Depending on 1.6-3mm PCB
5		Gnd
	8	
6		Sig
	8	
7		Gnd
	8	
8		Sig

8-layer

Layer	Spacing (mils)	
1		Sig
	8	
2		Gnd
	8	
3		Sig
	13 - 40.5	Depending on 1.6-3mm PCB
4		Gnd / HV
	5	
5		Gnd
	13 - 40.5	Depending on 1.6-3mm PCB
6		Sig
	8	
7		Gnd
	8	
8		Sig

10-layer

Layer	Spacing (mils)	
1		Sig
	8	
2		Gnd
	8	
3		Sig
	8	
4		Gnd
	5 - 32.5	Depending on 1.6-3mm PCB
5		HV
	5	
6		HV
	5 - 32.5	Depending on 1.6-3mm PCB
7		Gnd
	8	
8		Sig
	8	
9		Gnd
	8	
10		Sig

High Voltage – Block Diagram