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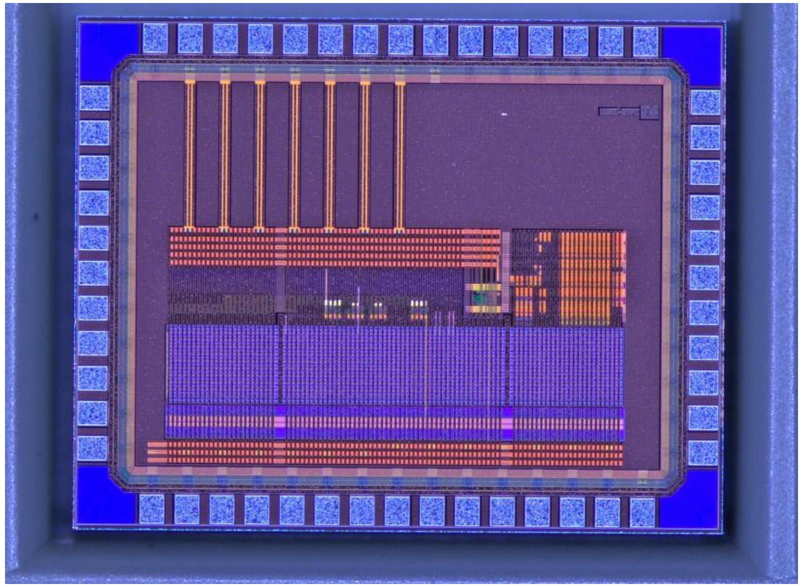
Overview and SLDO_5

Introduction

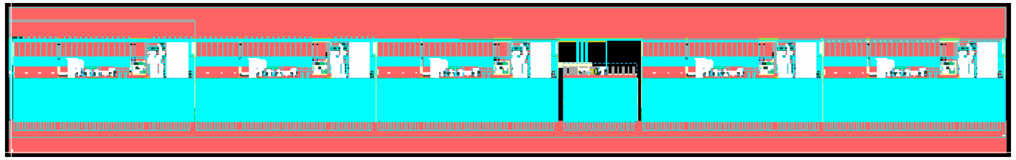


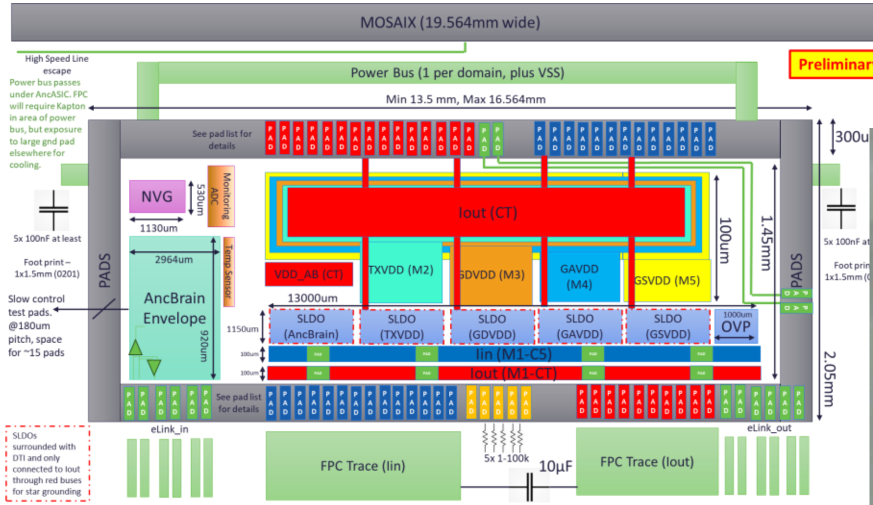
AncASIC Overview

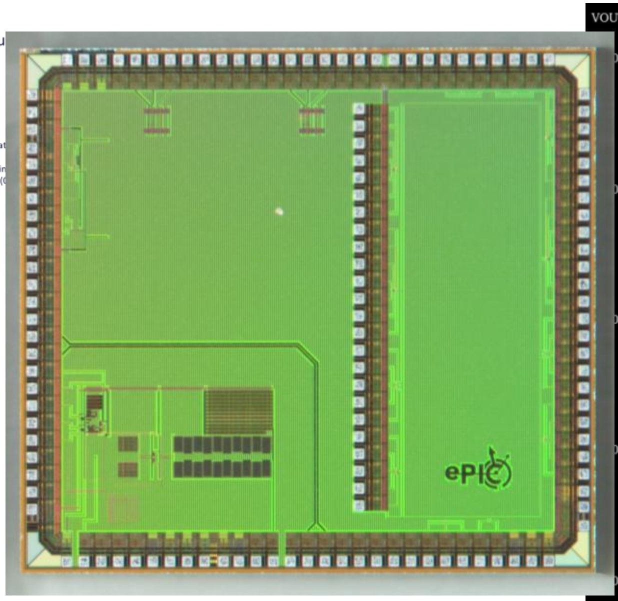
- Plan
- MPW1 (key block NVBG)
- MPW2 (key block SLDO)
- Software Mock-up Progress
- Chip Integration Progress

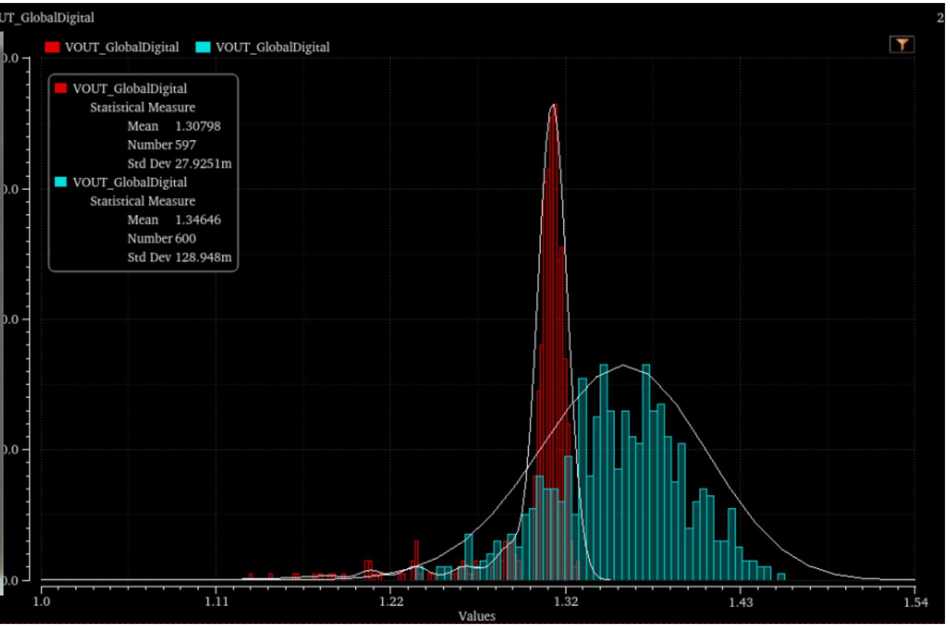
SLDO_5

- Overview
- Basic Operation
- Calibration
    - DAC Calibration
    - R3 Calibration
- Real World Operation









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AncASIC Overview

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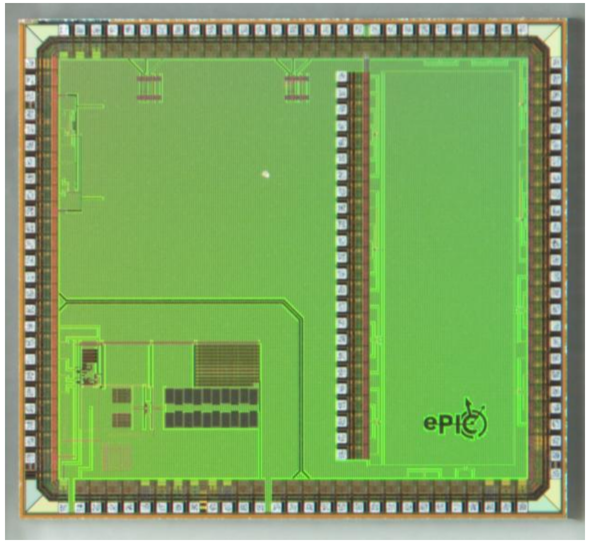
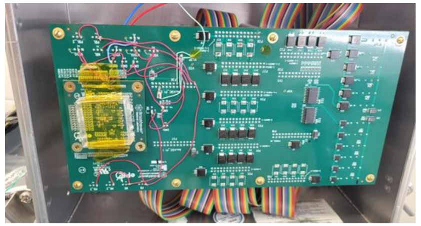
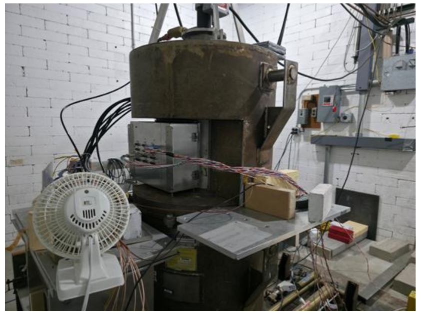
MPW1

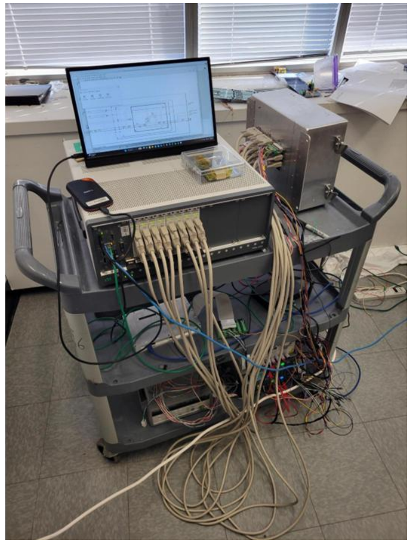
Summary

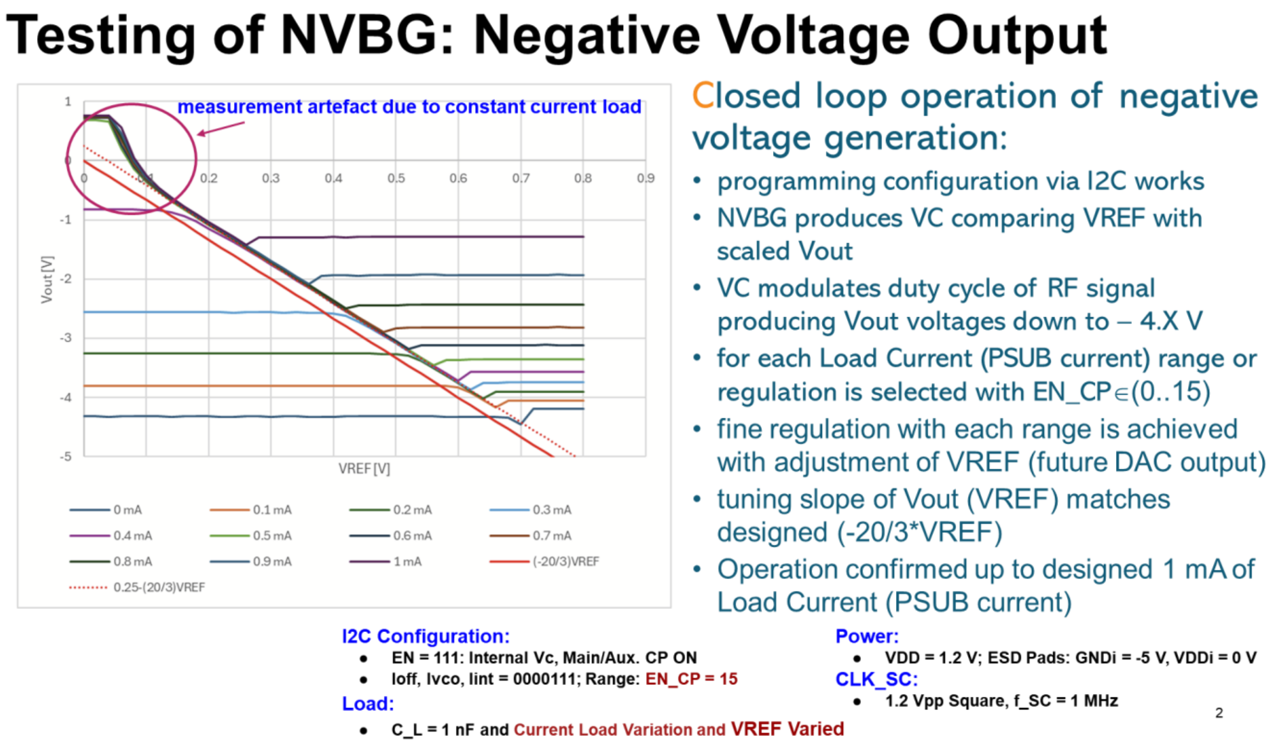
- Submitted a test structure containing the NVBG and various other test structures (transistors, digital I2C).
- Has returned and is in testing. Latest summary is here.
- Tested over a range of load currents up to 1mA design current. Functions as expected.
- Some changes may be needed to cope with higher than expected PSUB current of MOSAIX.
- Exploratory irradiations up to 3MRad, detailed irradiations ongoing.











Testing of NVBG: Negative Voltage Output

Closed loop operation of negative voltage generation:

- programming configuration via I2C works
- NVBG produces VC comparing VREF with scaled Vout
- VC modulates duty cycle of RF signal producing Vout voltages down to – 4.X V
- for each Load Current (PSUB current) range or regulation is selected with EN_CP∈(0..15)
- fine regulation with each range is achieved with adjustment of VREF (future DAC output)
- tuning slope of Vout (VREF) matches designed (-20/3*VREF)
- Operation confirmed up to designed 1 mA of Load Current (PSUB current)

I2C Configuration:
- EN = 111: Internal Vc, Main/Aux. CP ON
- Ioff, Ivco, Iint = 0000111; Range: EN_CP = 15

Load:
- C_L = 1 nF and Current Load Variation and VREF Varied

Power:
- VDD = 1.2 V; ESD Pads: GNDi = -5 V, VDDi = 0 V

CLK_SC:
- 1.2 Vpp Square, f_SC = 1 MHz

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MPW2

Summary

- Submitted a test structure containing a single SLDO.
- Has returned and is in testing. Latest summary is here.
- Tested over a range of load currents, temperatures and capacitances. Full set still to be completed.
- First serial chain constructed at Daresbury
- Everything functional so far
- Radiation tests planned, and more devices in bonding

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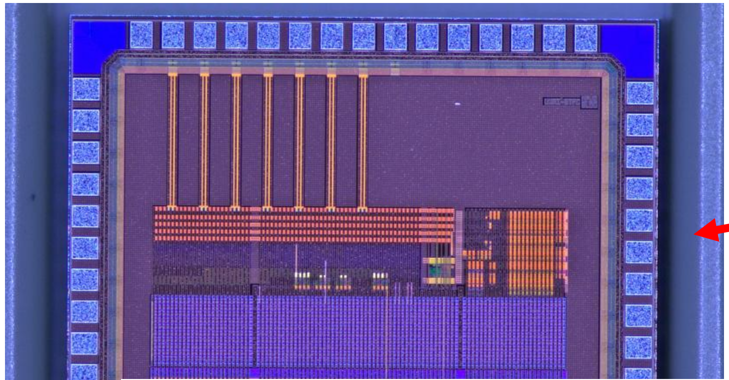
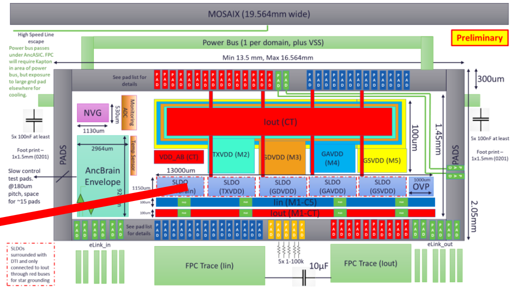
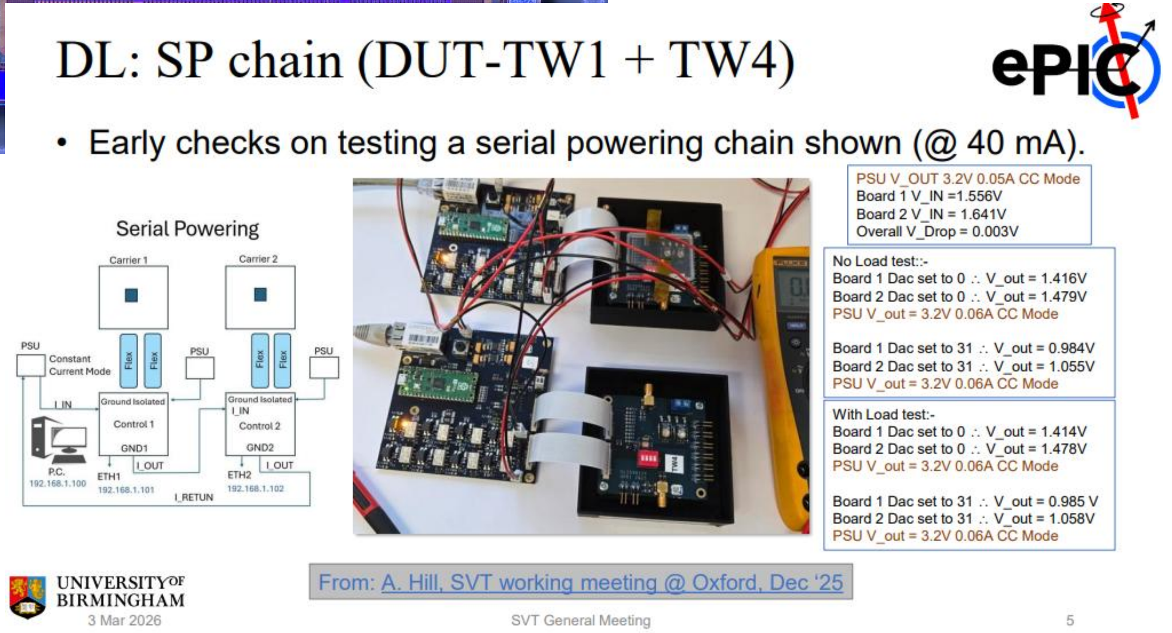






DL: SP chain (DUT-TW1 + TW4)

- Early checks on testing a serial powering chain shown (@ 40 mA).

PSU V_OUT 3.2V 0.05A CC Mode
Board 1 V_IN =1.556V
Board 2 V_IN = 1.641V
Overall V_Drop = 0.003V

No Load test:-
Board 1 Dac set to 0 ∴ V_out = 1.416V
Board 2 Dac set to 0 ∴ V_out = 1.479V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 ∴ V_out = 0.984V
Board 2 Dac set to 31 ∴ V_out = 1.055V
PSU V_out = 3.2V 0.06A CC Mode

With Load test:-
Board 1 Dac set to 0 ∴ V_out = 1.414V
Board 2 Dac set to 0 ∴ V_out = 1.478V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 ∴ V_out = 0.985 V
Board 2 Dac set to 31 ∴ V_out = 1.058V
PSU V_out = 3.2V 0.06A CC Mode

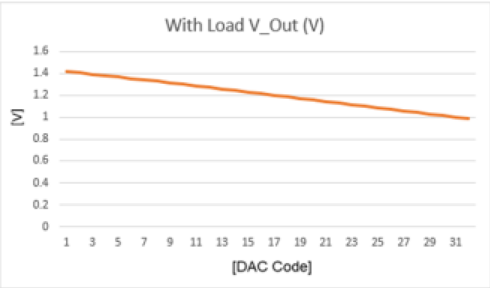
From: A. Hill, SVT working meeting @ Oxford, Dec '25

UNIVERSITY OF BIRMINGHAM
3 Mar 2026

SVT General Meeting

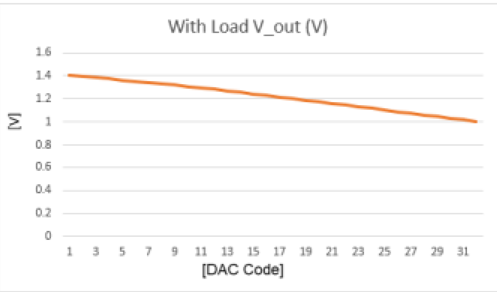
5

40 mA



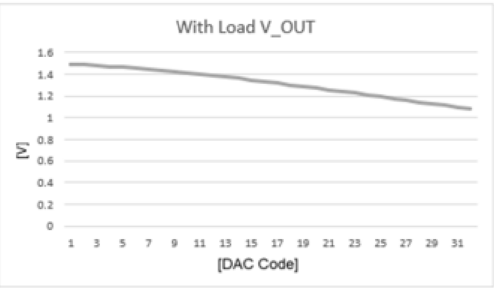
(V_in = 1.65 V)

500 mA



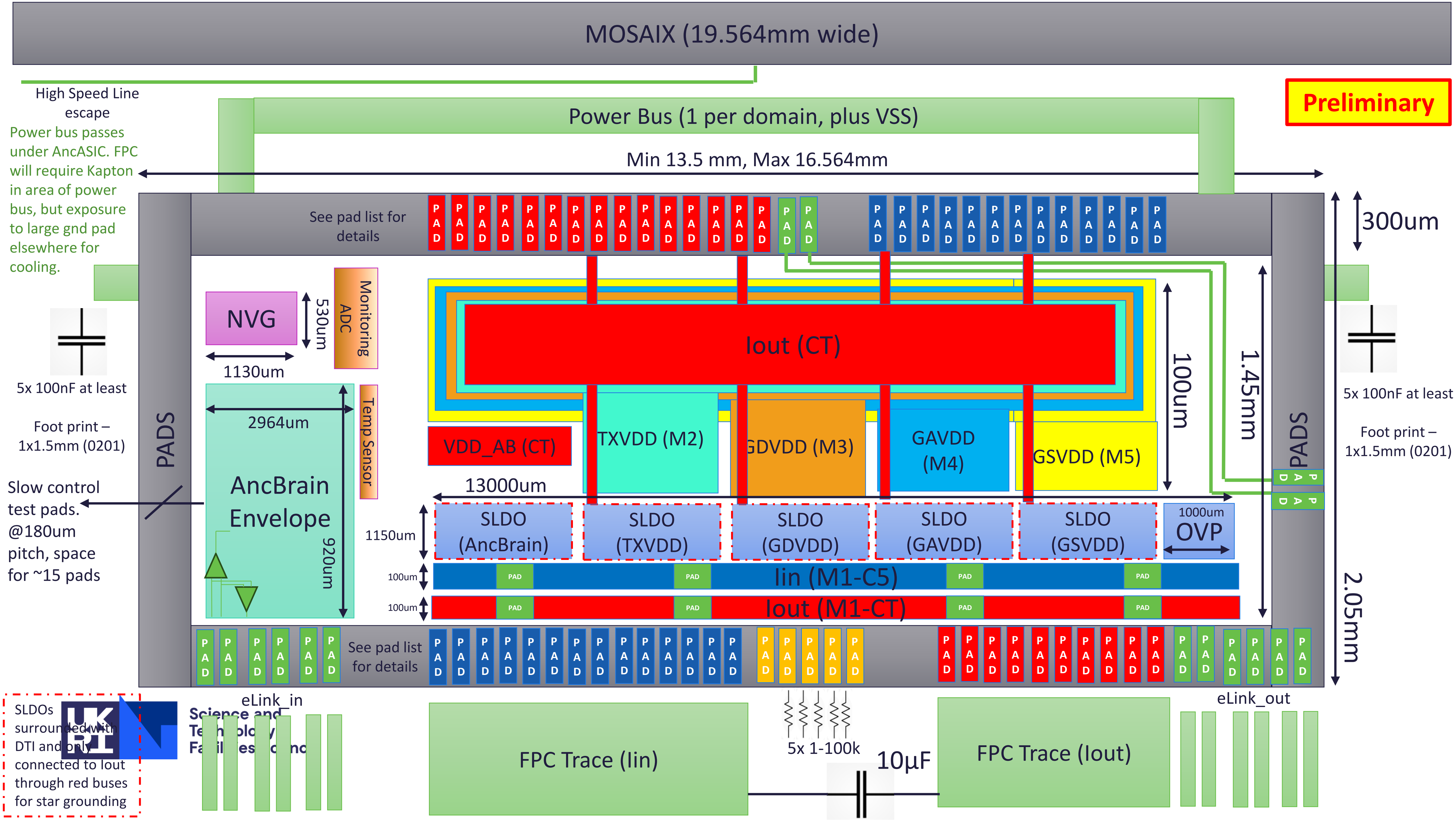
(V_in = 1.62 V)

900 mA



(V_in = 1.71 V)

Preliminary



MOSAIX (19.564mm wide)

High Speed Line escape

Power bus passes under AncASIC. FPC will require Kapton in area of power bus, but exposure to large gnd pad elsewhere for cooling.

Power Bus (1 per domain, plus VSS)

Min 13.5 mm, Max 16.564mm

5x 100nF at least

Foot print – 1x1.5mm (0201)

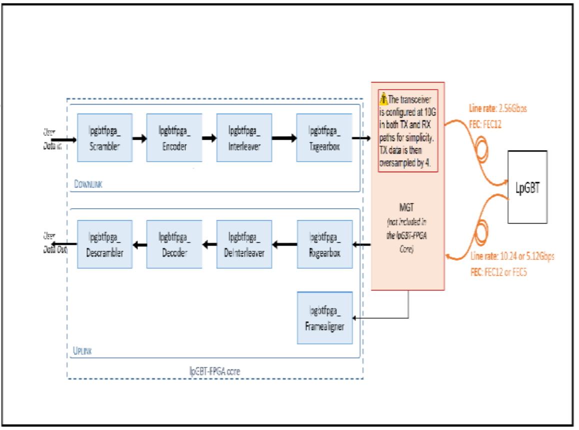
Slow control test pads. @180um pitch, space for ~15 pads

SLDOs surrounded with DTI and only connected to Iout through red buses for star grounding

AncASIC Overview

Software Mock-up Progress

- Detailed software mock-up currently in development
- Allows simulation of whole chain from control room to AncASIC
- Chain up to AncBrain tested and working. Adding the analogue sub-blocks (SLDO, NVG etc is currently in progress).



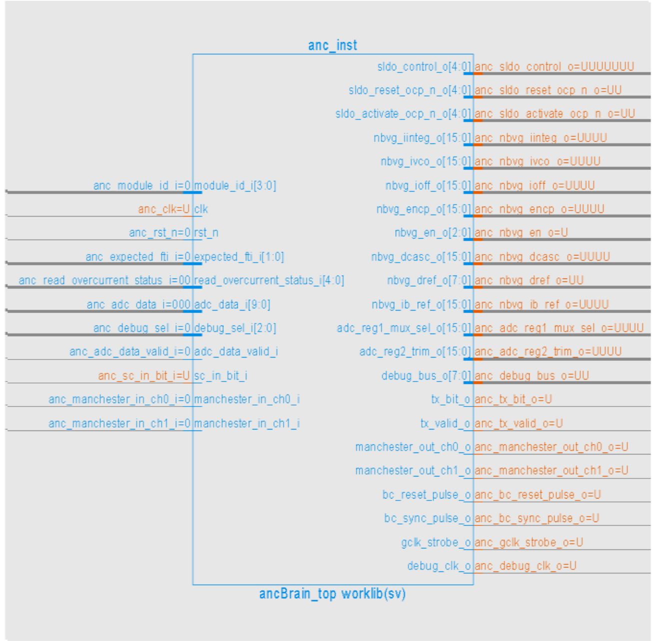
src: LpGBT-FPGA: Main Page

lpGBT-FPGA Core (version 2.2.0)

src: ASIC-DOE/lpgbt_model

The model was generated and tested with **XCELIUM 20.09.001**.

https://github.com/ASIC-DOE/AncBrain/tree/handoff_release



src: ASIC-DOE/AncBrain

In progress: VerilogA Models of sub-systems

Functional to this point

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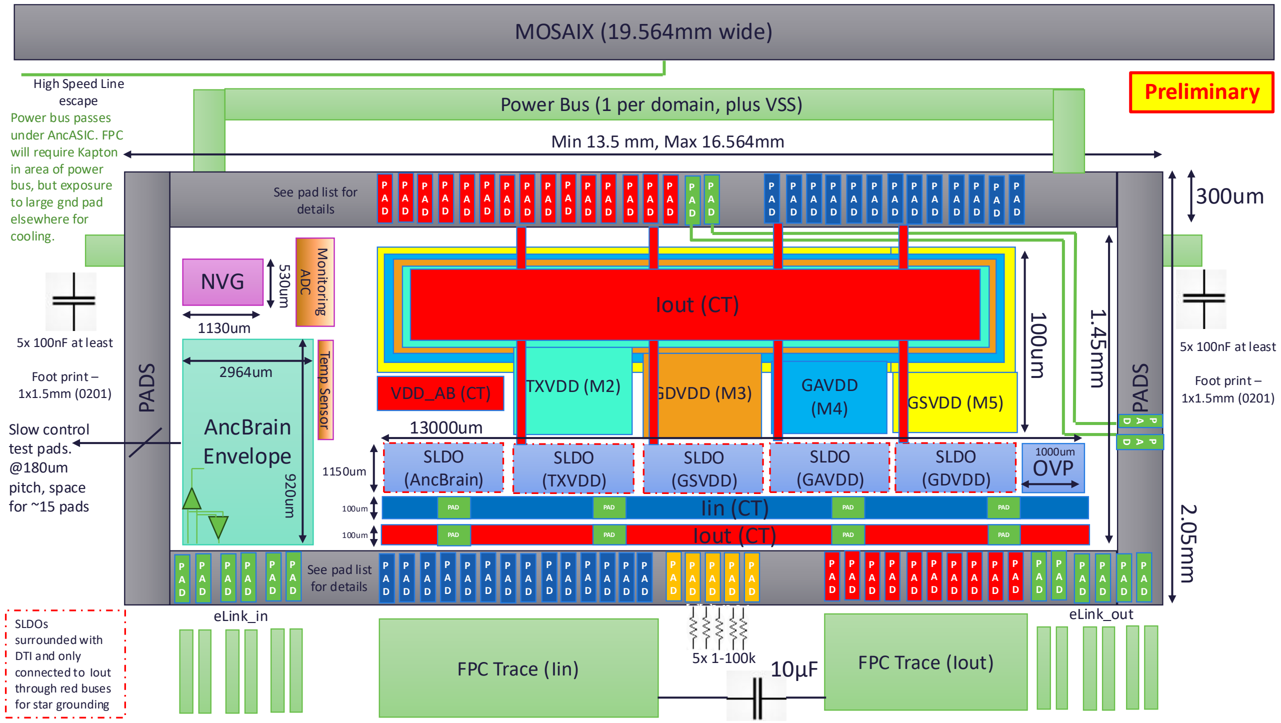
AncASIC Overview

Chip Integration Progress

- Blocks are complete (updates on most of them today)
- Integration underway at BNL
- Some technical and procurement delays
- Loss of UK effort unfortunate, but SLDO_5 complete and handed over
- Next available submission date is June



Block	Status
Pad-ring	• Preliminary PAD list ready. Work on the layout/integration can start as soon as pad list is finalized • Needs input on whether a different pad layout is required to help the FPC layout
SLDO	• A 5-SLDO super-block including OVP is complete • Need to perform DRC/LVS checks locally
NVG	• Design from AncASIC_P1 ready • DAC to set V_{REF} completed
AncBRAIN	• Feature set identified for May submission, RTL of those are also ready and simulated • Currently working on the physical implementation with the new LVT library
Monitoring ADC	• Layout is done. DRC/LVS clean with input capacitor and 16 inputs • Finalizing the protocol with AncBrain
Temperature Sensor	• Ready

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AncASIC Overview

Chip Integration

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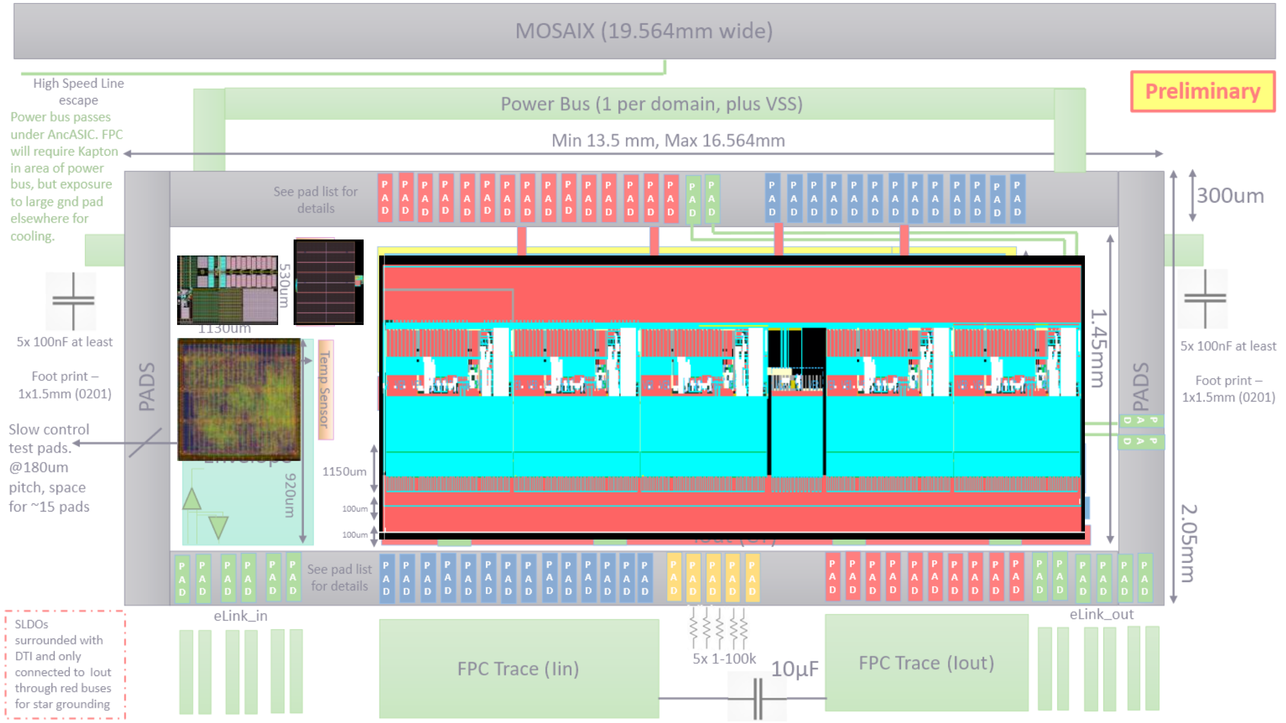

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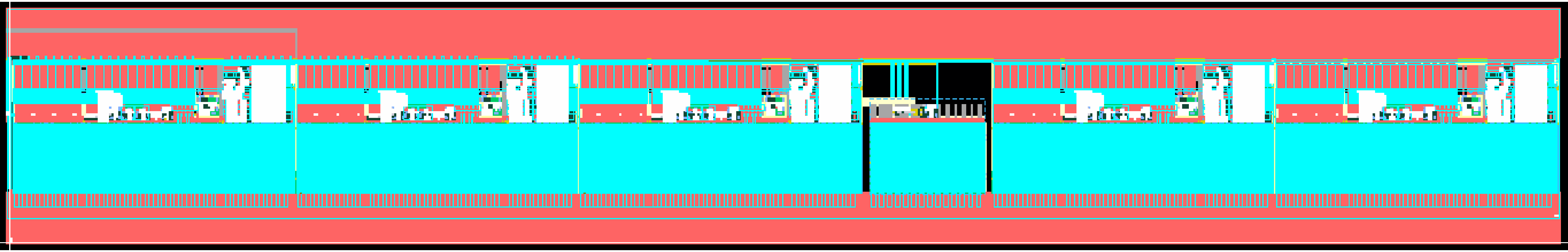
SLDO_5

5 SLDO Block

Background

- Need a block of 5 SLDOs and an OVP to meet the needs of the AncASIC
- Block complete and transferred to BNL for AncASIC integration
- Concentrating on detailed simulation
- Since this is a general meeting, won't show all those results, but focus on those that are particularly interesting or impact wider integration
- This skips **a lot** of detail – have moved those slides to backup



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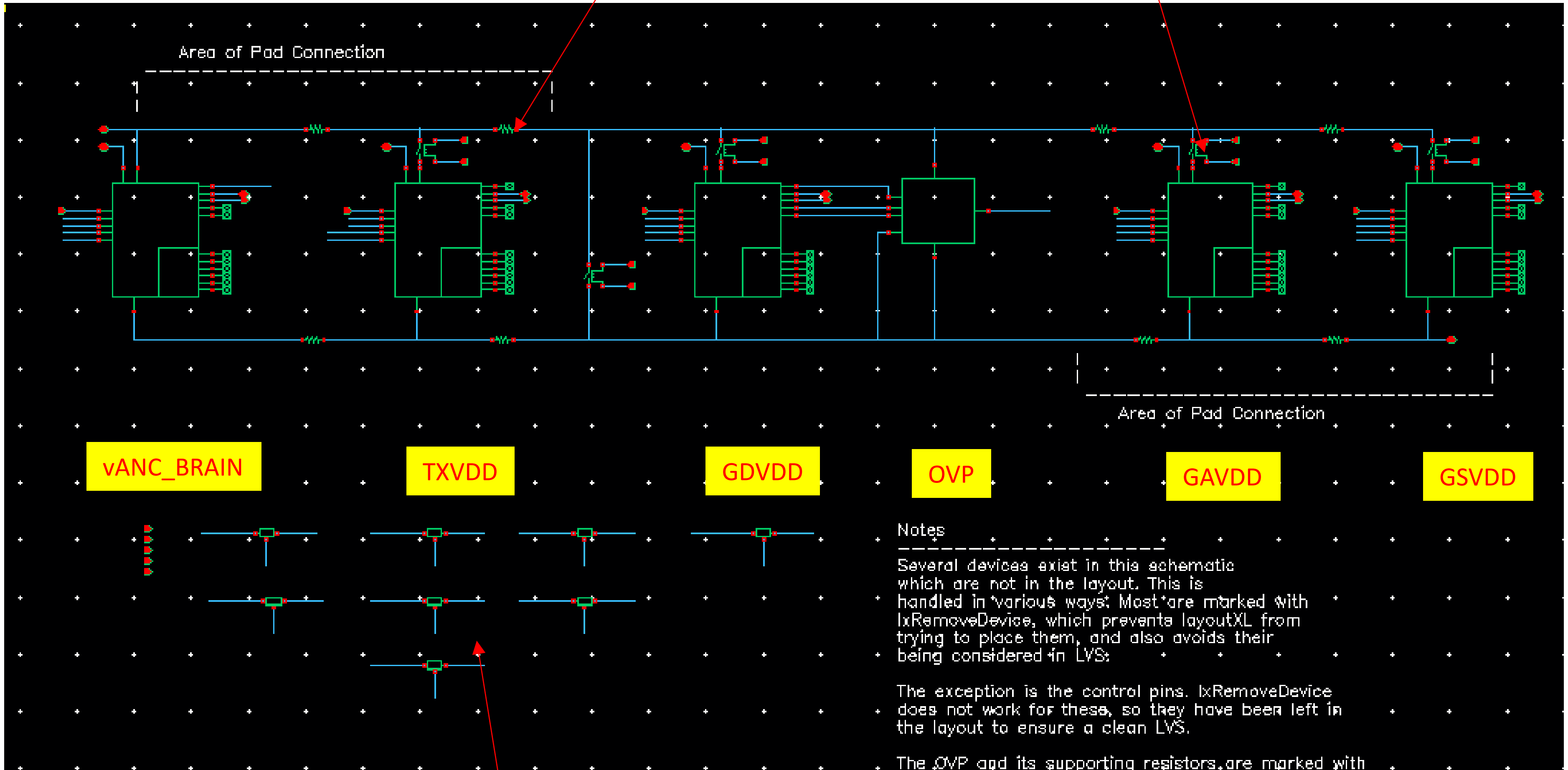
SLDO_5

Power Bus Resistances

Switches for failure testing

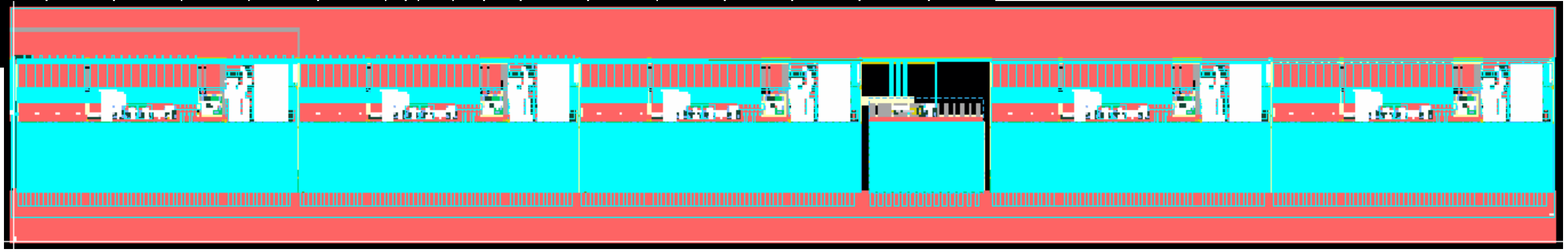


Notes

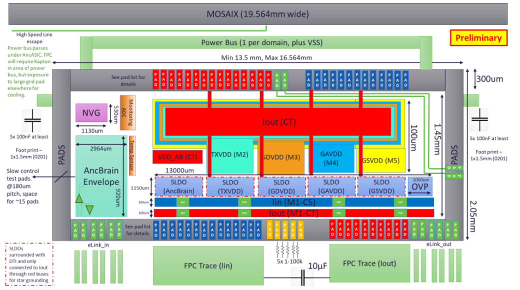
Several devices exist in this schematic which are not in the layout. This is handled in various ways. Most are marked with lxRemoveDevice, which prevents layoutXL from trying to place them, and also avoids their being considered in LVS.

The exception is the control pins. lxRemoveDevice does not work for these, so they have been left in the layout to ensure a clean LVS.

The OVP and its supporting resistors are marked with



Pull resistors for defaults



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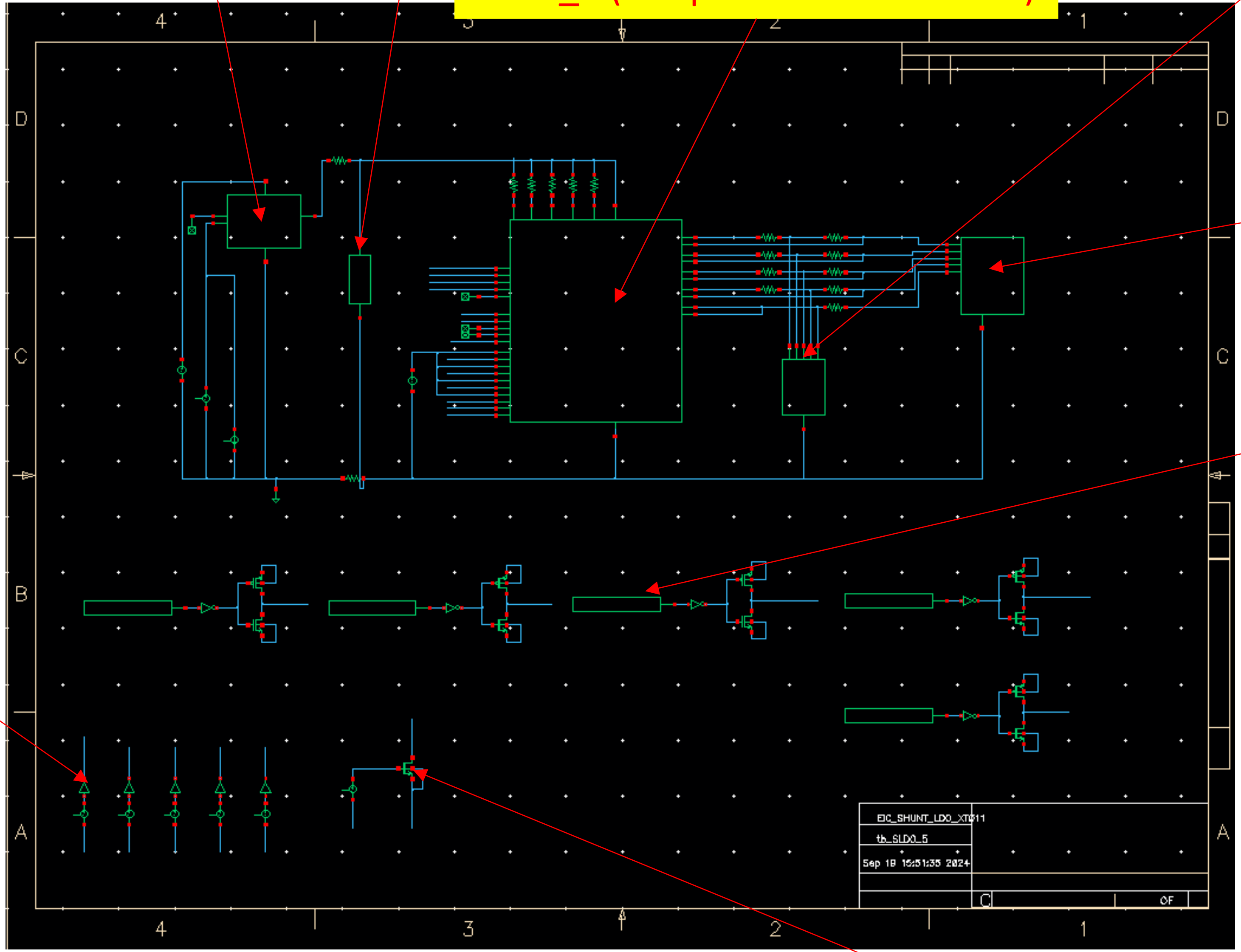
Testbench



Current source

Decoupling

SLDO_5 (inc. pads and bondwires)

Decoupling

Load

DAC Controls

Reset_OCP_N
and
activate_OCP_N

Load Overcurrent

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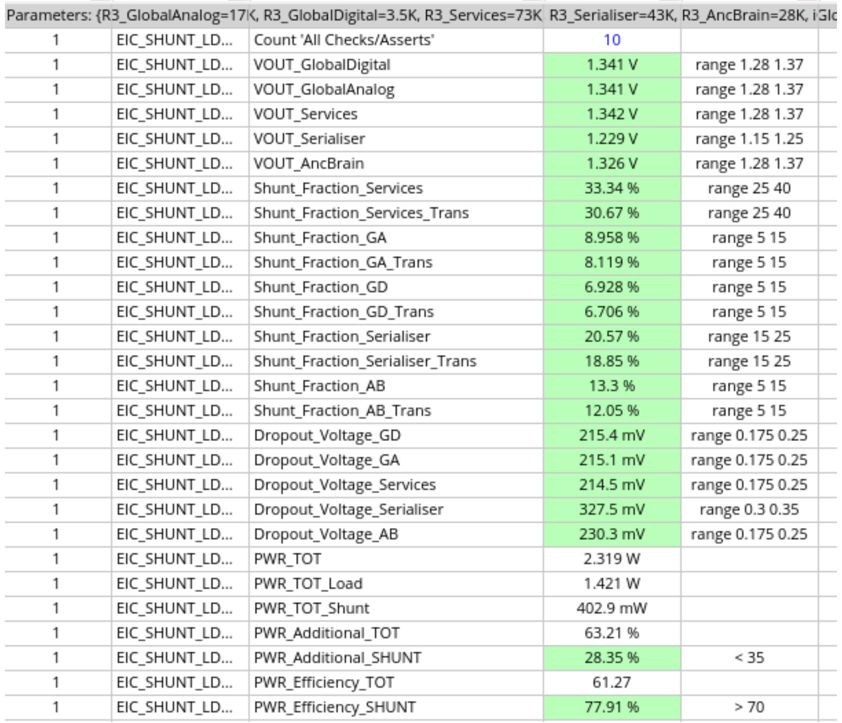
SLDO_5

Basic Operation

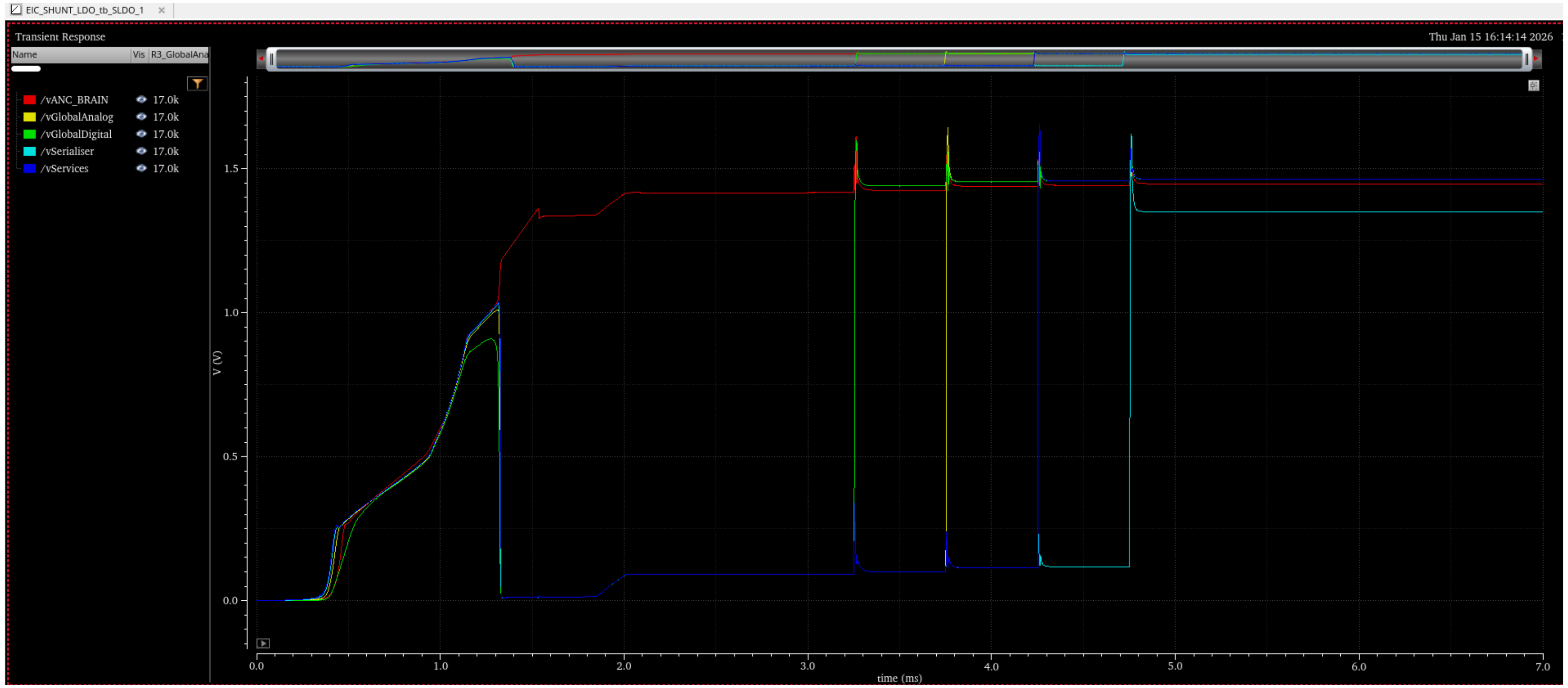
Basic Operation

Example

- Shows the SLDO_5 block operating in intended default mode – AncBrain enabled at startup, others disabled
- Simulation includes target specs used to evaluate performance in large runs



Parameters: {R3_GlobalAnalog=17K, R3_GlobalDigital=3.5K, R3_Services=73K, R3_Serialiser=43K, R3_AncBrain=28K, iGlc				
1	EIC_SHUNT_LD...	Count 'All Checks/Asserts'	10	
1	EIC_SHUNT_LD...	VOUT_GlobalDigital	1.341 V	range 1.28 1.37
1	EIC_SHUNT_LD...	VOUT_GlobalAnalog	1.341 V	range 1.28 1.37
1	EIC_SHUNT_LD...	VOUT_Services	1.342 V	range 1.28 1.37
1	EIC_SHUNT_LD...	VOUT_Serialiser	1.229 V	range 1.15 1.25
1	EIC_SHUNT_LD...	VOUT_AncBrain	1.326 V	range 1.28 1.37
1	EIC_SHUNT_LD...	Shunt_Fraction_Services	33.34 %	range 25 40
1	EIC_SHUNT_LD...	Shunt_Fraction_Services_Trans	30.67 %	range 25 40
1	EIC_SHUNT_LD...	Shunt_Fraction_GA	8.958 %	range 5 15
1	EIC_SHUNT_LD...	Shunt_Fraction_GA_Trans	8.119 %	range 5 15
1	EIC_SHUNT_LD...	Shunt_Fraction_GD	6.928 %	range 5 15
1	EIC_SHUNT_LD...	Shunt_Fraction_GD_Trans	6.706 %	range 5 15
1	EIC_SHUNT_LD...	Shunt_Fraction_Serialiser	20.57 %	range 15 25
1	EIC_SHUNT_LD...	Shunt_Fraction_Serialiser_Trans	18.85 %	range 15 25
1	EIC_SHUNT_LD...	Shunt_Fraction_AB	13.3 %	range 5 15
1	EIC_SHUNT_LD...	Shunt_Fraction_AB_Trans	12.05 %	range 5 15
1	EIC_SHUNT_LD...	Dropout_Voltage_GD	215.4 mV	range 0.175 0.25
1	EIC_SHUNT_LD...	Dropout_Voltage_GA	215.1 mV	range 0.175 0.25
1	EIC_SHUNT_LD...	Dropout_Voltage_Services	214.5 mV	range 0.175 0.25
1	EIC_SHUNT_LD...	Dropout_Voltage_Serialiser	327.5 mV	range 0.3 0.35
1	EIC_SHUNT_LD...	Dropout_Voltage_AB	230.3 mV	range 0.175 0.25
1	EIC_SHUNT_LD...	PWR_TOT	2.319 W	
1	EIC_SHUNT_LD...	PWR_TOT_Load	1.421 W	
1	EIC_SHUNT_LD...	PWR_TOT_Shunt	402.9 mW	
1	EIC_SHUNT_LD...	PWR_Additional_TOT	63.21 %	
1	EIC_SHUNT_LD...	PWR_Additional_SHUNT	28.35 %	< 35
1	EIC_SHUNT_LD...	PWR_Efficiency_TOT	61.27	
1	EIC_SHUNT_LD...	PWR_Efficiency_SHUNT	77.91 %	> 70

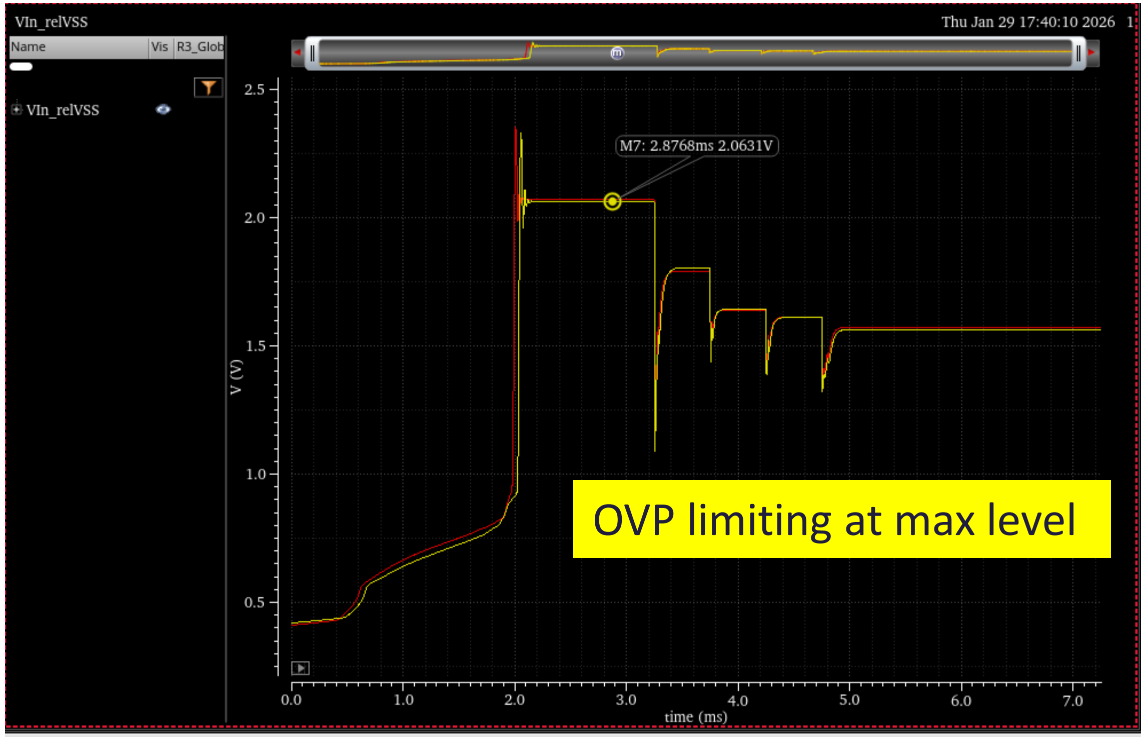


Many, many more detailed results in the backup slides. To be presented in full at a later WP1 meeting

Basic Operation

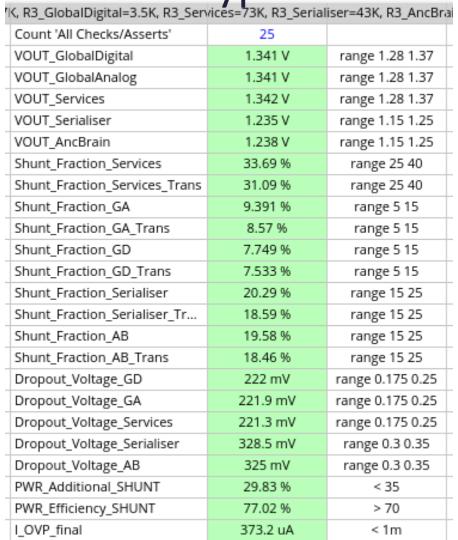
Default Levels

- To check the internal pull up/downs, disconnect the driving control signals



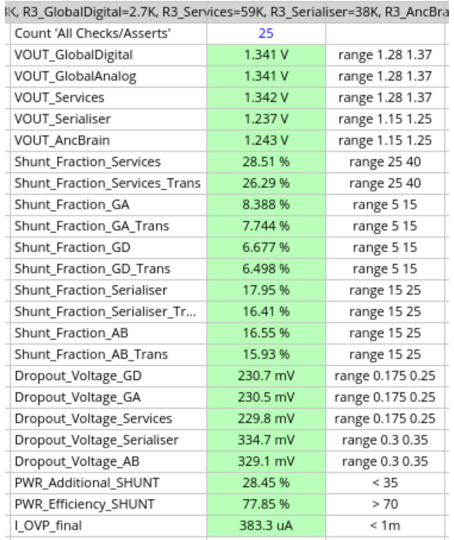
OVP limiting at max level

Typ

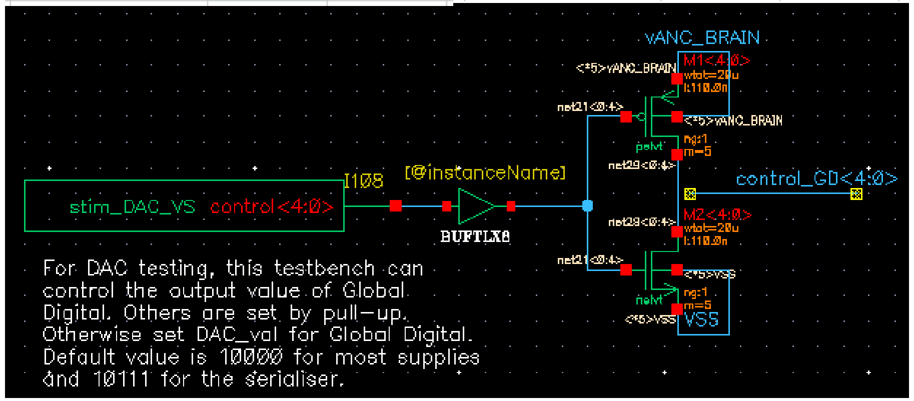


K, R3_GlobalDigital=3.5K, R3_Services=73K, R3_Serialiser=43K, R3_AncBrai		
Count 'All Checks/Asserts'	25	
VOUT_GlobalDigital	1.341 V	range 1.28 1.37
VOUT_GlobalAnalog	1.341 V	range 1.28 1.37
VOUT_Services	1.342 V	range 1.28 1.37
VOUT_Serialiser	1.235 V	range 1.15 1.25
VOUT_AncBrain	1.238 V	range 1.15 1.25
Shunt_Fraction_Services	33.69 %	range 25 40
Shunt_Fraction_Services_Trans	31.09 %	range 25 40
Shunt_Fraction_GA	9.391 %	range 5 15
Shunt_Fraction_GA_Trans	8.57 %	range 5 15
Shunt_Fraction_GD	7.749 %	range 5 15
Shunt_Fraction_GD_Trans	7.533 %	range 5 15
Shunt_Fraction_Serialiser	20.29 %	range 15 25
Shunt_Fraction_Serialiser_Tr...	18.59 %	range 15 25
Shunt_Fraction_AB	19.58 %	range 15 25
Shunt_Fraction_AB_Trans	18.46 %	range 15 25
Dropout_Voltage_GD	222 mV	range 0.175 0.25
Dropout_Voltage_GA	221.9 mV	range 0.175 0.25
Dropout_Voltage_Services	221.3 mV	range 0.175 0.25
Dropout_Voltage_Serialiser	328.5 mV	range 0.3 0.35
Dropout_Voltage_AB	325 mV	range 0.3 0.35
PWR_Additional_SHUNT	29.83 %	< 35
PWR_Efficiency_SHUNT	77.02 %	> 70
I_OVP_final	373.2 uA	< 1m

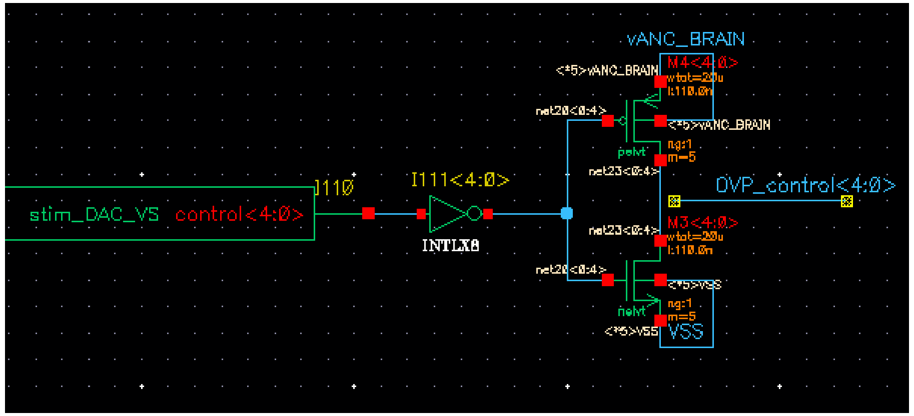
Max



K, R3_GlobalDigital=2.7K, R3_Services=59K, R3_Serialiser=38K, R3_AncBra		
Count 'All Checks/Asserts'	25	
VOUT_GlobalDigital	1.341 V	range 1.28 1.37
VOUT_GlobalAnalog	1.341 V	range 1.28 1.37
VOUT_Services	1.342 V	range 1.28 1.37
VOUT_Serialiser	1.237 V	range 1.15 1.25
VOUT_AncBrain	1.243 V	range 1.15 1.25
Shunt_Fraction_Services	28.51 %	range 25 40
Shunt_Fraction_Services_Trans	26.29 %	range 25 40
Shunt_Fraction_GA	8.388 %	range 5 15
Shunt_Fraction_GA_Trans	7.744 %	range 5 15
Shunt_Fraction_GD	6.677 %	range 5 15
Shunt_Fraction_GD_Trans	6.498 %	range 5 15
Shunt_Fraction_Serialiser	17.95 %	range 15 25
Shunt_Fraction_Serialiser_Tr...	16.41 %	range 15 25
Shunt_Fraction_AB	16.55 %	range 15 25
Shunt_Fraction_AB_Trans	15.93 %	range 15 25
Dropout_Voltage_GD	230.7 mV	range 0.175 0.25
Dropout_Voltage_GA	230.5 mV	range 0.175 0.25
Dropout_Voltage_Services	229.8 mV	range 0.175 0.25
Dropout_Voltage_Serialiser	334.7 mV	range 0.3 0.35
Dropout_Voltage_AB	329.1 mV	range 0.3 0.35
PWR_Additional_SHUNT	28.45 %	< 35
PWR_Efficiency_SHUNT	77.85 %	> 70
I_OVP_final	383.3 uA	< 1m



For DAC testing, this testbench can control the output value of Global Digital. Others are set by pull-up. Otherwise set DAC_val for Global Digital. Default value is 10000 for most supplies and 10111 for the serialiser.



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SLDO_5

Calibration

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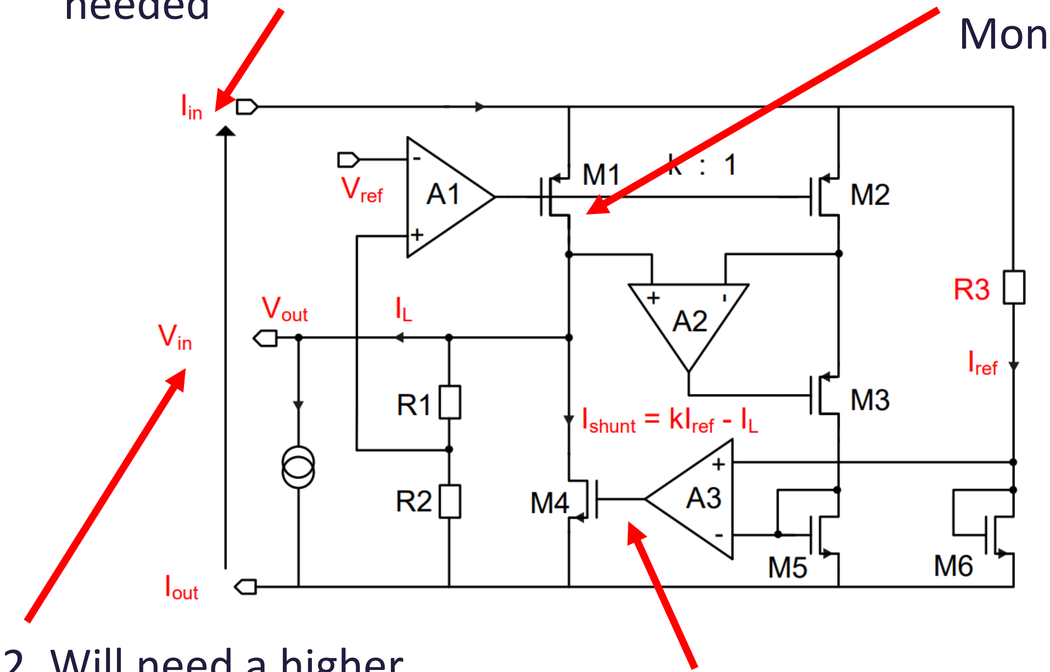
Calibration

Background

- Performance varies due to manufacturing variation
- Requires tuning of the DAC to get the correct voltage
- Effective resistance of the SLDO also varies, and need to calibrate R3 to compensate
- Then need to set suitable OVP level
- Could just set these last two high enough to cover all cases, but would lead to low efficiency and high voltage stress



1. For example, rd increases due to Monte Carlo

2. Will need a higher Vin to sustain same Vout

3. Or, higher gm leads to more shunted current

4. Higher current needed

Calibration

DAC Calibration

- Certain Monte Carlo runs lead to non-linear DAC responses

- This is throwing off the calibration, which assumes a linear response 0 -> 31 (dashed line is the extracted slope)

- Several options
  - Increase voltage to linearise
    - Unnecessary and would probably cause other issues
  - Non-linear calibration
    - Too complicated
  - Take calibration points at 0 and 16
    - Not accurate
  - Multi-linear (0,16,31)
    - Least worst option

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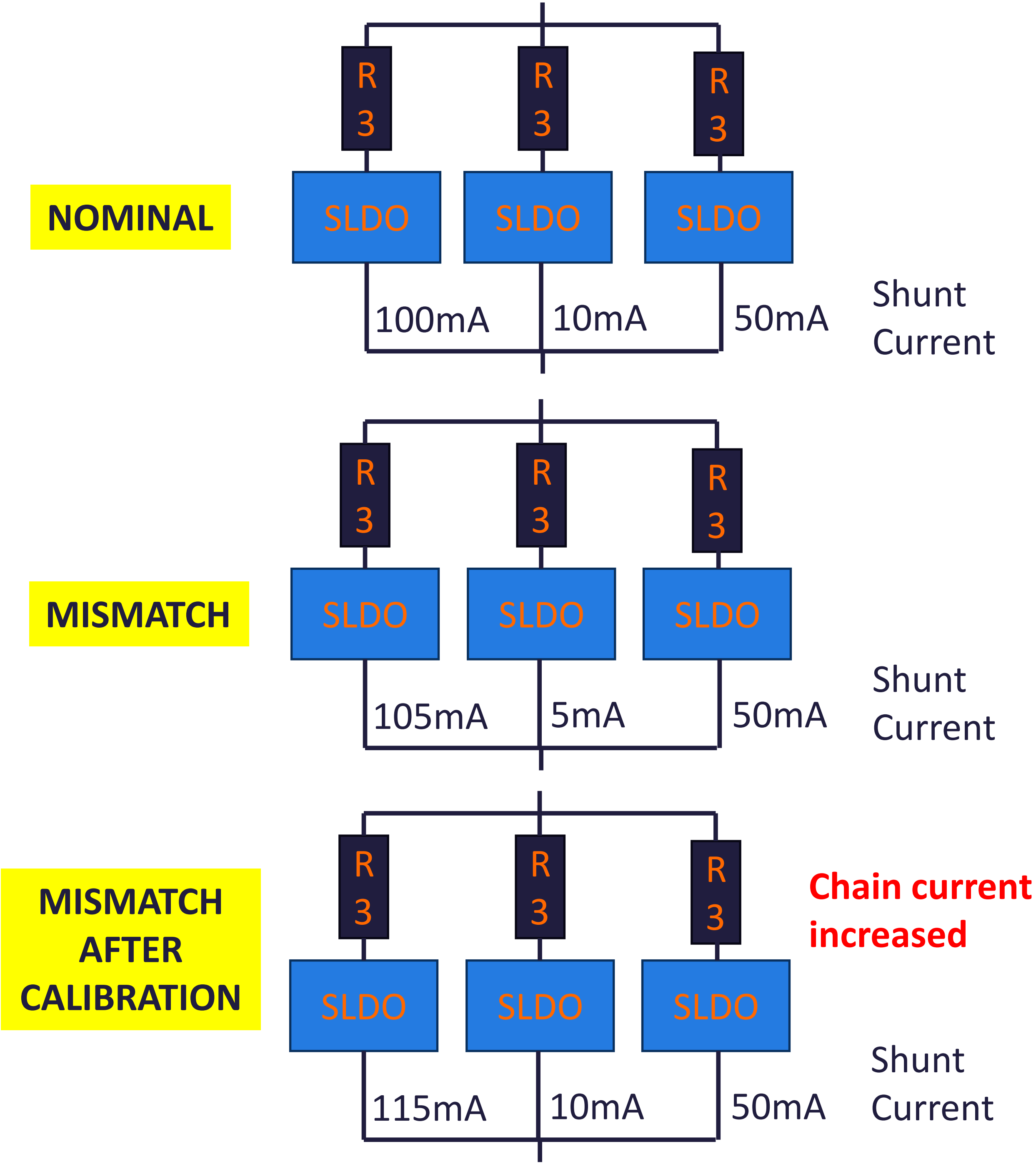
Calibration

R3 Calibration

- Variation in SLDO can lead to change in effective resistance. This leads to non-ideal current split.
- In Mode 1, this can mean the shunt percentage falling below the target 10%. In Mode 0, it can lead to SLDO shut down, because the shunt current falls below the ~10mA minimum used to detect a load overcurrent.
- This can be solved by increasing the chain current, but this leads to high inefficiency
- It is more efficient to tune R3 to compensate



Calibration

Procedure

- With these constraints in mind, proposed (and simulated) calibration procedure is:

1. Calibrate DAC
    1. Set OVP limit and chain current to high values
    2. Measure values at 0, 15 and 31 Determine code needed for target output voltage

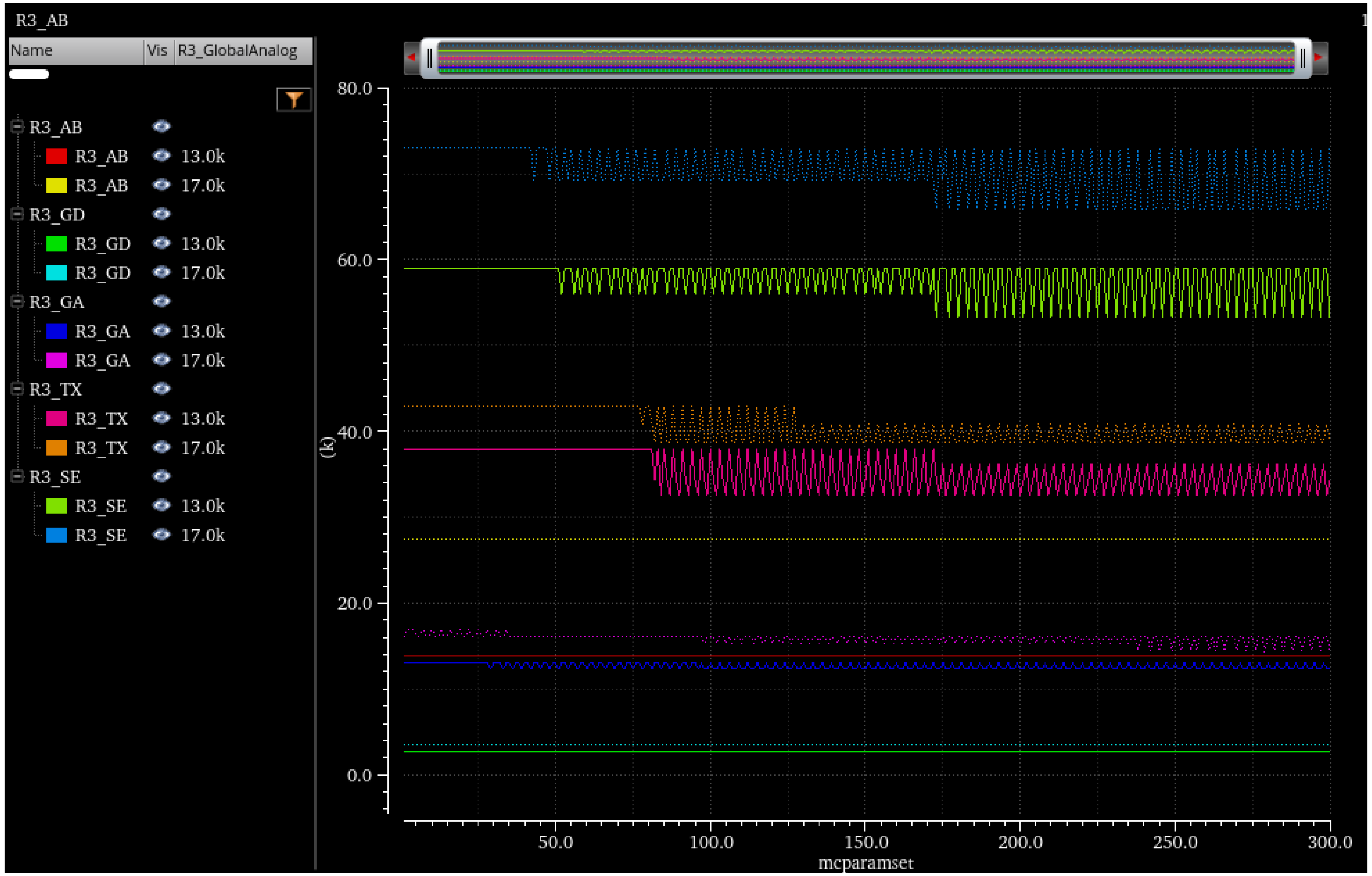
2. Determine required R3 value
    1. Set current to default
    2. Check that all SLDOs have started up (in practice, that their voltage exceeds 1V)
    3. For any supply that does not start, decrease its R3 by 5%

3. Determine required OVP level
    1. Set level to default
    2. Check that output voltages same as previous step and OVP off
    3. Increase OVP limit

Monte Carlo

Resulting R3 Values

- Plot shows R3 after calibration for many Monte Carlo iterations
- Solid: EIC-LAS Max
- Dashed: EIC-LAS Typ
- Note there is a range of R3 values from calibration, but **also a larger range based on the LAS current**.
- Calibrating R3 could be done at AncASIC wafer probe. **However, how to determine R3 to match the LAS current, which may also vary?**



R3_AB

Name	Vis	R3_GlobalAnalog
R3_AB	👁	
🟥 R3_AB	👁	13.0k
🟨 R3_AB	👁	17.0k
R3_GD	👁	
🟩 R3_GD	👁	13.0k
🟦 R3_GD	👁	17.0k
R3_GA	👁	
🟦 R3_GA	👁	13.0k
🟪 R3_GA	👁	17.0k
R3_TX	👁	
🟪 R3_TX	👁	13.0k
🟧 R3_TX	👁	17.0k
R3_SE	👁	
🟩 R3_SE	👁	13.0k
🟦 R3_SE	👁	17.0k

Thoughts on calibration:

- Re-calibrate R3 at module test – **would need R3 to remain variable at this stage**
- Wafer probe all LAS to get supply current, then wafer probe AncASIC with correct load current to set correct R3 based on both variables – **individual LAS and AncASIC pairs would then exist**.
- Perhaps LAS current variation will not be as extreme as shown here and may not be an issue
- Assume R3 will need to handle max case – **heavily reduced efficiency**

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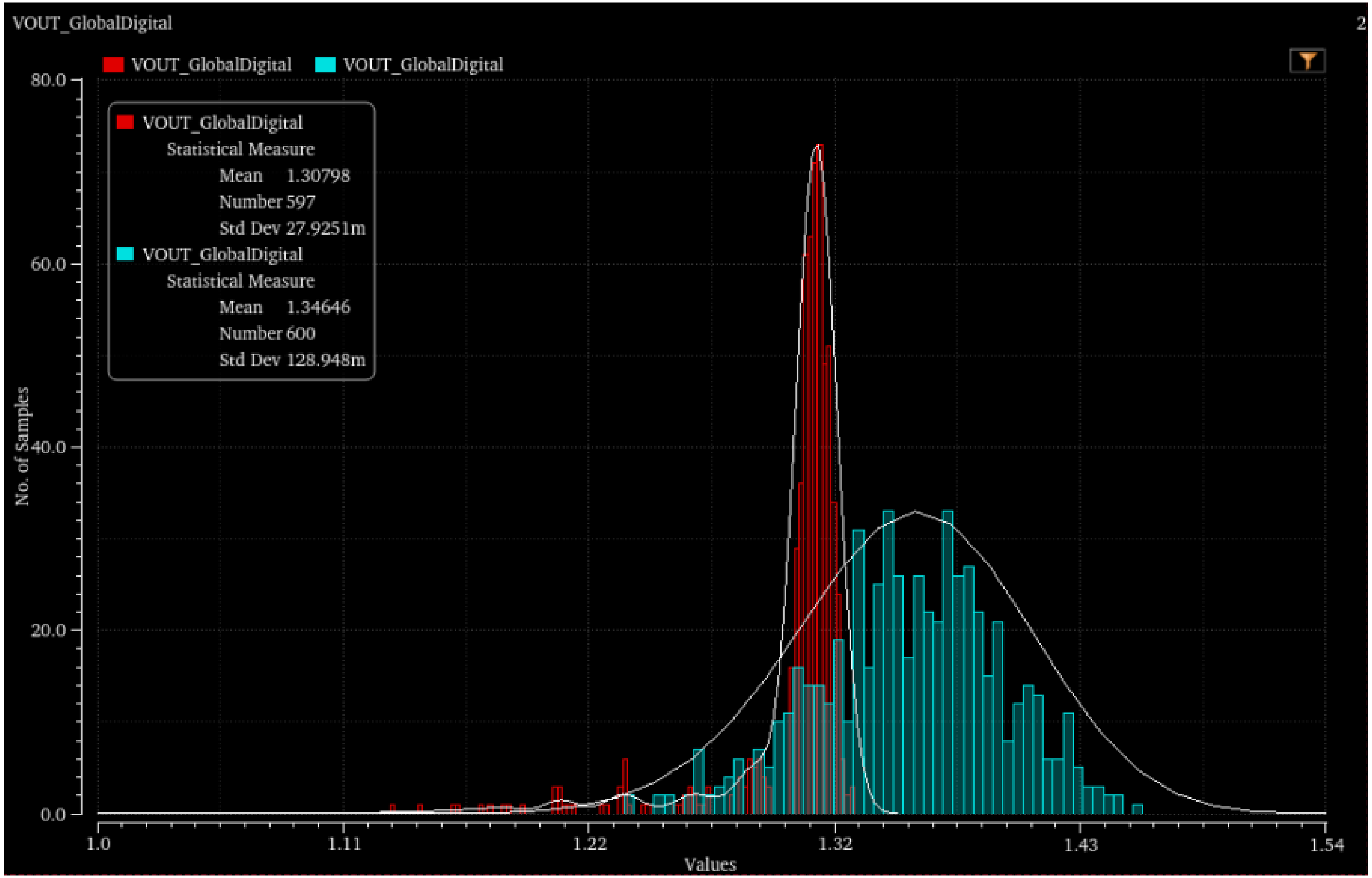
Calibration

Output Voltage Spread

- Just an example to prove calibration is worth it…
- Compare GDVDD uncalibrated (blue) with calibrated (red)
- 5x reduction in standard deviation



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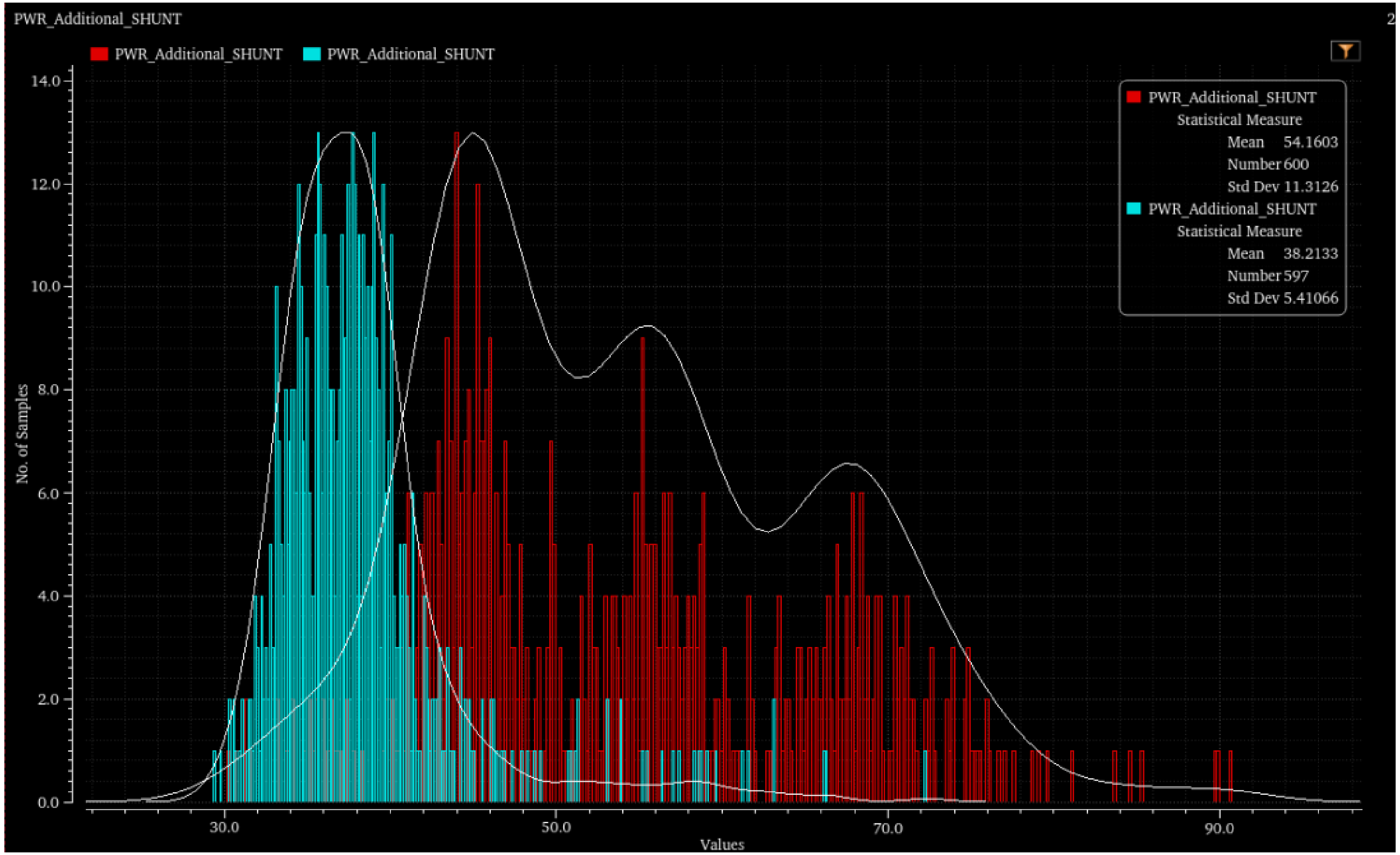
Calibration

Efficiency – Results

- Compare efficiency using an iChain based calibration (red) to an R3 based calibration (blue)
- Results are now significantly better, and more in line with MPW2 corner simulations
- Key points are:
    - R3 calibration
    - Current boost in startup (see backup)



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SLDO_5

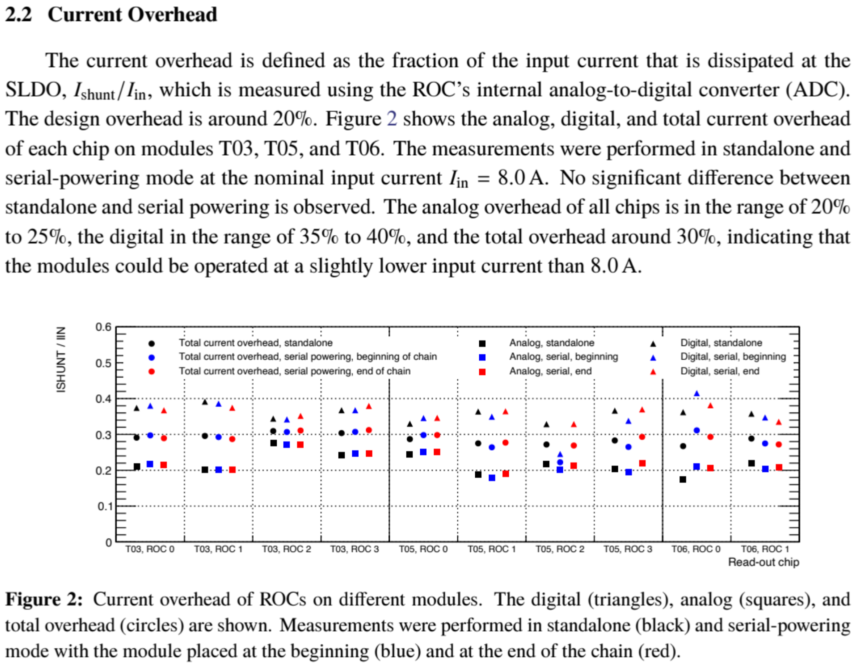
Real World Operation

Real World Operation

Papers from CMS and ATLAS

- The relationship between current distribution, required headroom and efficiency is now discussed in several papers

Performance of Phase-2 CMS Inner Tracker CROC-V1 modules in a serial power chain

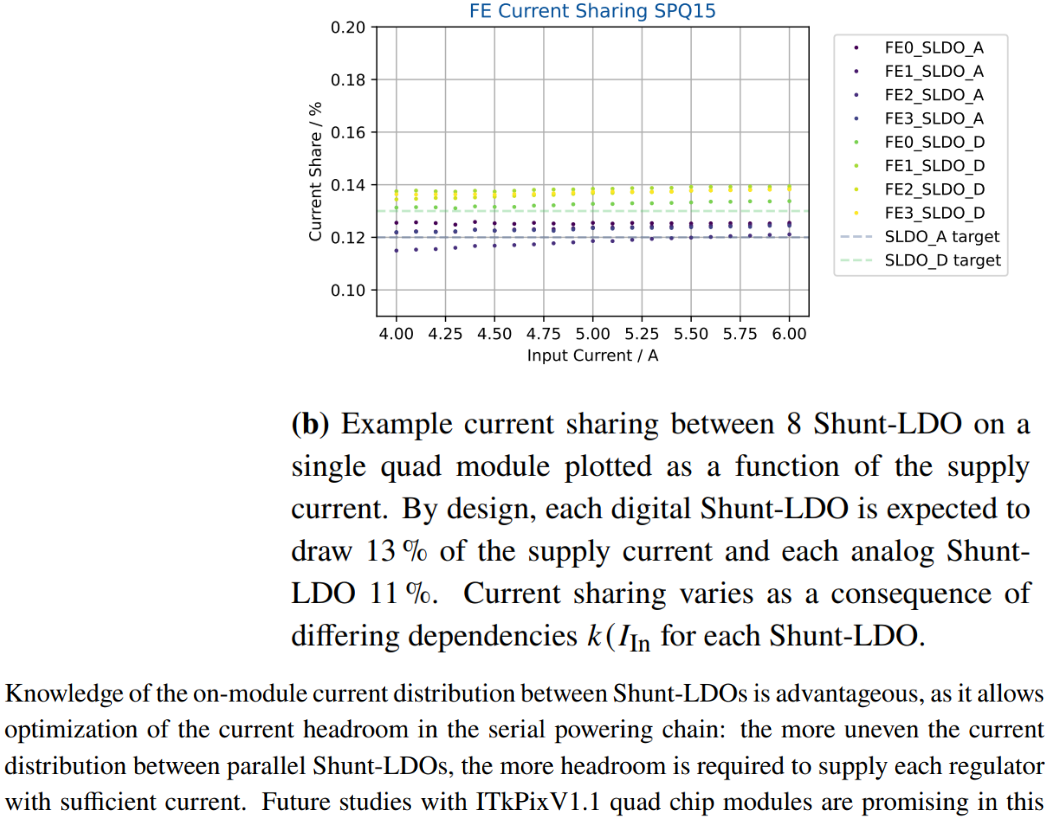


2.2 Current Overhead

The current overhead is defined as the fraction of the input current that is dissipated at the SLDO, $I_{\text{shunt}}/I_{\text{in}}$, which is measured using the ROC's internal analog-to-digital converter (ADC). The design overhead is around 20%. Figure 2 shows the analog, digital, and total current overhead of each chip on modules T03, T05, and T06. The measurements were performed in standalone and serial-powering mode at the nominal input current $I_{\text{in}} = 8.0$ A. No significant difference between standalone and serial powering is observed. The analog overhead of all chips is in the range of 20% to 25%, the digital in the range of 35% to 40%, and the total overhead around 30%, indicating that the modules could be operated at a slightly lower input current than 8.0 A.

Figure 2: Current overhead of ROCs on different modules. The digital (triangles), analog (squares), and total overhead (circles) are shown. Measurements were performed in standalone (black) and serial-powering mode with the module placed at the beginning (blue) and at the end of the chain (red).

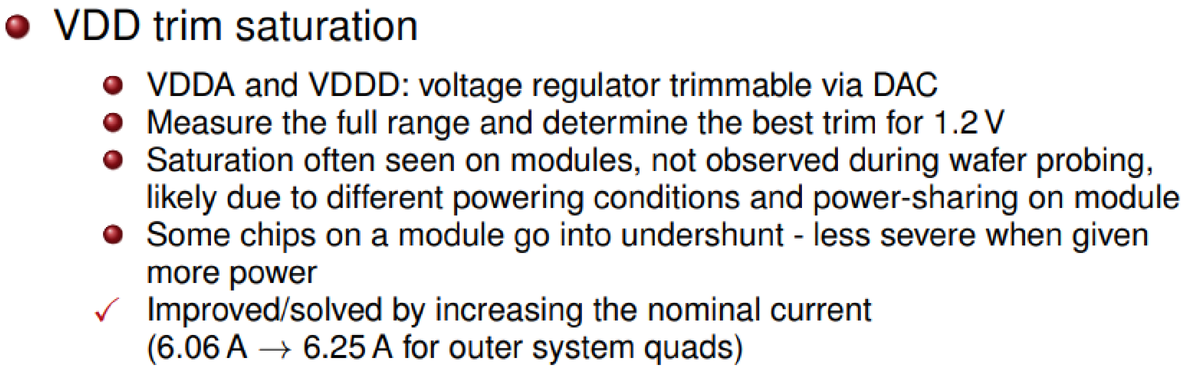
Prototyping Serial Powering with RD53A and ITkPixV1.1



(b) Example current sharing between 8 Shunt-LDO on a single quad module plotted as a function of the supply current. By design, each digital Shunt-LDO is expected to draw 13 % of the supply current and each analog Shunt-LDO 11 %. Current sharing varies as a consequence of differing dependencies $k(I_{\text{In}}$ for each Shunt-LDO.

Knowledge of the on-module current distribution between Shunt-LDOs is advantageous, as it allows optimization of the current headroom in the serial powering chain: the more uneven the current distribution between parallel Shunt-LDOs, the more headroom is required to supply each regulator with sufficient current. Future studies with ITkPixV1.1 quad chip modules are promising in this

Electrical QC Testing of Pixel Modules in the ATLAS Inner Tracker Upgrade for the HL-LHC

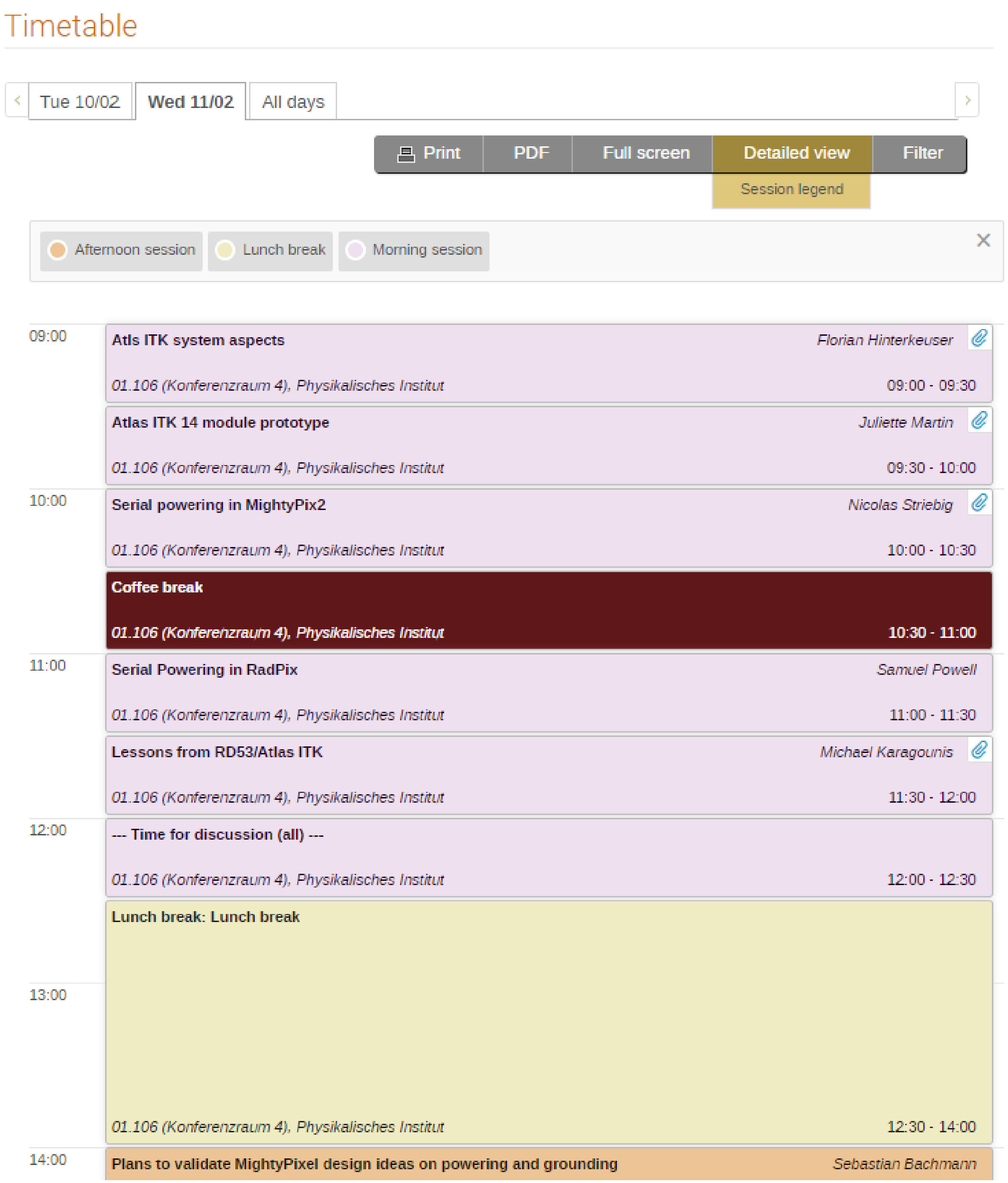


- VDD trim saturation
  - VDDA and VDDD: voltage regulator trimmable via DAC
  - Measure the full range and determine the best trim for 1.2 V
  - Saturation often seen on modules, not observed during wafer probing, likely due to different powering conditions and power-sharing on module
  - Some chips on a module go into undershunt - less severe when given more power
  - ✓ Improved/solved by increasing the nominal current (6.06 A → 6.25 A for outer system quads)

Real World Operation

Preparation for LHCb

- Also a recent meeting on experience from CMS and ATLAS in preparation for LHCb
- Very useful resource. Broader than calibration, but that is a major topic
- https://indico.cern.ch/event/1636729/timetable/#20260211.detailed
- Most interesting points in the following slides



Time	Title	Speaker	Location	Slot
09:00	**Atls ITK system aspects**	*Florian Hinterkeuser*	*01.106 (Konferenzraum 4), Physikalisches Institut*	09:00 - 09:30
	Atlas ITK 14 module prototype	*Juliette Martin*	*01.106 (Konferenzraum 4), Physikalisches Institut*	09:30 - 10:00
10:00	**Serial powering in MightyPix2**	*Nicolas Striebig*	*01.106 (Konferenzraum 4), Physikalisches Institut*	10:00 - 10:30
	Coffee break		*01.106 (Konferenzraum 4), Physikalisches Institut*	10:30 - 11:00
11:00	**Serial Powering in RadPix**	*Samuel Powell*	*01.106 (Konferenzraum 4), Physikalisches Institut*	11:00 - 11:30
	Lessons from RD53/Atlas ITK	*Michael Karagounis*	*01.106 (Konferenzraum 4), Physikalisches Institut*	11:30 - 12:00
12:00	**--- Time for discussion (all) ---**		*01.106 (Konferenzraum 4), Physikalisches Institut*	12:00 - 12:30
	Lunch break: Lunch break		*01.106 (Konferenzraum 4), Physikalisches Institut*	12:30 - 14:00
13:00				
14:00	**Plans to validate MightyPixel design ideas on powering and grounding**	*Sebastian Bachmann*		

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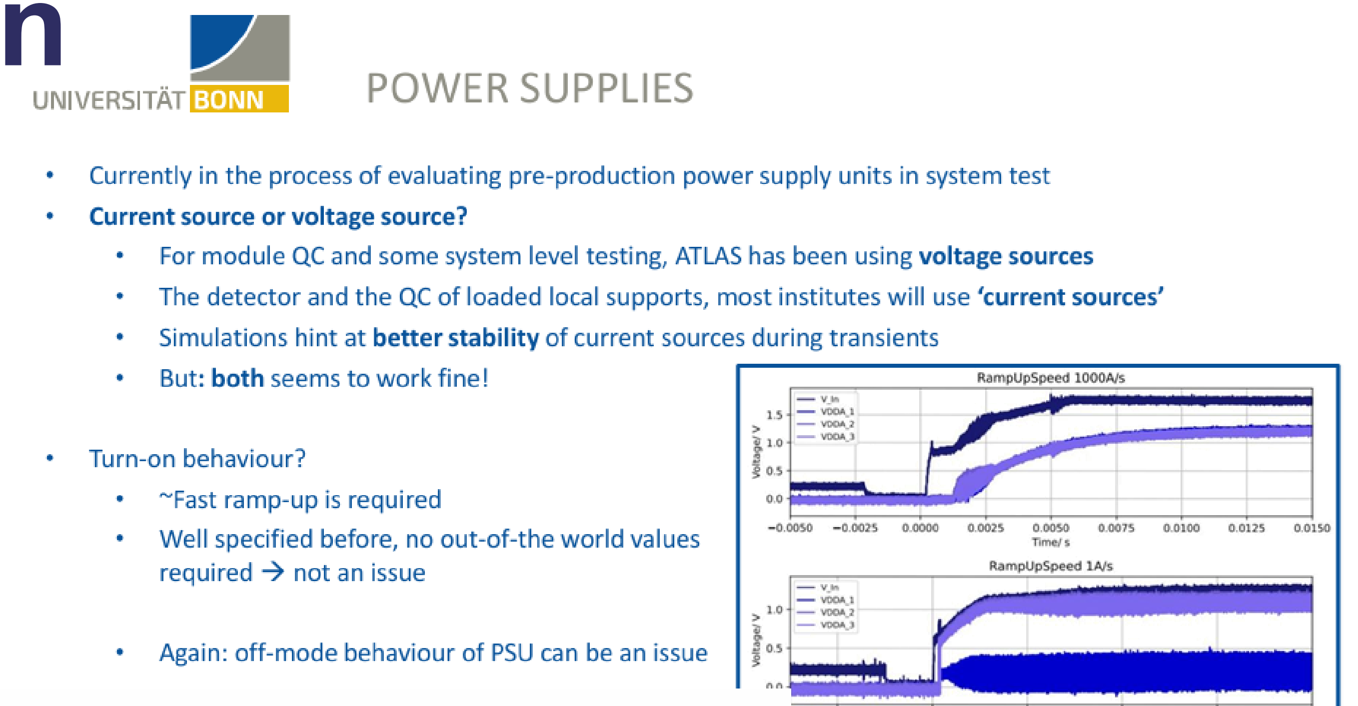
Real World Operation

Preparation for LHCb

- *ATLAS ITk System Aspects (Florian Hinterkeuser)*
- Current source or voltage source both seem to be acceptable.
- Which one for ePIC?
- Ramp speed is critical for start-up (simulations are currently 500A/s)



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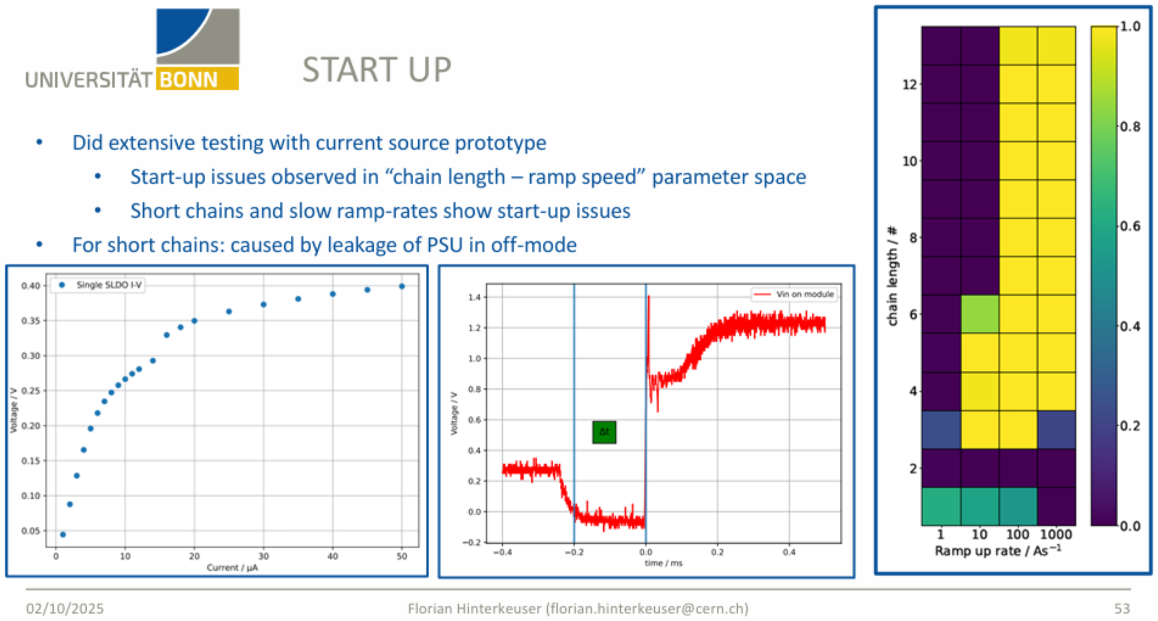
POWER SUPPLIES

- Currently in the process of evaluating pre-production power supply units in system test
- **Current source or voltage source?**
  - For module QC and some system level testing, ATLAS has been using **voltage sources**
  - The detector and the QC of loaded local supports, most institutes will use **'current sources'**
  - Simulations hint at **better stability** of current sources during transients
  - But: **both** seems to work fine!
- Turn-on behaviour?
  - ~Fast ramp-up is required
  - Well specified before, no out-of-the world values required → not an issue
  - Again: off-mode behaviour of PSU can be an issue



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START UP

- Did extensive testing with current source prototype
  - Start-up issues observed in "chain length – ramp speed" parameter space
  - Short chains and slow ramp-rates show start-up issues
- For short chains: caused by leakage of PSU in off-mode

02/10/2025 Florian Hinterkeuser (florian.hinterkeuser@cern.ch) 53

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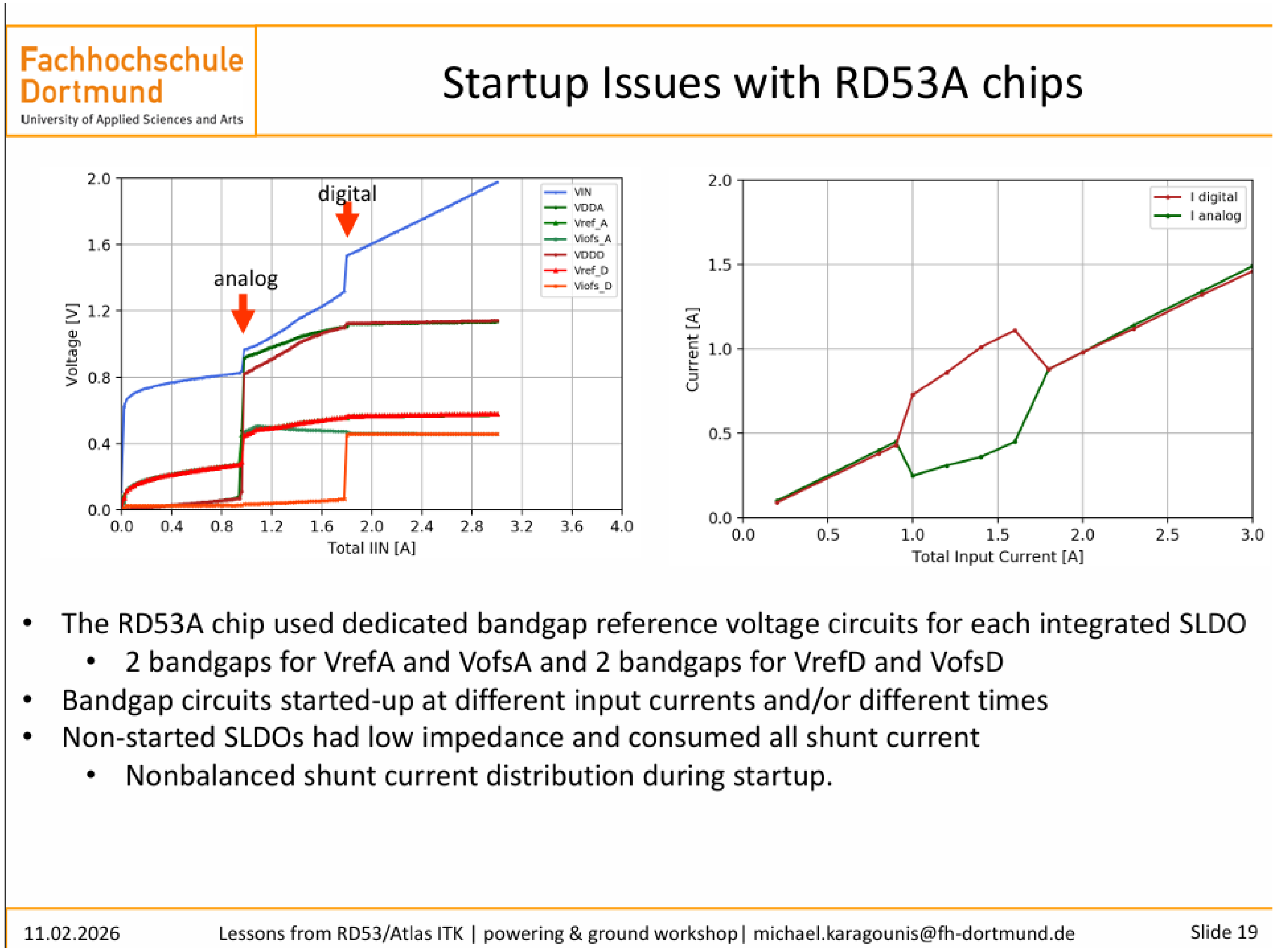
Real World Operation

Preparation for LHCb

- *Lessons from RD53/Atlas ITK (Michael Karagounis)*
- Mis-match in SLDOs leads to startup at different times
- Non-started SLDOs have low impedance, and consume all the shunt current – other SLDOs do not start
- This may not occur with us. Mode 1 has the SLDOs in high impedance. May occur in Mode 0, still to check.
- We also have fewer bandgaps than this



Startup Issues with RD53A chips

- The RD53A chip used dedicated bandgap reference voltage circuits for each integrated SLDO
  - 2 bandgaps for VrefA and VofsA and 2 bandgaps for VrefD and VofsD
- Bandgap circuits started-up at different input currents and/or different times
- Non-started SLDOs had low impedance and consumed all shunt current
  - Nonbalanced shunt current distribution during startup.

11.02.2026 Lessons from RD53/Atlas ITK | powering & ground workshop | michael.karagounis@fh-dortmund.de Slide 19

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Conclusion

Conclusion

Conclusion

- **Overview**
  - AncASIC (MPW3) progressing well, blocks ready, integration and software mockup underway.
  - Starting to build up a lot of really good test results from MPW1 and MPW2
  - Next submission opportunity in June
- **SLDO_5**
  - SLDO_5 design complete and ready for integration
  - Key point going forward is that we are now able to think about calibration of the SLDO_5 block and should probably start to do so

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Questions?

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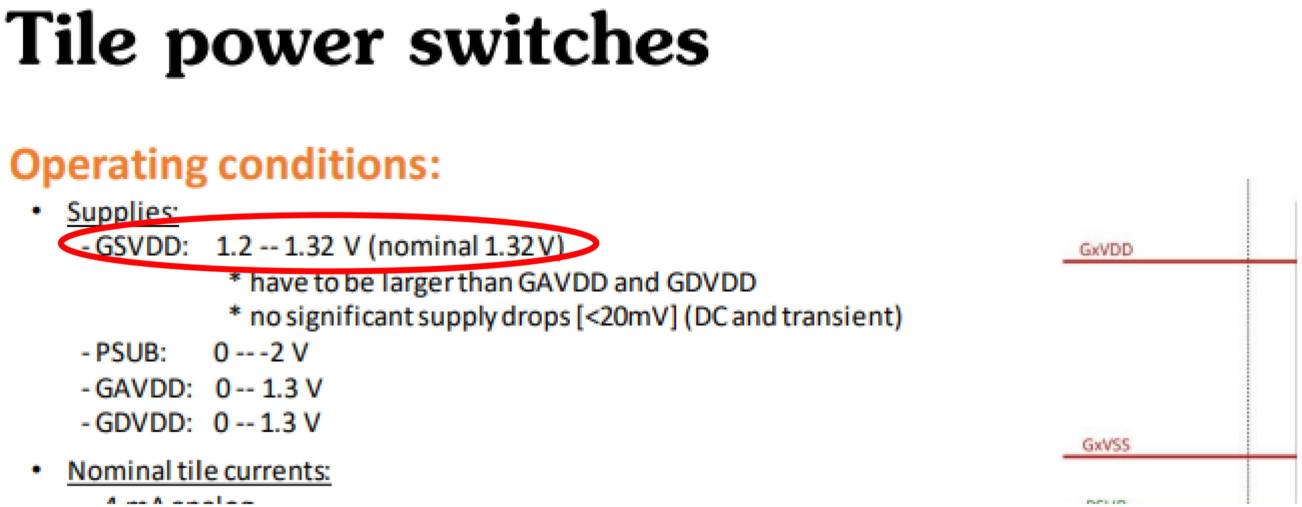
Backup

MOSAIX Supply Complexities

GA, GD and Services

- Remaining voltages are all driven at 1.32V
- It is necessary that services should always be above the other two, but this is handled internally by assuming that only GA and GD droop.
- Therefore we assume GA, GD and Services at 1.32V.



Tile power switches

Operating conditions:

- Supplies:
  - GSVDD: 1.2 -- 1.32 V (nominal 1.32 V)
    - * have to be larger than GAVDD and GDVDD
    - * no significant supply drops [<20mV] (DC and transient)
  - PSUB: 0 --- -2 V
  - GAVDD: 0 -- 1.3 V
  - GDVDD: 0 -- 1.3 V
- Nominal tile currents:

Testing MOSAIX with AncASIC

- James suggested it would be useful to be able to test the AncASIC powering MOSAIX when ER2 returns
- Ran some simulations to check if it is possible
- Seems that it is (for the Expected 25 case) because designing for Max45 EIC-LAS leaves a lot of headroom

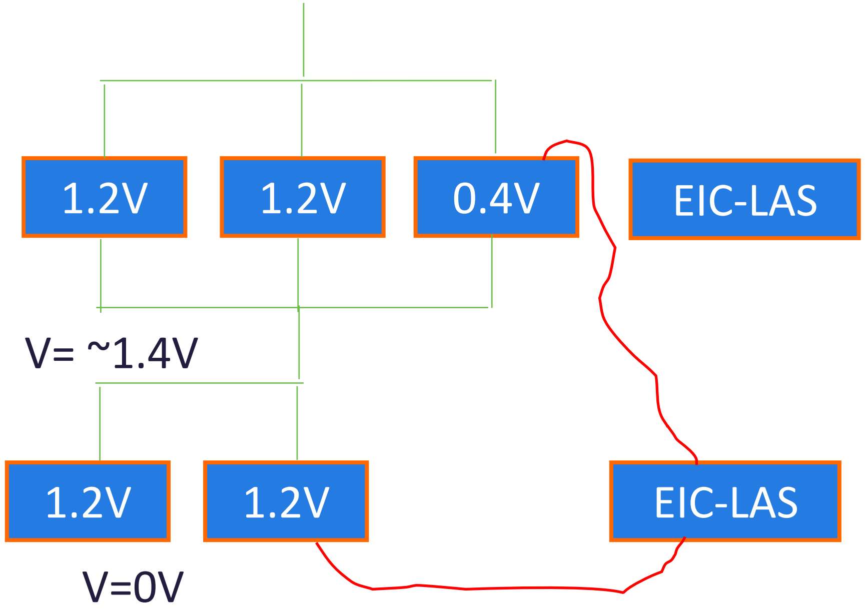
MOSAIX Supply Complexities…

The 1.8V Problem…

- MOSAIX requires not just a 1.2V supply, but also 1.8V to run the serialisers
- The AncASIC itself will need a 1.8V supply for logic and the NVG
- However, all SLDOs need to be in parallel, and if we run them at 1.8V, the 1.2V supplies will waste considerable power

What can we do?

- Run the SLDOs at 1.8V Considerable waste of power - ~1.1W
- Two serial powering chains Impossible – shared ground at various points
- Use the NVG? Could it step 1.2V up to 1.8V? Noise issues?
- Tap power from the next stage? Routing complexity. Stability? Still a power waste - ~300mW. What about the last one?
- Remove serialiser LDO from 65nm IP (serialiser itself is 1.2V)
- Supply 1.8V externally to each LAS Would need 8 lines (supply and return for each of 4 LAS).



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MOSAIX Supply Complexities…

The 1.8V Solution?

- João’s idea to edit the 65nm database to skip the LDO seems like a good one.
- We do not yet have a solution to powering the AncASIC circuits that run at 1.8V.
- It does seem that the serialiser could be separated from it’s LDO

https://indico.cern.ch/event/1376523/contributions/5785064/attachments/2789901/4865135/ALPIDE_65_30_01_2024.pdf

- So for the rest of this presentation, I will assume that the serialiser can be powered at 1.2V in order to get an overall power number.
- We should perhaps suggest to the higher SVT that they think about point-to-point powering of the 1.8V system just in case (would mean 8 extra wires)

Summary of Previous Data

EIC-LAS Power Consumption

- Since the MOSAIX design is evolving, power estimates are regularly updated. Key points at which we have updated our data in the past are:
    - ITS3 TDR (Feb 2024)
    - MOSAIX Engineering Specification Review (May 2024)
    - MOSAIX Sign-off Review (Nov 2024)
    - ITS3 Chamonix Meeting (May 2025) – provided detail on effect of number of links

- These have been refined into estimates for the LAS and combined with AncASIC simulations to produce estimates for the SVT
- Most recent is here, where Joao also updated the estimates based on EIC hit rates
- Will need to be refined further following test results

Update for Chamonix

- Have updated power estimates used in SLDO for the Chamonix numbers
- Assumes 1 Link, but not any power benefit of slower clock

	Voltage(V)	**Typ Power (mW)**			**Max Power (mW)**		
		ESR	Cham	Cham-SC	ESR	Cham	Cham-SC
GAVDD	1.32	222	222	222	356	356	356
GDVDD	1.32	908	1052	349	1148	1280	560
GSVDD	1.32	52	38	38	78	55	55
TXVDD	1.2	240	71	66	360	100	91
Total (LAS)		1422	1382	675	1942	1791	1062

Notes:
ESR: Based on Engineering Specification Review
Cham: Based on updated numbers from Chamonix
Cham-SC: Based on updated numbers from Chamonix and assuming the tile clock speed can be reduced

Numbers are for the LAS. AncASIC overhead adds 35-45%
Simulations also include AncBrain at 100mA and 200mA

Power Caveats…

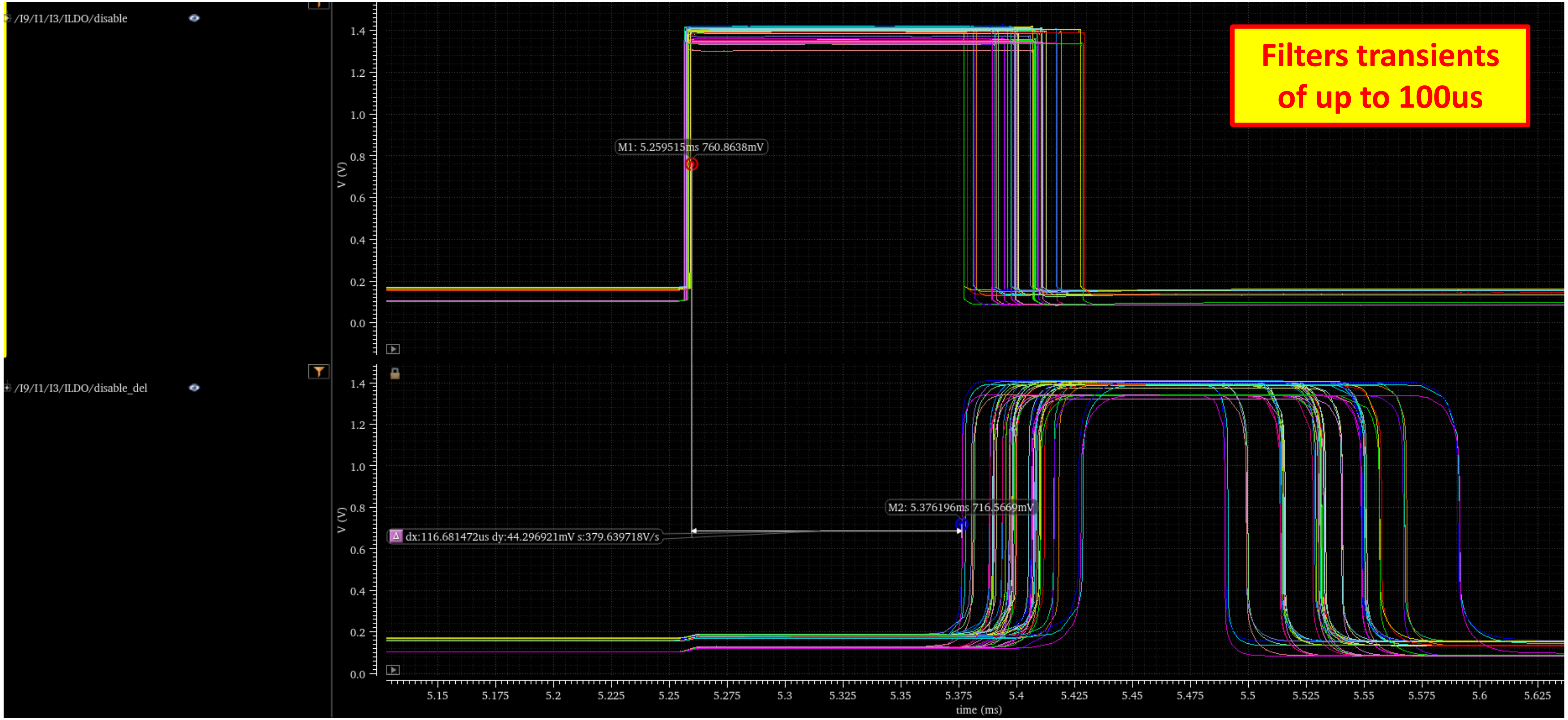
Caveats to the numbers

- Best estimate from MOSAIX. Not a warranty.
- Possibility that LEC value will rise (additional functions)
- For GAVDD, it is likely that EIC-LAS will be in the Max case, since we want the fastest frontend speed
- We may be able to reduce TXVDD consumption if we don't need all the transmitters (or can run slower). See Joao's presentation referenced in Slide 4.
- Need to add consumption of non-SLDO AncASIC
- Mis-match in GAVDD, GDVDD consumption may require different input voltages (waste of power in serial powering chain)
- Irradiation

Future Updates

- ~~May be future releases from MOSAIX~~
- ~~AncASIC will need to be updated once porting to XT011 is completed~~
- Test results from ER2

Overcurrent Protection



Filters transients of up to 100us

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SLDO_5

Voltage Stress

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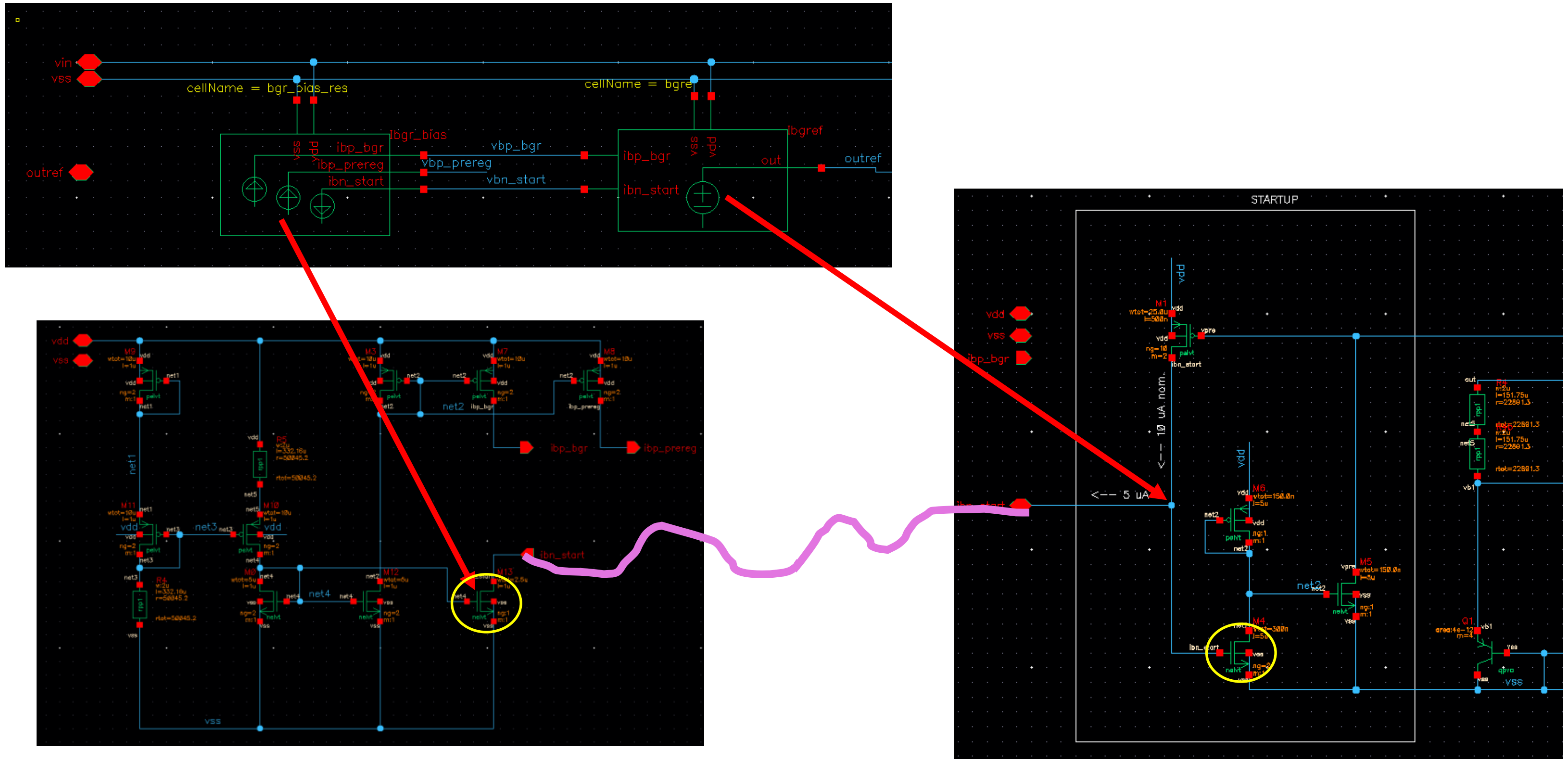
Voltage Stress in the Pre-Regulator

Device Check Violations

- Violations were continuing to be reported for the pre-regulator
- These are all tied to the transistors in the start-up circuit

2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I85/I62/Ibgr_bias/M13/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I85/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I85/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I85/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I2/I62/Ibgr_bias/M13/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I2/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I2/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I2/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I3/I62/Ibgr_bias/M13/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I3/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I3/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I3/I62/Ibgref/M4/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I1/I62/Ibgr_bias/M13/m1
2	Nominal	EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V6_POST_STARTUP	tran	/I9/I0/I0/I1/I62/Ibgref/M4/m1

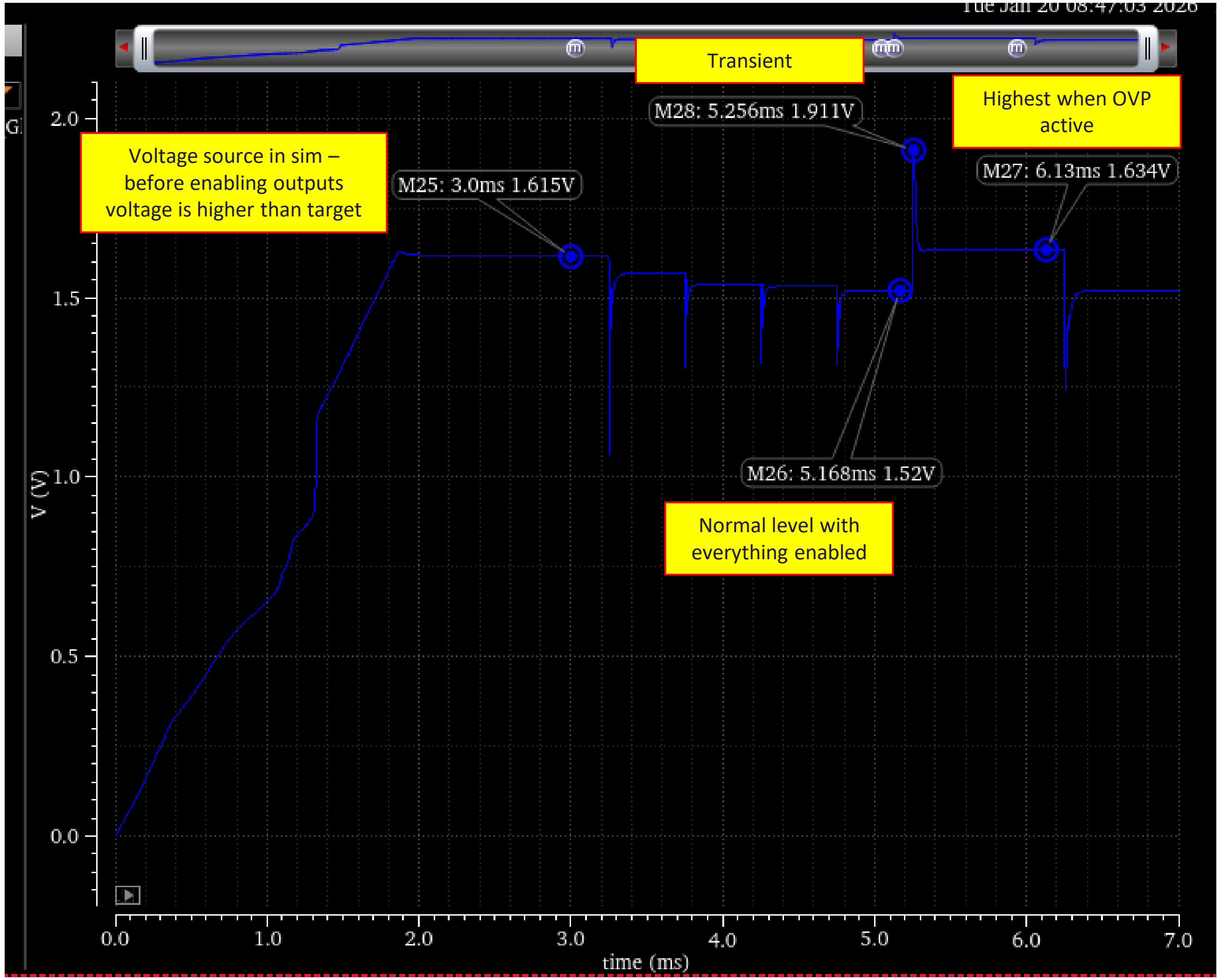


Voltage Stress in the Pre-Regulator

Vbn_start in detail

- Not a major issue, but is the biggest voltage weakness in the design
- Most of the violating levels are not extreme
- Still, this is the only place in the design where there is a single transistor between Vin and VSS
- Would be nice to fix it

vbn_start minus VSS

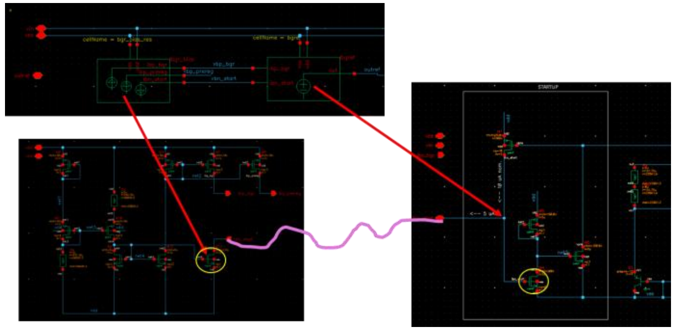


Transient

Highest when OVP active

Voltage source in sim – before enabling outputs voltage is higher than target

Normal level with everything enabled



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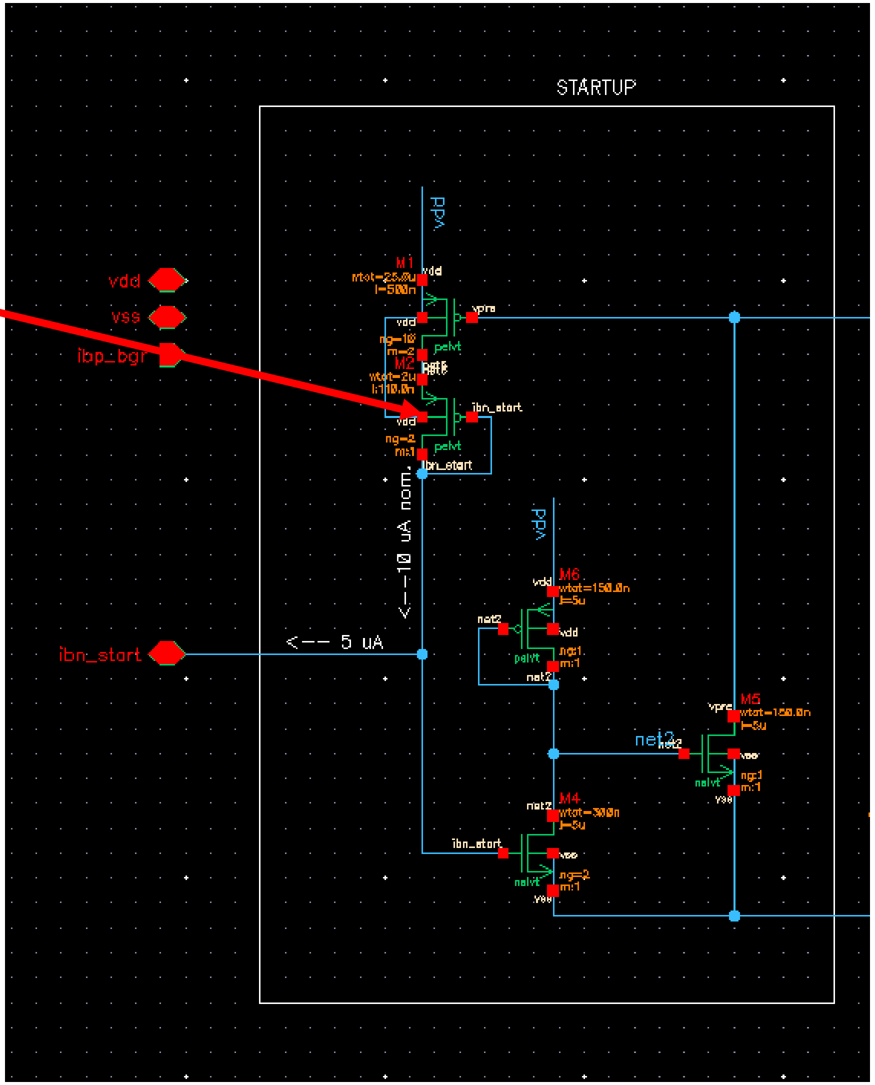
Voltage Stress in the Pre-Regulator

Correction

- This has been fixed by Amanda with the addition of an extra transistor



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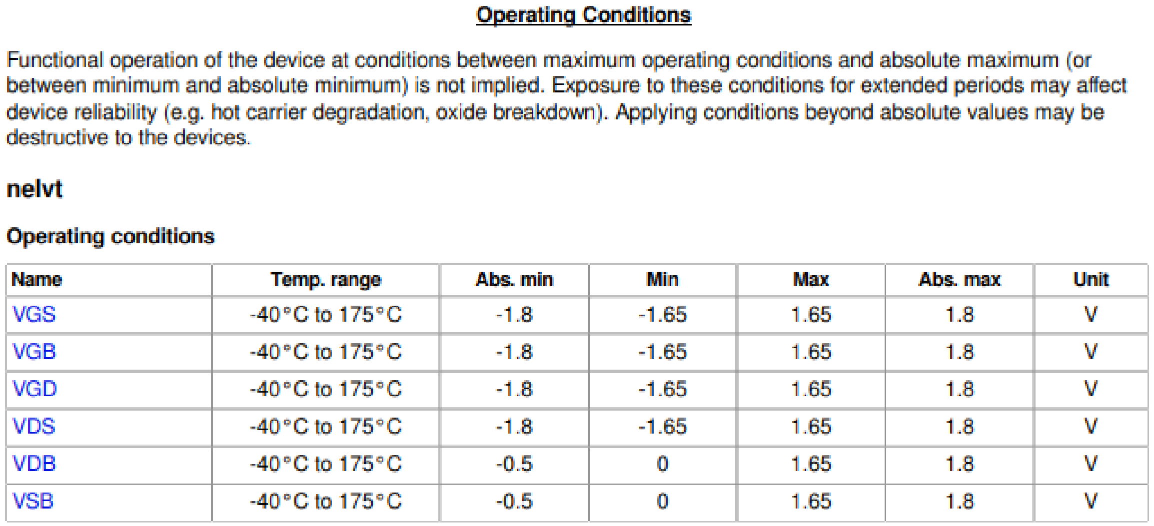
Voltage Stress in the OVP DAC

DAC Switches

- Remaining device check failures are all in the OVP DAC
- Basically because it is exposed to the full (clamped) Vin
- Should be OK, when clamped, will be within acceptable process range
- May fix as low priority (Roy is looking at it)



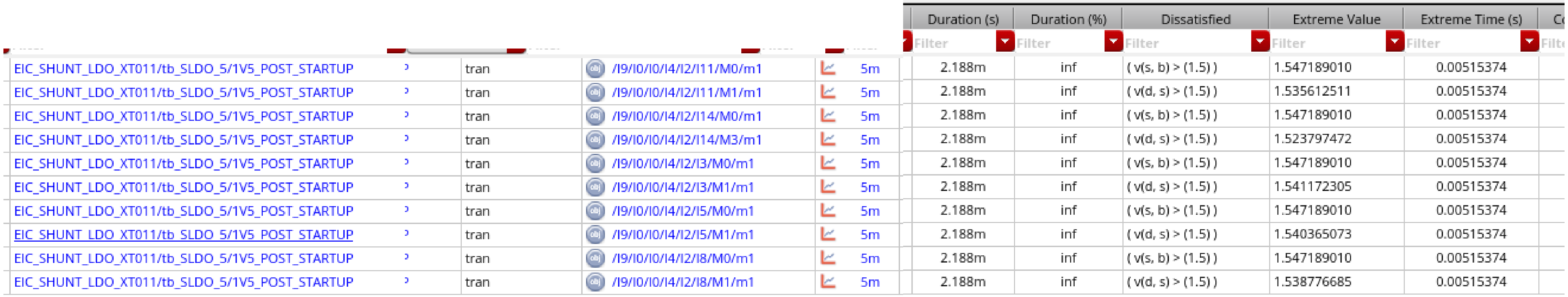
Operating Conditions

Functional operation of the device at conditions between maximum operating conditions and absolute maximum (or between minimum and absolute minimum) is not implied. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions beyond absolute values may be destructive to the devices.

nelvt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-1.8	-1.65	1.65	1.8	V
VGB	-40°C to 175°C	-1.8	-1.65	1.65	1.8	V
VGD	-40°C to 175°C	-1.8	-1.65	1.65	1.8	V
VDS	-40°C to 175°C	-1.8	-1.65	1.65	1.8	V
VDB	-40°C to 175°C	-0.5	0	1.65	1.8	V
VSB	-40°C to 175°C	-0.5	0	1.65	1.8	V

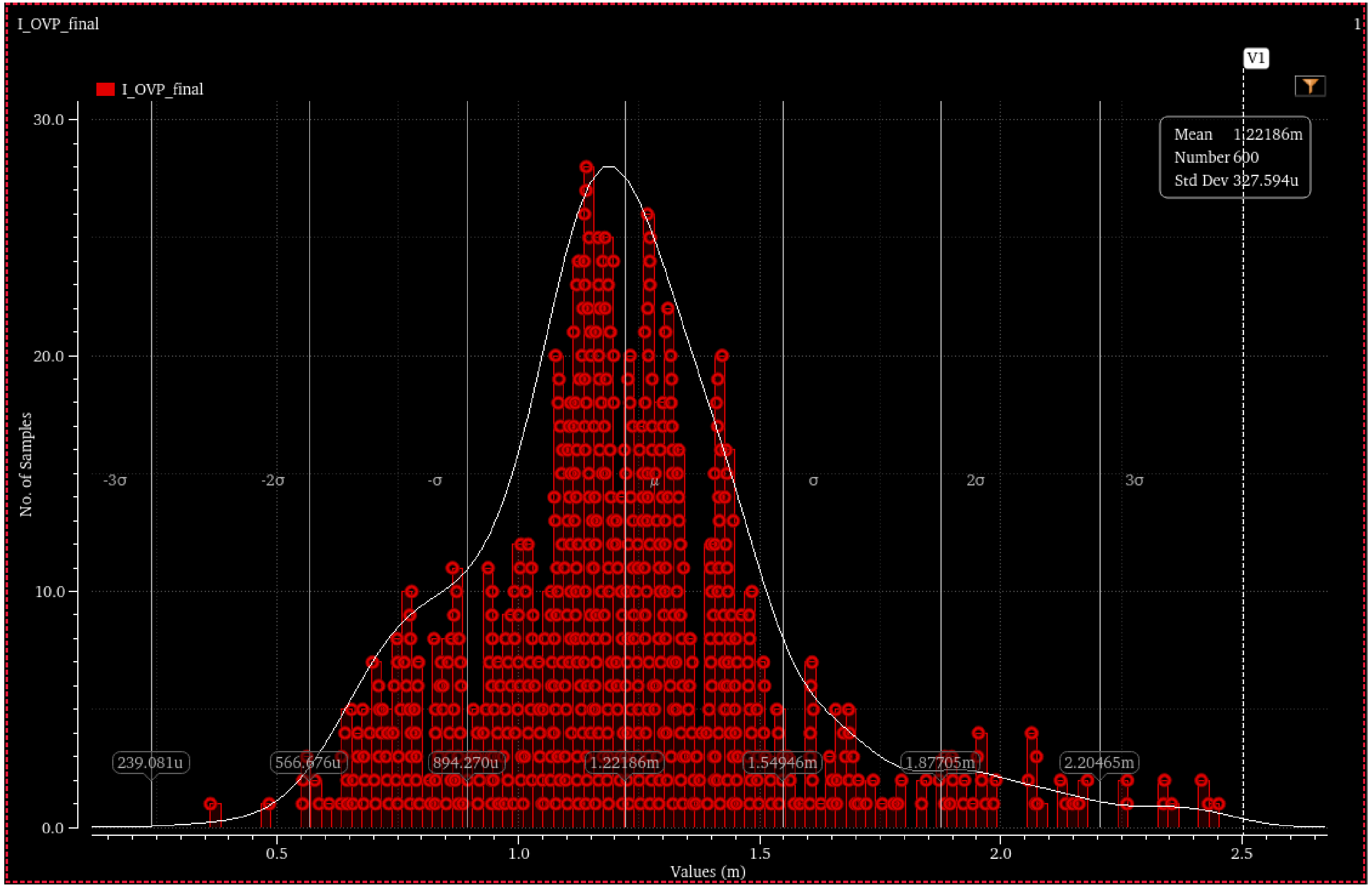


				Duration (s)	Duration (%)	Dissatisfied	Extreme Value	Extreme Time (s)
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I11/M0/m1	5m	2.188m	inf	(v(s, b) > (1.5))	1.547189010	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I11/M1/m1	5m	2.188m	inf	(v(d, s) > (1.5))	1.535612511	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I14/M0/m1	5m	2.188m	inf	(v(s, b) > (1.5))	1.547189010	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I14/M3/m1	5m	2.188m	inf	(v(d, s) > (1.5))	1.523797472	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I3/M0/m1	5m	2.188m	inf	(v(s, b) > (1.5))	1.547189010	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I3/M1/m1	5m	2.188m	inf	(v(d, s) > (1.5))	1.541172305	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I5/M0/m1	5m	2.188m	inf	(v(s, b) > (1.5))	1.547189010	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I5/M1/m1	5m	2.188m	inf	(v(d, s) > (1.5))	1.540365073	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I8/M0/m1	5m	2.188m	inf	(v(s, b) > (1.5))	1.547189010	0.00515374
EIC_SHUNT_LDO_XT011/tb_SLDO_5/1V5_POST_STARTUP	tran	/I9/I0/I0/I4/I2/I8/M1/m1	5m	2.188m	inf	(v(d, s) > (1.5))	1.538776685	0.00515374

Monte Carlo

OVP Calibration

- Need to calibrate the OVP code as well as the DAC code and chain current
- Done by increasing OVP limit until current falls below a given threshold
- Threshold also varies with Monte Carlo, so look at early simulations and set a limit suited to all – 2.5mA



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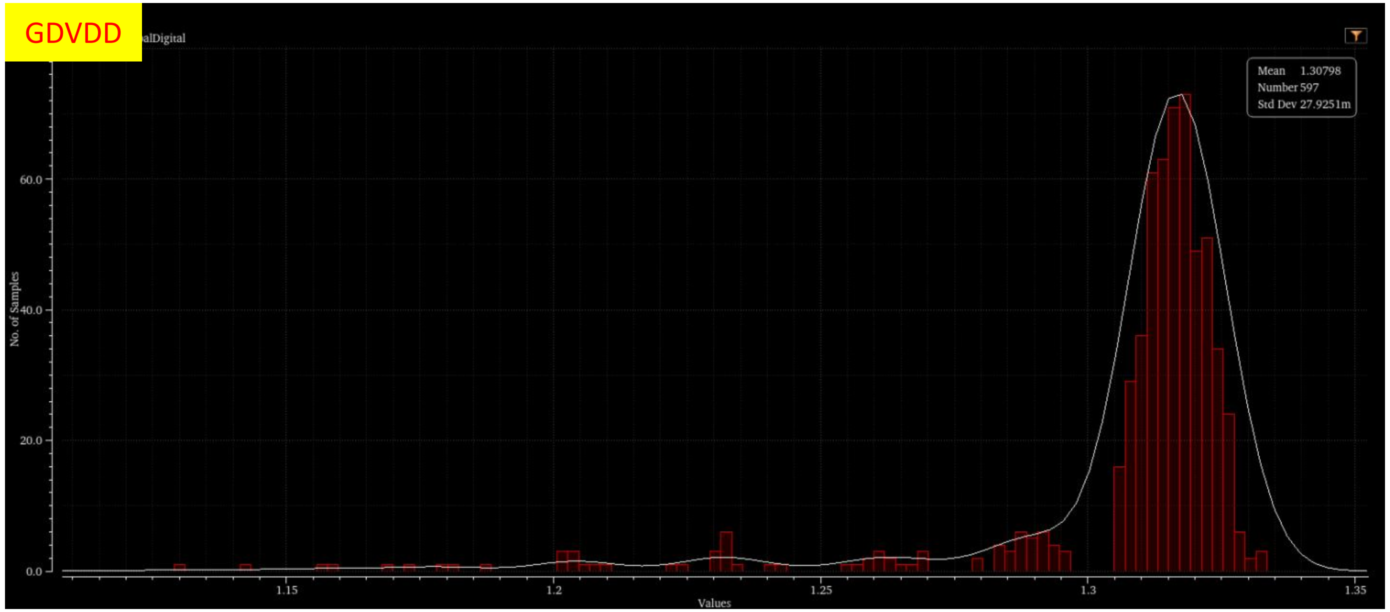
Monte Carlo

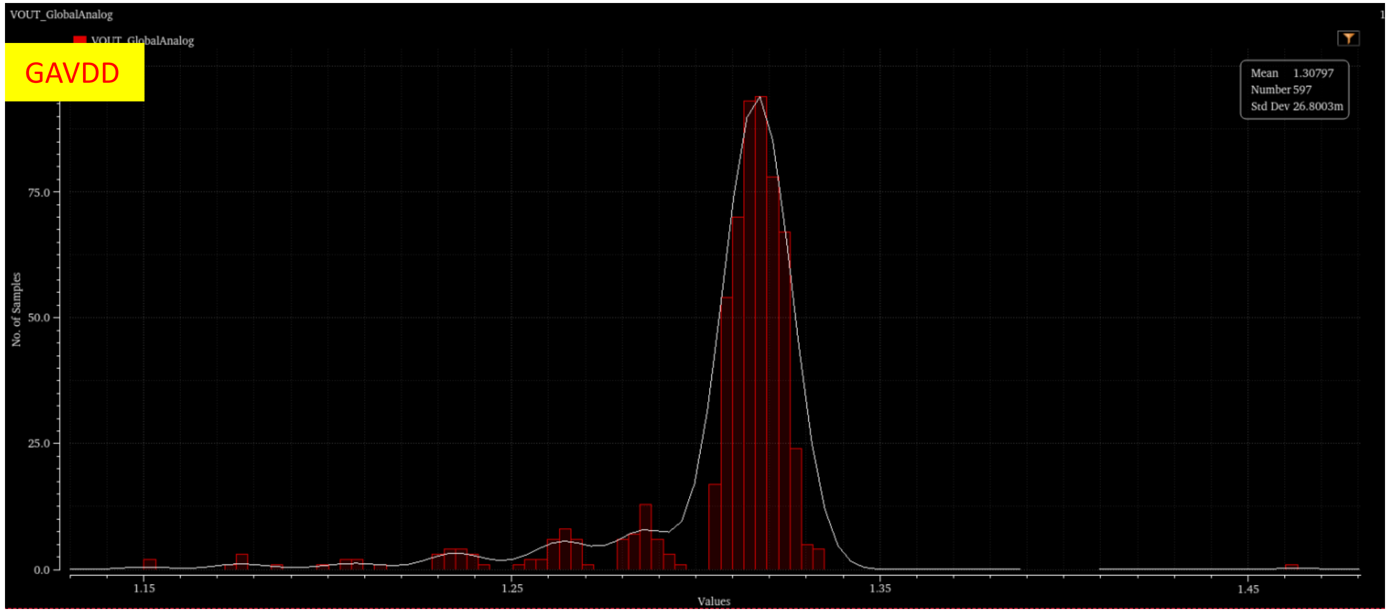
Output Voltage Spread

- 600 runs (300 in typ case, 300 in max)

- Most of the values at the wrong code probably due to improper calibration (could spend time on this…but doesn't seem worth it)

- Note that the supply for the AncBrain is uncalibrated because the AncBrain does not drive it to avoid the risk of the AncBrain taking down its own supply.





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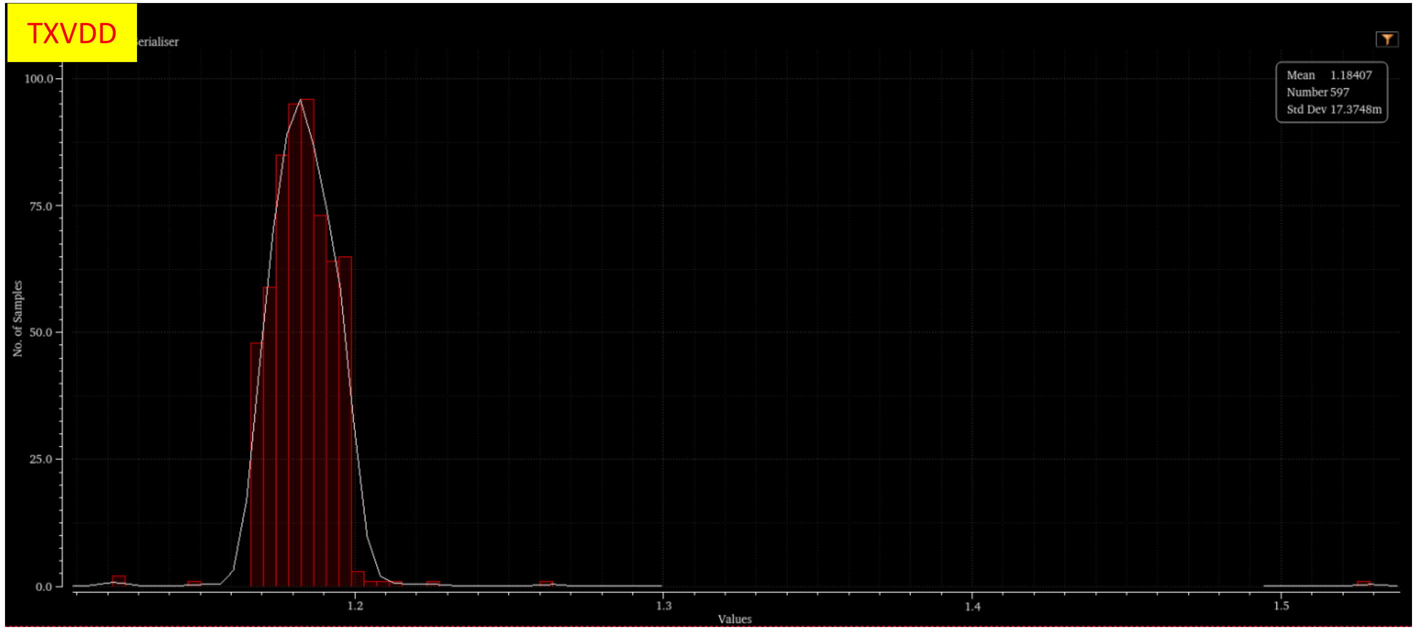
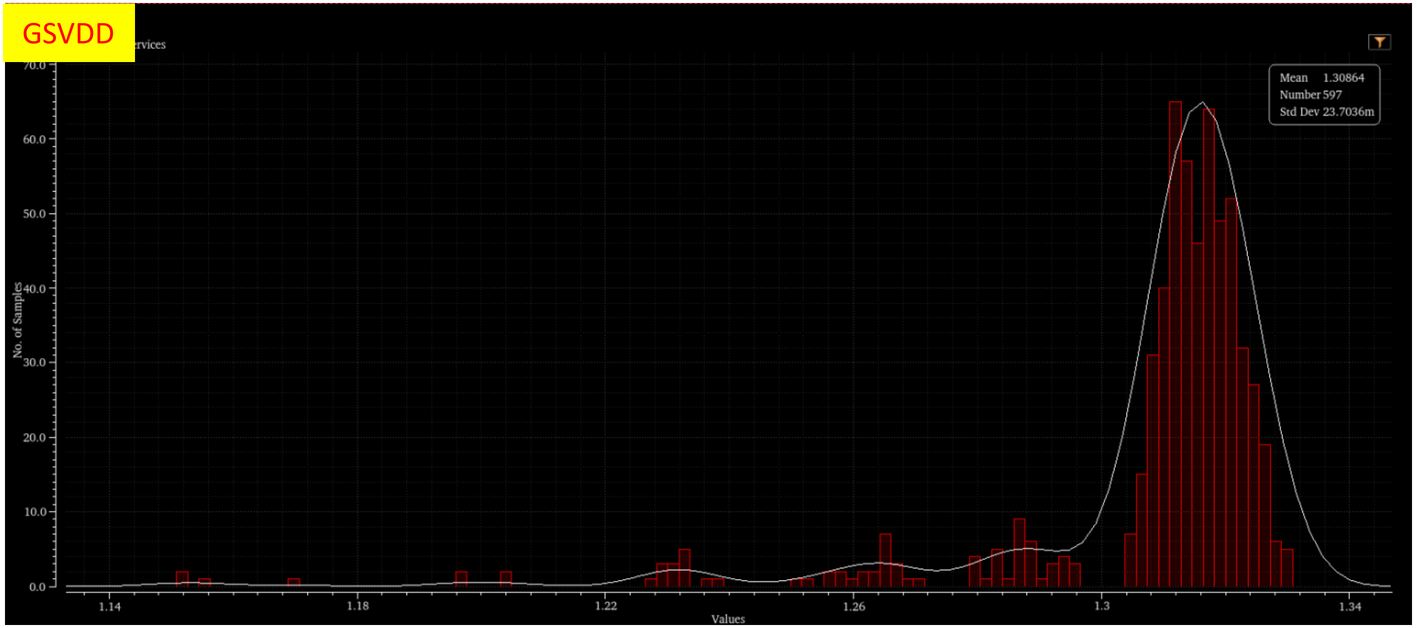
Monte Carlo

Output Voltage Spread

- 600 runs (300 in typ case, 300 in max)
- Most of the values at the wrong code probably due to improper calibration (could spend time on this…but doesn't seem worth it)
- Note that the supply for the AncBrain is uncalibrated because the AncBrain does not drive it to avoid the risk of the AncBrain taking down its own supply.





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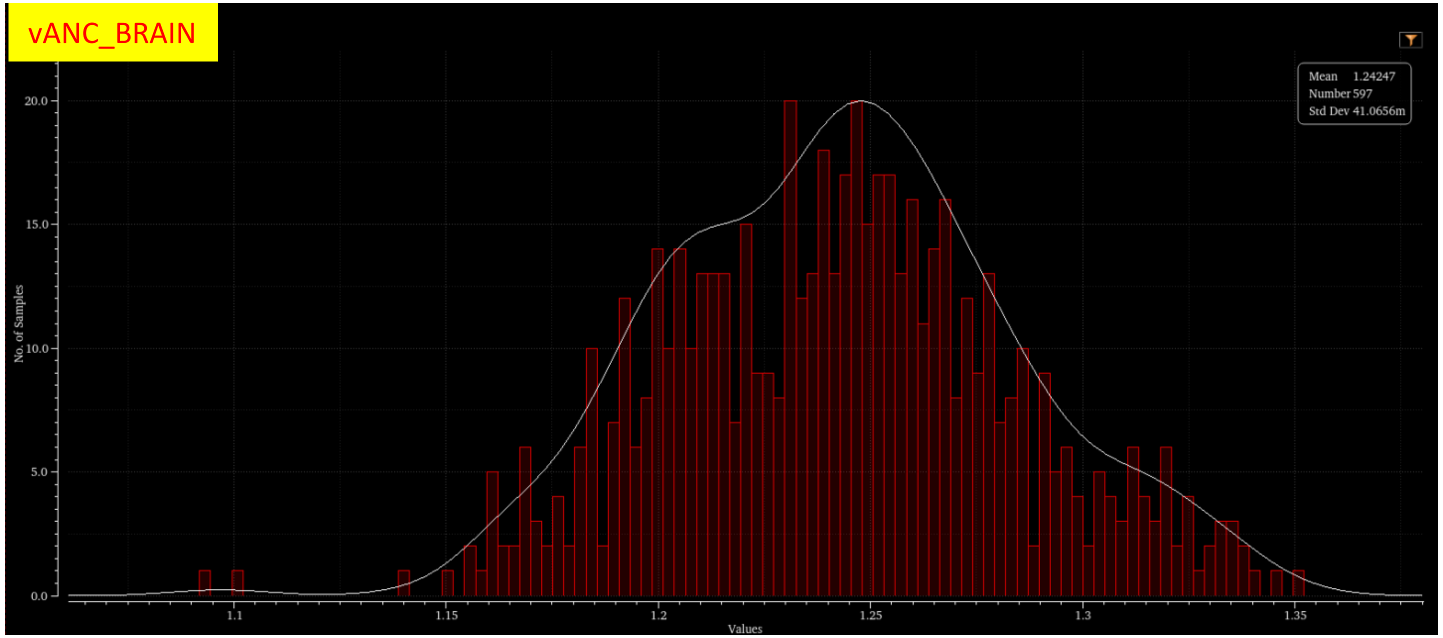
Monte Carlo

Output Voltage Spread

- Note that the supply for the AncBrain is uncalibrated because the AncBrain does not drive it to avoid the risk of the AncBrain taking down its own supply.
- Of course, this introduces the alternative risk that the AncBrain supply does not come up correctly.
- Higher than target probably not an issue. Lower could be.
- We could alter the default slightly to make lower voltages even less likely



μ: 1.247V
σ: 41.2mV
Max: 1.36
Min: 1.1
Target: 1.2V

This could be shifted to the right if we are worried about AncBrain speed. For now, we leave it as is, since we think this matches well with the PVT corner Arif is simulating.

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Monte Carlo

Voltage Stress

- Previously used device checks to monitor individual device stresses
- Not possible in Monte Carlo (device checks not permitted)
- Just check the stress across the individual shunts – local voltages vary due to the internal supply resistances
- A good analog, since a few devices do see this voltage
- “Absolute Max” never exceeded. “Max” breached very rarely. However, this is not applied to most transistors. Only OVP DAC gates remain a possible issue.

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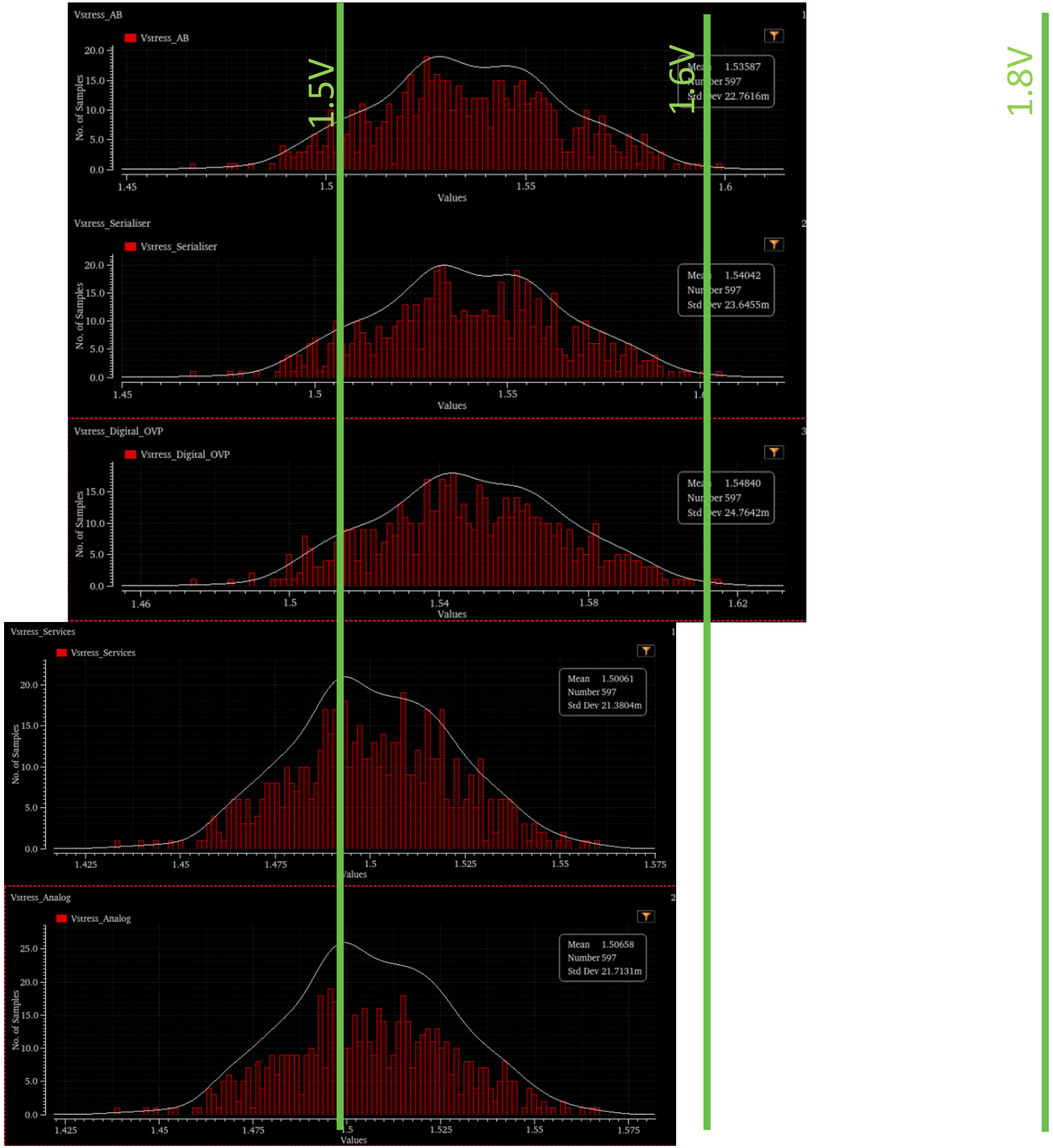
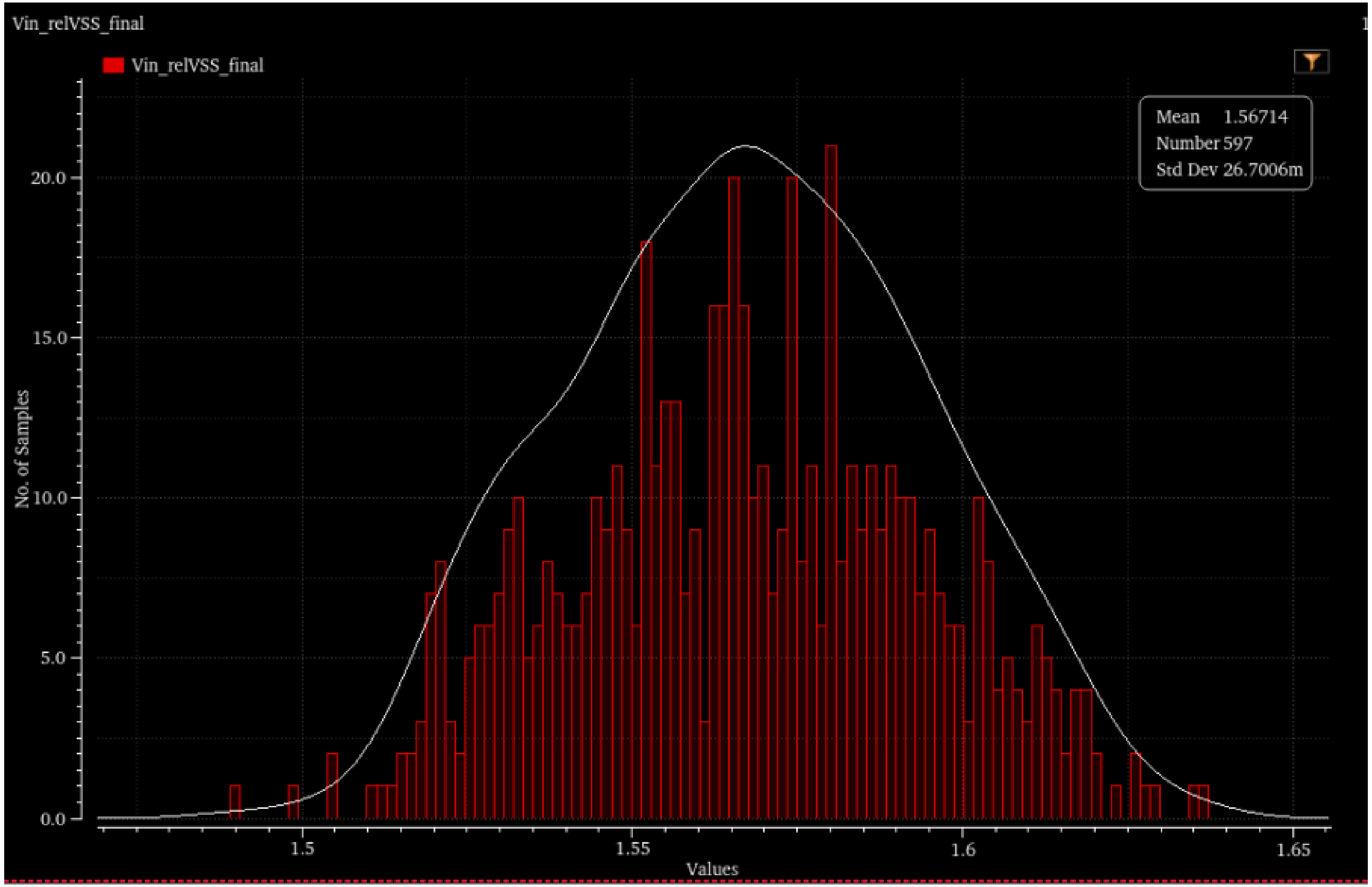


Monte Carlo

Full chip stress

- Covers SLDO, power bus resistances, bond wires resistances, pads
- Within the 1.65V max value
- Targeting a dropout of 250mV over the 1.32V supply



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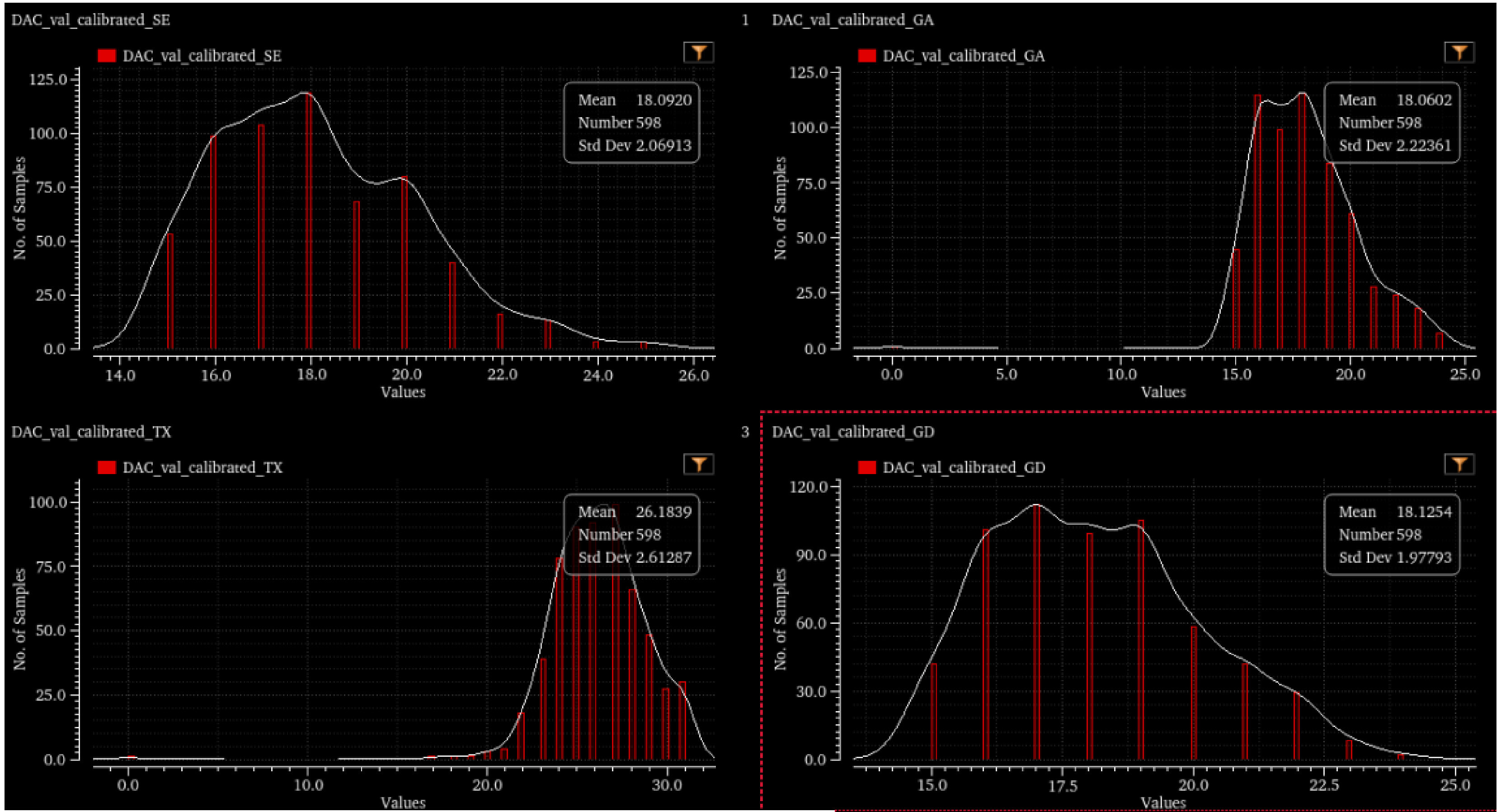
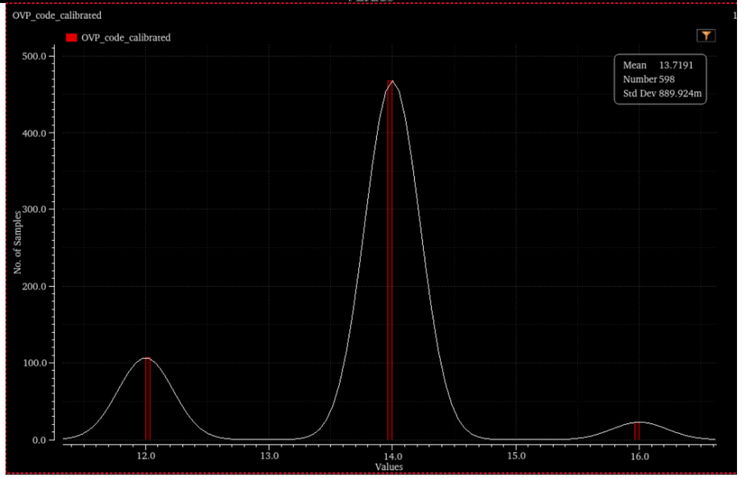
Monte Carlo

Calibration Codes

- To check what range of calibration codes we are using
- Mostly within the range. TX is against the limit because it is the lowest voltage.
- OVP codes are well within range and vary little





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SLDO_5

Corners

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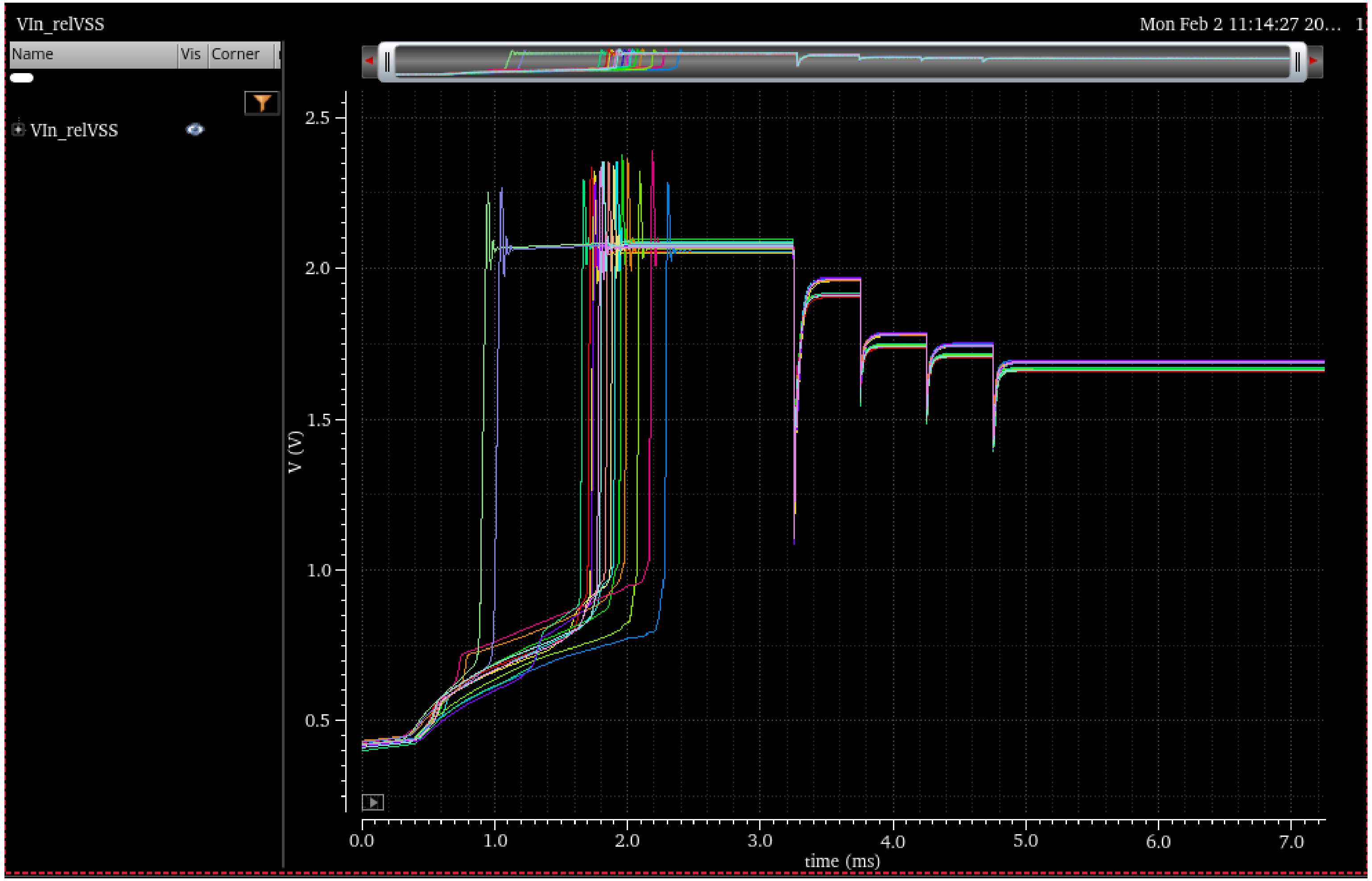
Corners

OVP Triggering

- Check in the corners that the OVP does not unexpectedly trigger.
- Ran the MOS and RES corners
- Operation is fine, no unexpected triggering
- Need to increase current to 1.5A (typ) and 1.95A (max) as with single SLDO corners
- Leads to loss of efficiency



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Corners

Constant Voltage vs. Constant Current

- Much as with the Monte Carlo simulations running with a constant current source has startup implications
- An increased current beyond the nominal current is needed for startup (at least in Mode 1)
- This is higher than the level needed for the Monte Carlo simulations (was set at 300mA) but the same principle applies
- Does not imply higher voltage
- Some corners need iChain_start as high as 800mA

This simulation is an example with a constant voltage source to allow the required current to be measured. It can be seen that in "nominal", the steady state, 1.3A current is sufficient, but an additional 600mA is needed to start in one extreme corner. This should be applied only for startup, otherwise the efficiency will be poor.

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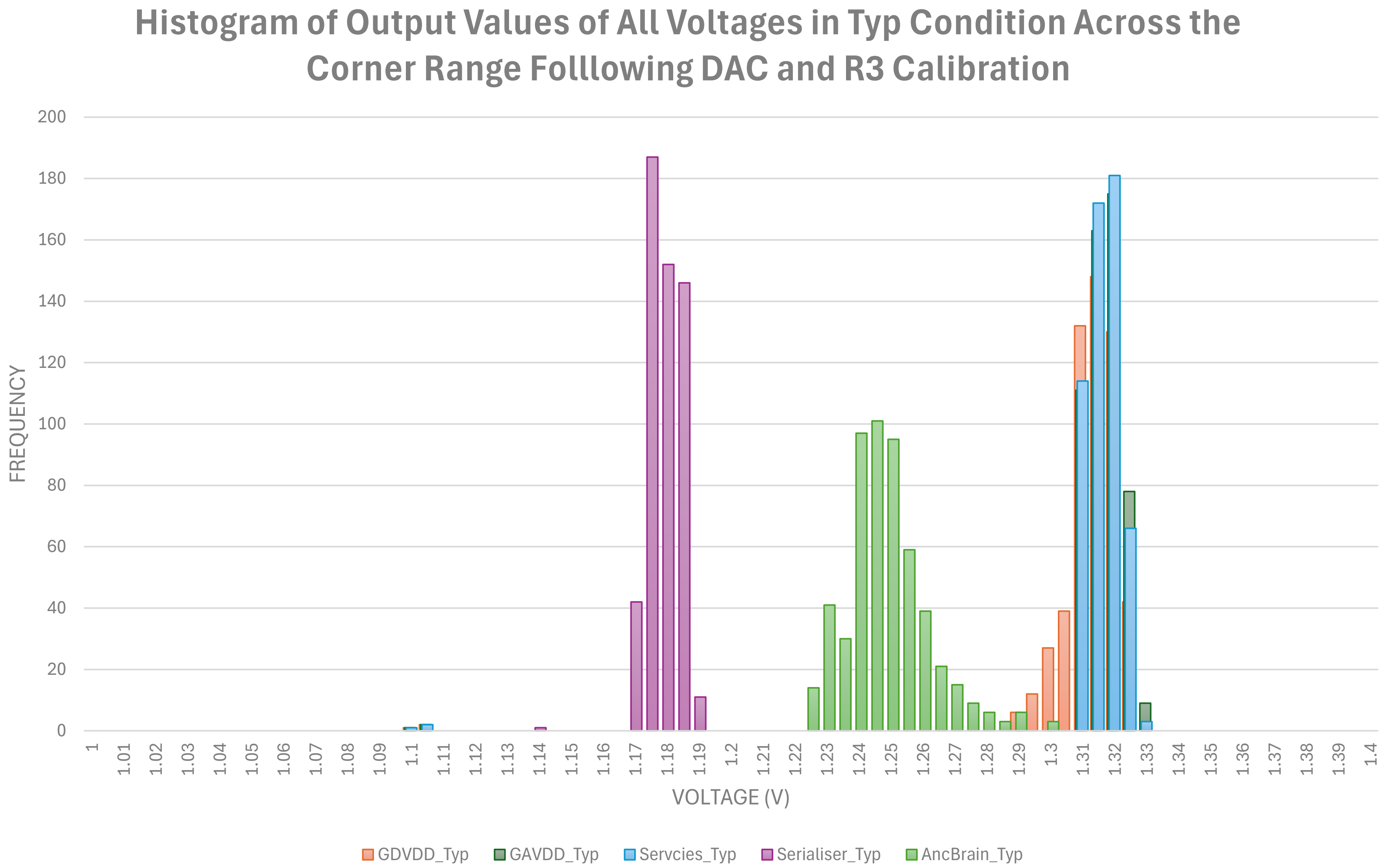
Corners

Typ Condition

- Typical EIC-LAS Current Values
- DAC Calibration Applied
- R3 Calibration Applied



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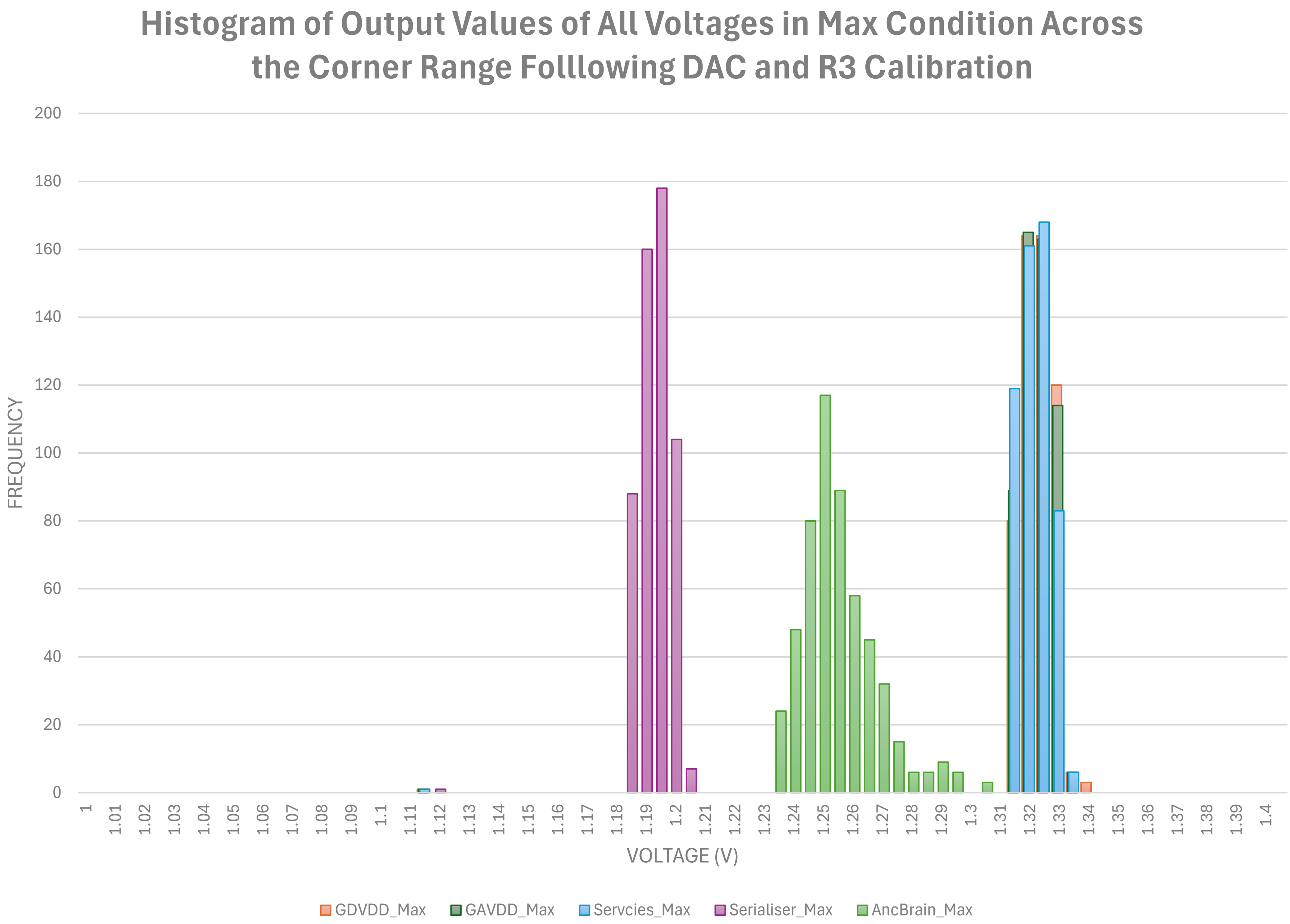
Corners

Max Condition

- Max EIC-LAS Current Values
- DAC Calibration Applied
- R3 Calibration Applied



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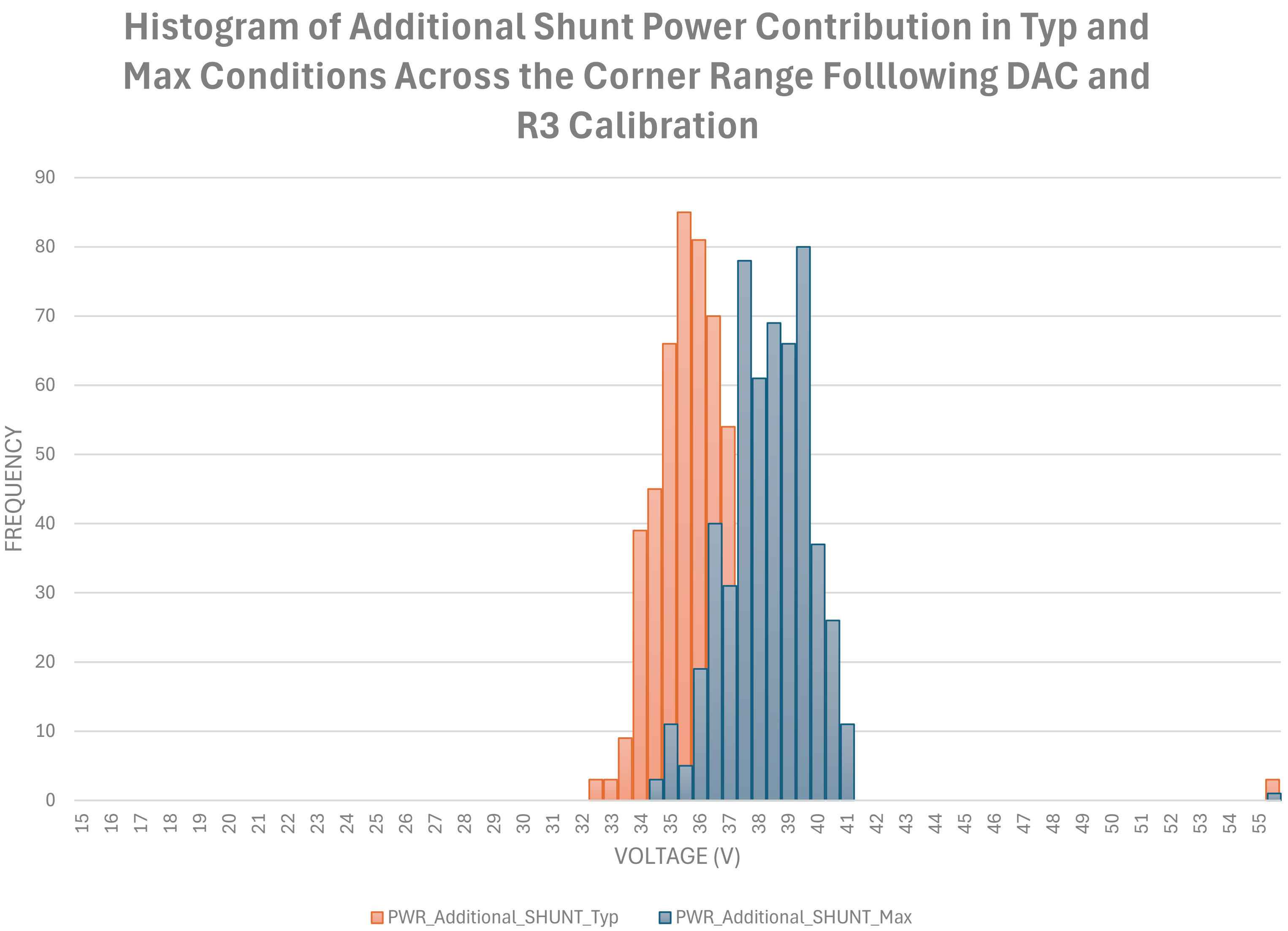
Corners

Additional Shunt Power

- Additional power added by SLDO_5 as a fraction of the load power
- 32-41%
- Consistent with previous SLDO corner values, and SLDO_5 Monte Carlo simulations
- Greate Typ-Max variation that in single SLDO, because some SLDO_5 power bus routing included, so losses there
- **Just the SLDOs. Does not include FPC losses.**



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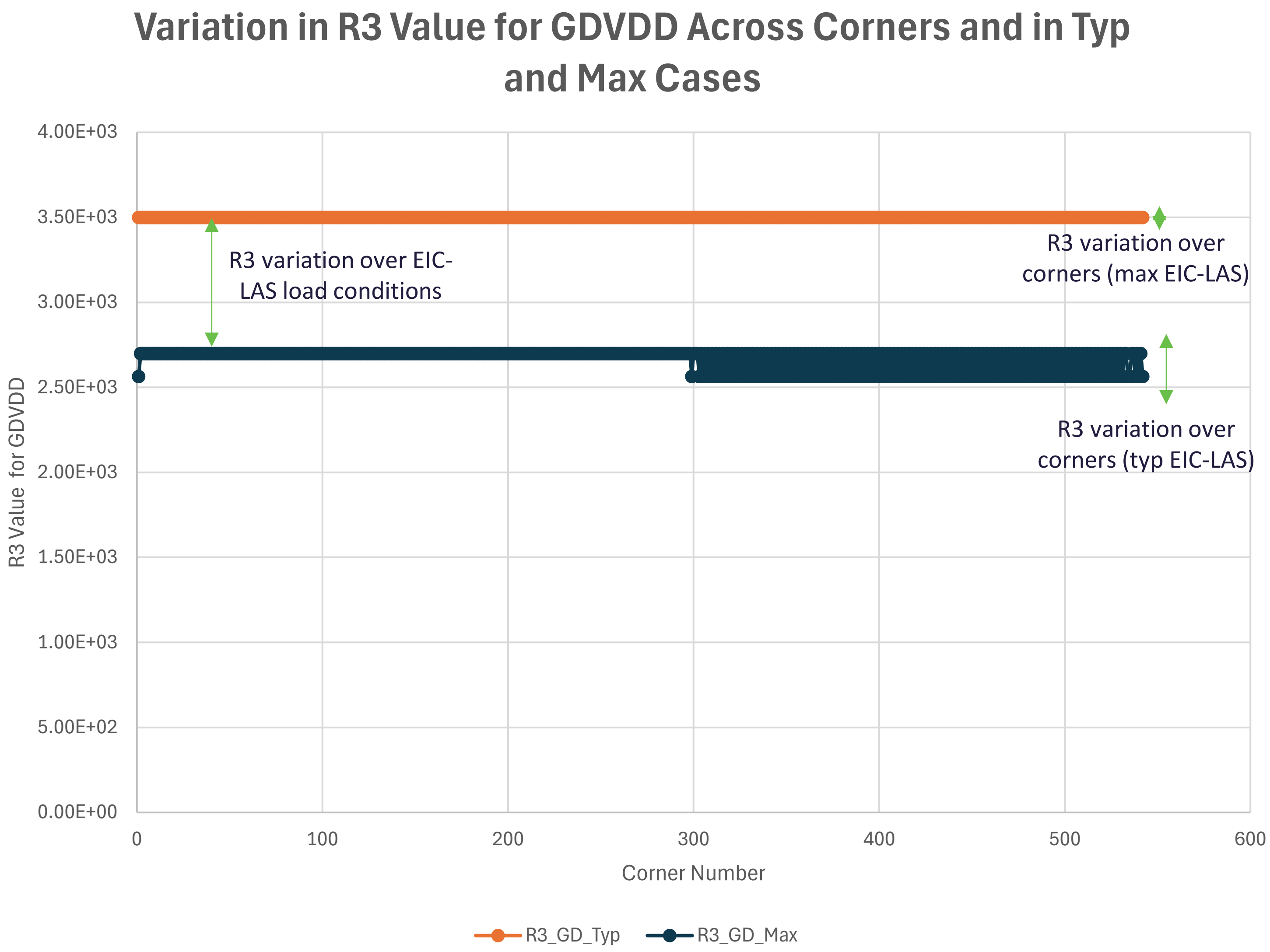
Corners

R3 Variation

- As for Monte Carlo, variation in R3 Value required for highest efficiency is grate between load conditions than for SLDO variation
- Actually, there is almost no variation for the corners themselves, showing mis-match is more important
- Showing GDVDD as an example, but applies to all



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SLDO_5

Extracted and EMIR

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Extracted

Conditions

- Ran the extraction on SLDO_5, but with the SLDO and OVP “black boxed” i.e. excluded from the extraction
- Therefore effectively just extracting the power buses (since SLDO already tested and OVP extraction simulated separately)
- Extraction is R only
- Need to merge and filter resistances to get to a reasonably size extracted view

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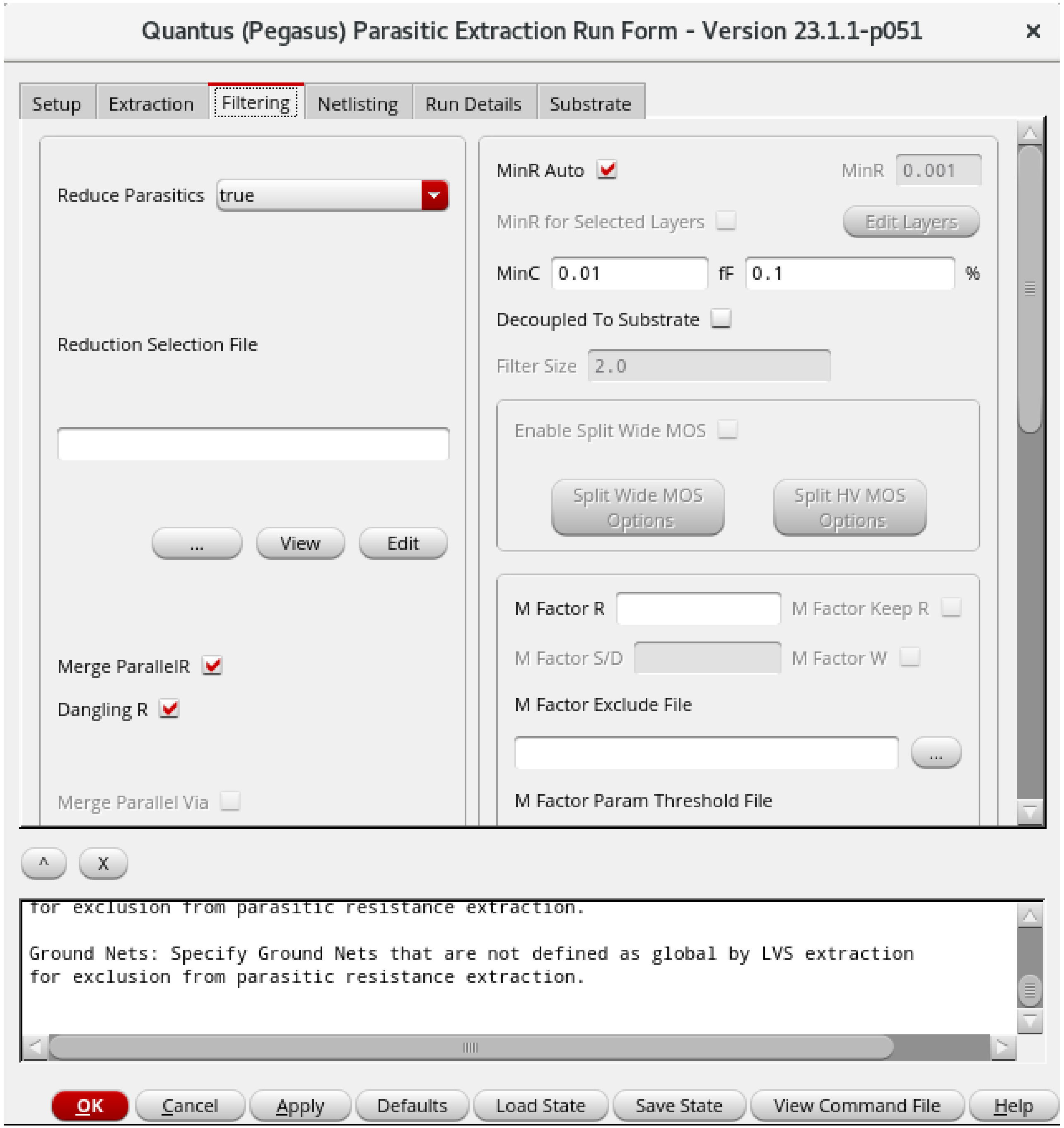


Quantus (Pegasus) Parasitic Extraction Run Form - Version 23.1.1-p051

Reduce Parasitics: true

Reduction Selection File

Merge ParallelR ☑

Dangling R ☑

Merge Parallel Via ☐

MinR Auto ☑ MinR 0.001

MinR for Selected Layers ☐

MinC 0.01 fF 0.1 %

Decoupled To Substrate ☐

Filter Size 2.0

Enable Split Wide MOS ☐

M Factor R M Factor Keep R ☐

M Factor S/D M Factor W ☐

M Factor Exclude File

M Factor Param Threshold File

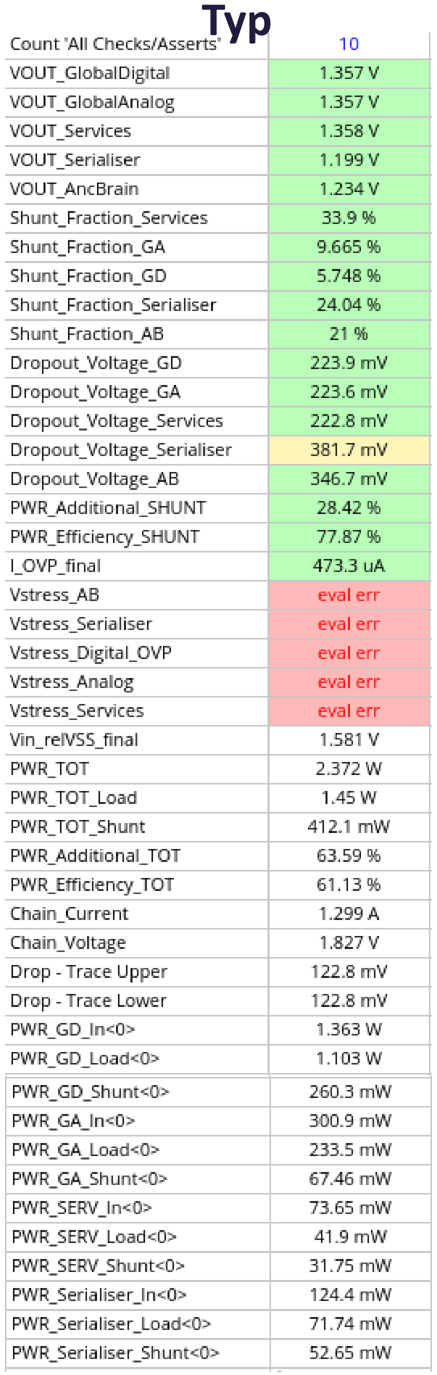
```
for exclusion from parasitic resistance extraction.

Ground Nets: Specify Ground Nets that are not defined as global by LVS extraction
for exclusion from parasitic resistance extraction.
```

Extracted

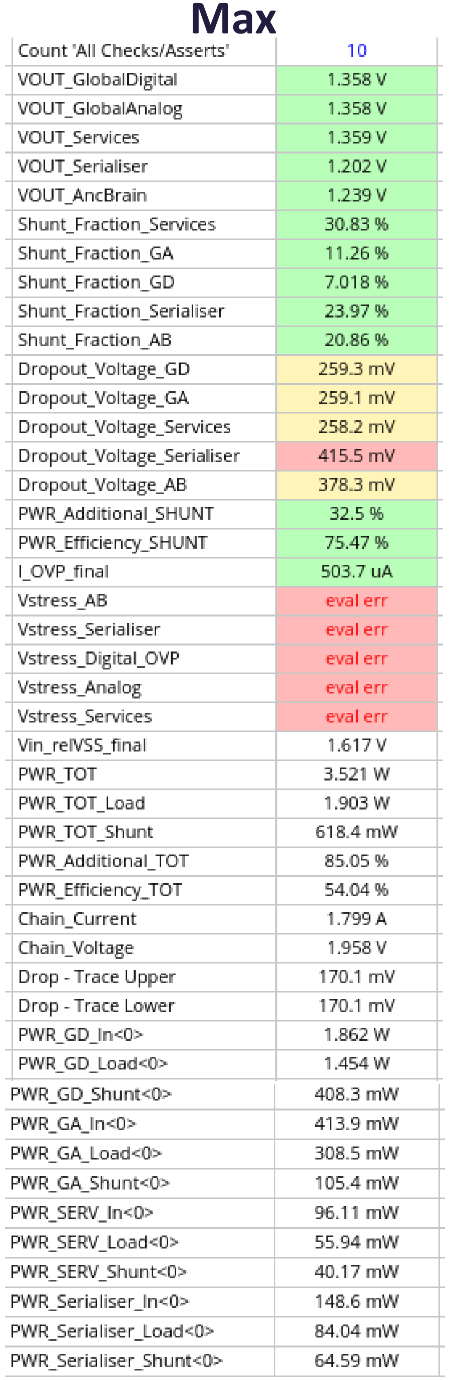
Simulation

- Typ and Max cases re-run with extracted view



Typ

Count 'All Checks/Asserts'	10
VOUT_GlobalDigital	1.357 V
VOUT_GlobalAnalog	1.357 V
VOUT_Services	1.358 V
VOUT_Serialiser	1.199 V
VOUT_AncBrain	1.234 V
Shunt_Fraction_Services	33.9 %
Shunt_Fraction_GA	9.665 %
Shunt_Fraction_GD	5.748 %
Shunt_Fraction_Serialiser	24.04 %
Shunt_Fraction_AB	21 %
Dropout_Voltage_GD	223.9 mV
Dropout_Voltage_GA	223.6 mV
Dropout_Voltage_Services	222.8 mV
Dropout_Voltage_Serialiser	381.7 mV
Dropout_Voltage_AB	346.7 mV
PWR_Additional_SHUNT	28.42 %
PWR_Efficiency_SHUNT	77.87 %
I_OVP_final	473.3 uA
Vstress_AB	eval err
Vstress_Serialiser	eval err
Vstress_Digital_OVP	eval err
Vstress_Analog	eval err
Vstress_Services	eval err
Vin_relVSS_final	1.581 V
PWR_TOT	2.372 W
PWR_TOT_Load	1.45 W
PWR_TOT_Shunt	412.1 mW
PWR_Additional_TOT	63.59 %
PWR_Efficiency_TOT	61.13 %
Chain_Current	1.299 A
Chain_Voltage	1.827 V
Drop - Trace Upper	122.8 mV
Drop - Trace Lower	122.8 mV
PWR_GD_In<0>	1.363 W
PWR_GD_Load<0>	1.103 W
PWR_GD_Shunt<0>	260.3 mW
PWR_GA_In<0>	300.9 mW
PWR_GA_Load<0>	233.5 mW
PWR_GA_Shunt<0>	67.46 mW
PWR_SERV_In<0>	73.65 mW
PWR_SERV_Load<0>	41.9 mW
PWR_SERV_Shunt<0>	31.75 mW
PWR_Serialiser_In<0>	124.4 mW
PWR_Serialiser_Load<0>	71.74 mW
PWR_Serialiser_Shunt<0>	52.65 mW



Max

Count 'All Checks/Asserts'	10
VOUT_GlobalDigital	1.358 V
VOUT_GlobalAnalog	1.358 V
VOUT_Services	1.359 V
VOUT_Serialiser	1.202 V
VOUT_AncBrain	1.239 V
Shunt_Fraction_Services	30.83 %
Shunt_Fraction_GA	11.26 %
Shunt_Fraction_GD	7.018 %
Shunt_Fraction_Serialiser	23.97 %
Shunt_Fraction_AB	20.86 %
Dropout_Voltage_GD	259.3 mV
Dropout_Voltage_GA	259.1 mV
Dropout_Voltage_Services	258.2 mV
Dropout_Voltage_Serialiser	415.5 mV
Dropout_Voltage_AB	378.3 mV
PWR_Additional_SHUNT	32.5 %
PWR_Efficiency_SHUNT	75.47 %
I_OVP_final	503.7 uA
Vstress_AB	eval err
Vstress_Serialiser	eval err
Vstress_Digital_OVP	eval err
Vstress_Analog	eval err
Vstress_Services	eval err
Vin_relVSS_final	1.617 V
PWR_TOT	3.521 W
PWR_TOT_Load	1.903 W
PWR_TOT_Shunt	618.4 mW
PWR_Additional_TOT	85.05 %
PWR_Efficiency_TOT	54.04 %
Chain_Current	1.799 A
Chain_Voltage	1.958 V
Drop - Trace Upper	170.1 mV
Drop - Trace Lower	170.1 mV
PWR_GD_In<0>	1.862 W
PWR_GD_Load<0>	1.454 W
PWR_GD_Shunt<0>	408.3 mW
PWR_GA_In<0>	413.9 mW
PWR_GA_Load<0>	308.5 mW
PWR_GA_Shunt<0>	105.4 mW
PWR_SERV_In<0>	96.11 mW
PWR_SERV_Load<0>	55.94 mW
PWR_SERV_Shunt<0>	40.17 mW
PWR_Serialiser_In<0>	148.6 mW
PWR_Serialiser_Load<0>	84.04 mW
PWR_Serialiser_Shunt<0>	64.59 mW

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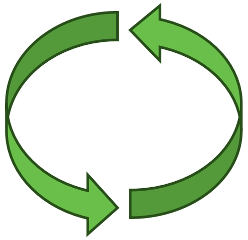
Calibration

- Have developed a calibration procedure for this, which runs as a pre-run script before every simulation. Actual simulation then runs with the parameters from calibration

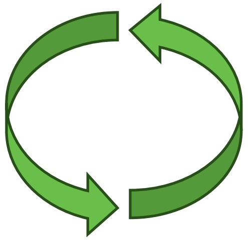
- Procedure is:

1. Calibrate DAC
    1. Set OVP limit and chain current to high values
    2. Measure values at 0, 15 and 31 (why?)
    3. Determine code needed for target output voltage

2. Determine required chain current
    1. Set current to default
    2. Check that all SLDOs have started up (in practice, that their voltage exceeds 1V)
    3. Increase current by 5%



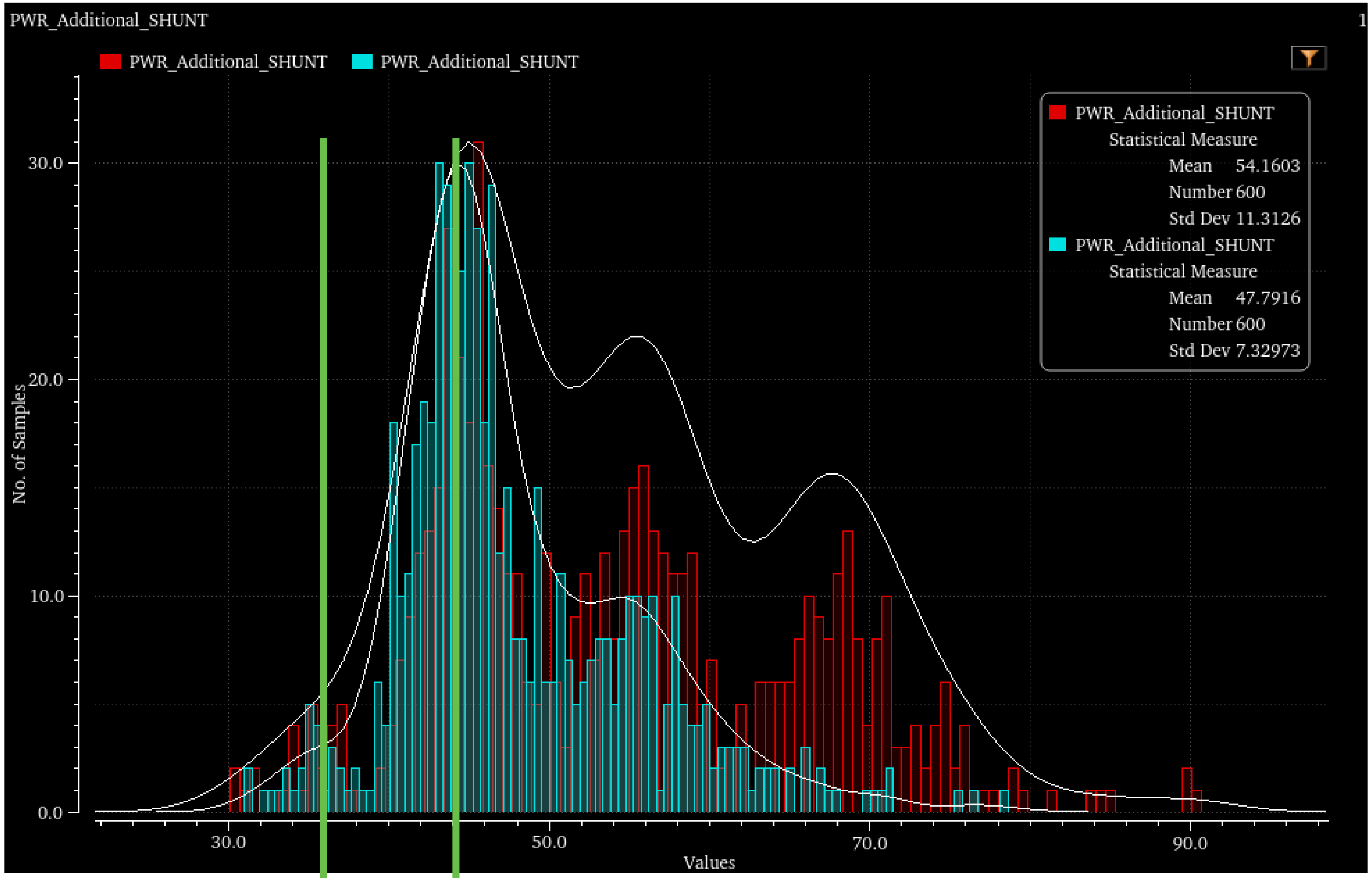
3. Determine required OVP level
    1. Set level to default
    2. Check that output voltages same as previous step and OVP off (how?)
    3. Increase OVP limit



Monte Carlo

Efficiency

- Power efficiency was reported previously as the power added by the shunt as a percentage
- Show in the histograms on this slide for 0.15ohm (red) and 0 ohm (blue) cases
- Range of ~30-70% (90% for the 0.15 ohm case)
- Was previously 25-40%
- Not the supply resistance. So why the increase?



Range from MPW2 sims

2 possible reasons identified…

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Monte Carlo

Efficiency Improvement – Constant Voltage vs. Constant Current Source

- Look back at old MPW2 simulations
- These were simulated with a constant **voltage** source
- For SLDO_5, moved to a constant **current** source, since is ultimately what is intended
- This is causing an efficiency issue because the required start-up current exceeds the steady state current in some corners and mis-match scenarios
- However, the tuning script increases the current until everything can start then leaves it there. For runs that needed a high start-up current this extra current is then shunted and leads to a loss of power efficiency

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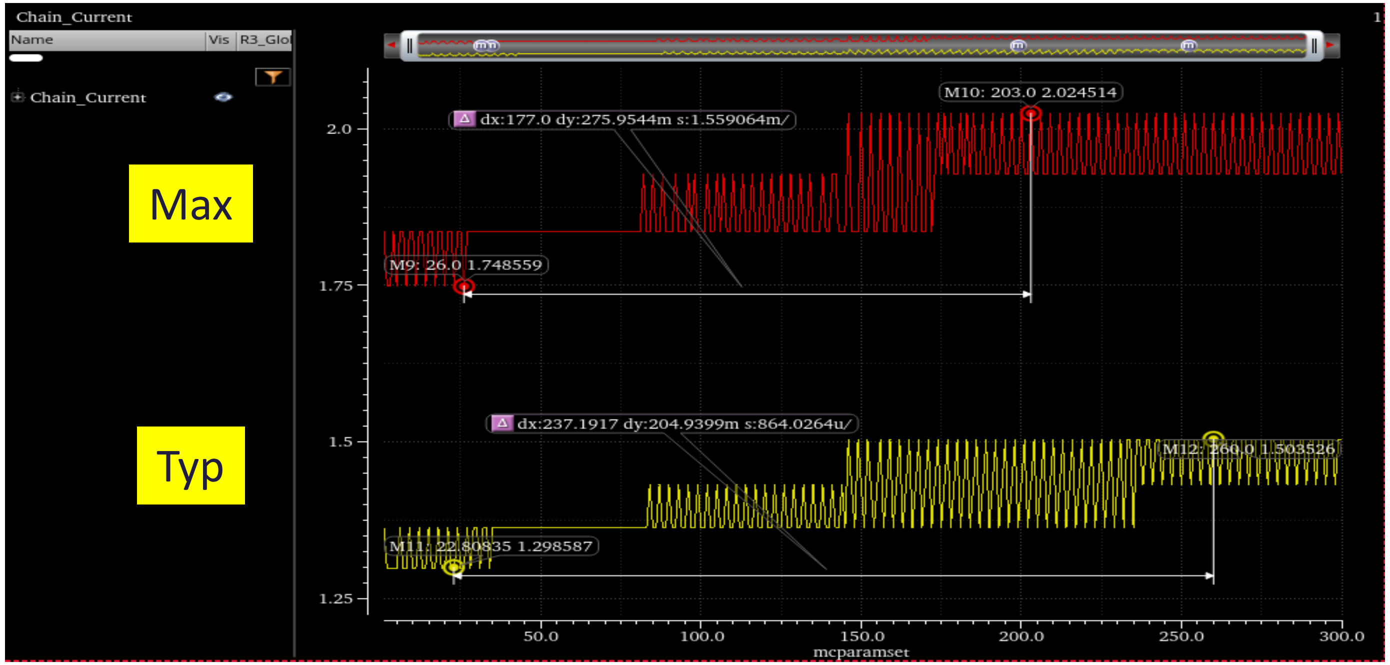
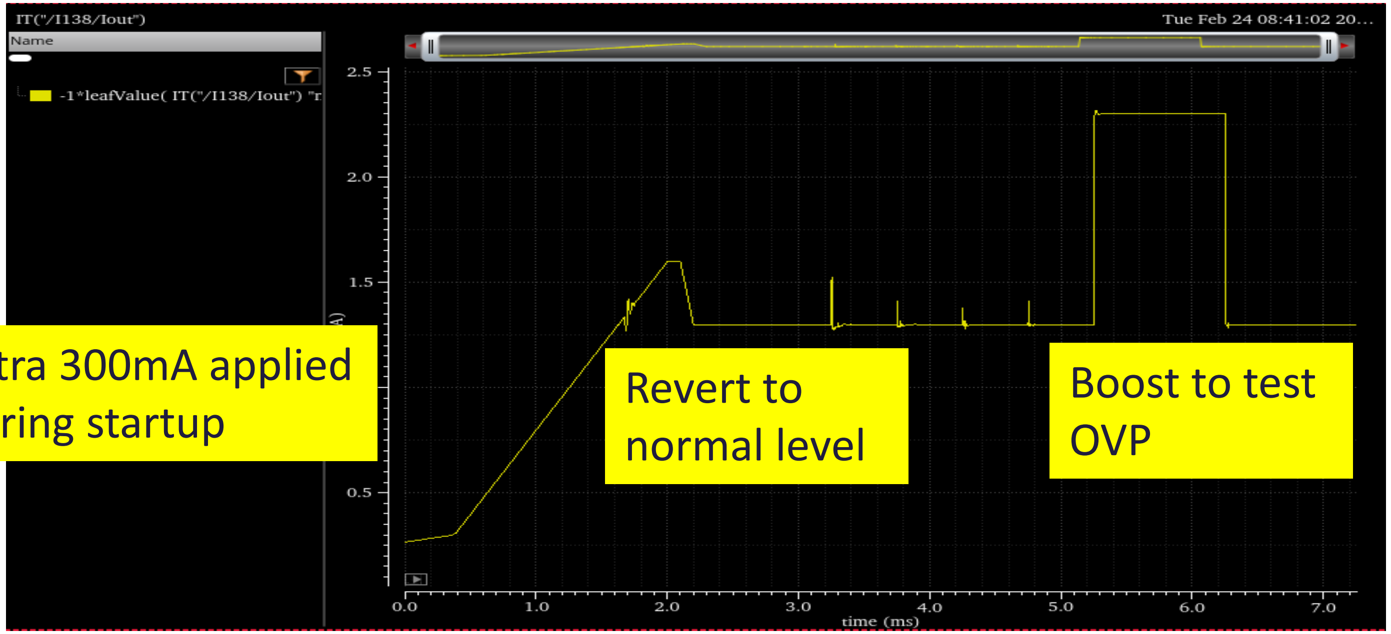
Efficiency Improvement – Constant Voltage vs. Constant Current Source

- Apply slightly higher current during startup only, then reduce
- Ensures startup, then highest efficiency
- Also realistic for waferprobing, calibration and operation
- Added advantage that it reduces the number of current calibration steps
- Chain current levels in steady state now match calculations (load+10%). Higher current only needed to startup.
- Note that this effectively also changes the ramp rate. It could be that ramp rate is the critical factor.



Max

Typ



Extra 300mA applied during startup

Revert to normal level

Boost to test OVP

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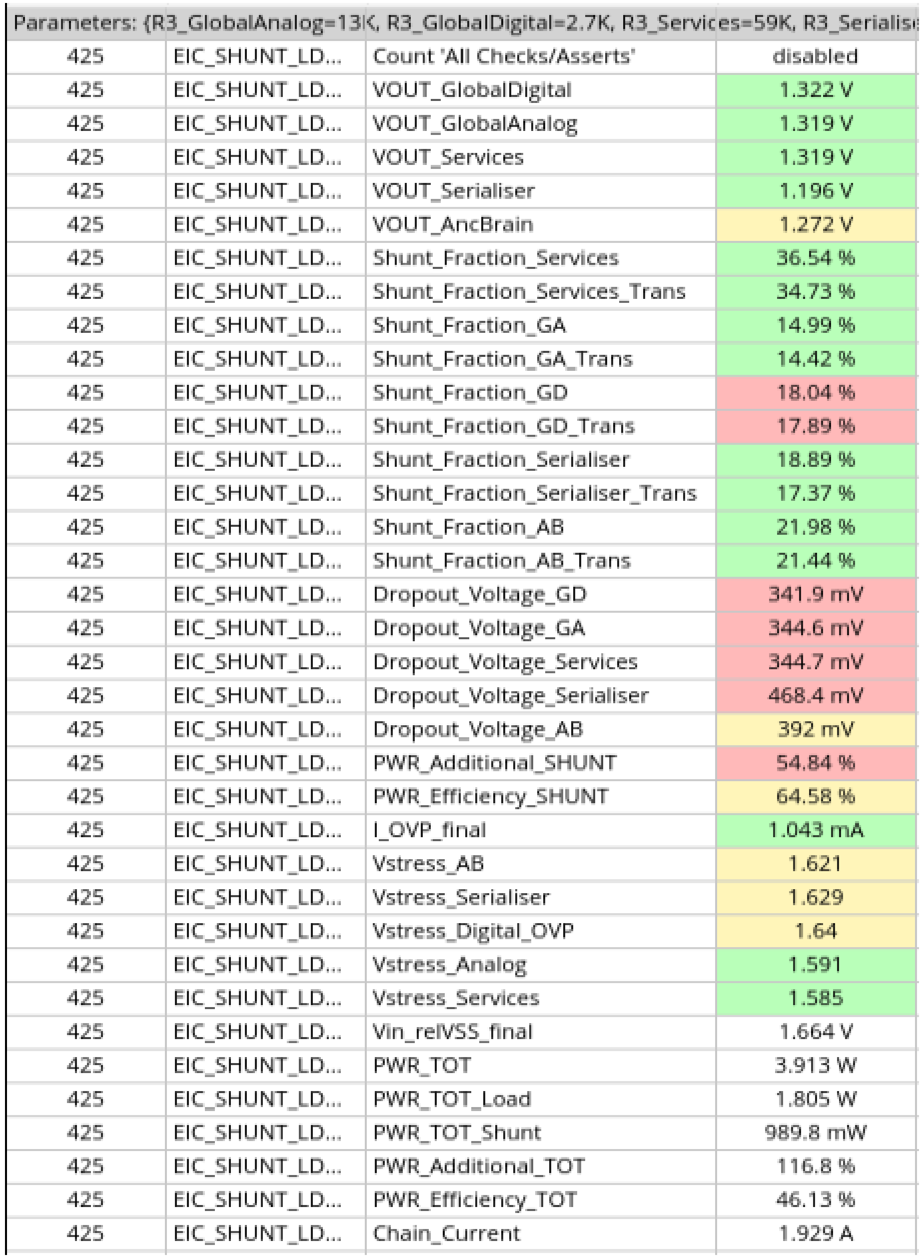
Efficiency Improvement – Increase of Current During Calibration

- Calibration procedure demonstrated previously involved **increasing the shunt current** when certain devices did not start
- However, looking at the results indicated that most of this current was then shunted away. Here is a classic example where current has increased from 1.8A to 1.93A, but GlobalDigital is now shunting 18%, not the target of 10%. This is ~84mA i.e. most of the current increase.
- Believe that what is happening is that there is mismatch between the equivalent resistances of the 5 SLDOs. This leads to current split being incorrect. In some cases, this pushes the shunted current of some supplies below the level at which the load overcurrent shutdown is triggered.
- The calibration procedure increases the current to stop this happening, but this increases the shunted current in all the SLDOs. If the split is also not what was intended, the situation is worse



Parameters: {R3_GlobalAnalog=13K, R3_GlobalDigital=2.7K, R3_Services=59K, R3_Serialise

425	EIC_SHUNT_LD...	Count 'All Checks/Asserts'	disabled
425	EIC_SHUNT_LD...	VOUT_GlobalDigital	1.322 V
425	EIC_SHUNT_LD...	VOUT_GlobalAnalog	1.319 V
425	EIC_SHUNT_LD...	VOUT_Services	1.319 V
425	EIC_SHUNT_LD...	VOUT_Serialiser	1.196 V
425	EIC_SHUNT_LD...	VOUT_AncBrain	1.272 V
425	EIC_SHUNT_LD...	Shunt_Fraction_Services	36.54 %
425	EIC_SHUNT_LD...	Shunt_Fraction_Services_Trans	34.73 %
425	EIC_SHUNT_LD...	Shunt_Fraction_GA	14.99 %
425	EIC_SHUNT_LD...	Shunt_Fraction_GA_Trans	14.42 %
425	EIC_SHUNT_LD...	Shunt_Fraction_GD	18.04 %
425	EIC_SHUNT_LD...	Shunt_Fraction_GD_Trans	17.89 %
425	EIC_SHUNT_LD...	Shunt_Fraction_Serialiser	18.89 %
425	EIC_SHUNT_LD...	Shunt_Fraction_Serialiser_Trans	17.37 %
425	EIC_SHUNT_LD...	Shunt_Fraction_AB	21.98 %
425	EIC_SHUNT_LD...	Shunt_Fraction_AB_Trans	21.44 %
425	EIC_SHUNT_LD...	Dropout_Voltage_GD	341.9 mV
425	EIC_SHUNT_LD...	Dropout_Voltage_GA	344.6 mV
425	EIC_SHUNT_LD...	Dropout_Voltage_Services	344.7 mV
425	EIC_SHUNT_LD...	Dropout_Voltage_Serialiser	468.4 mV
425	EIC_SHUNT_LD...	Dropout_Voltage_AB	392 mV
425	EIC_SHUNT_LD...	PWR_Additional_SHUNT	54.84 %
425	EIC_SHUNT_LD...	PWR_Efficiency_SHUNT	64.58 %
425	EIC_SHUNT_LD...	I_OVP_final	1.043 mA
425	EIC_SHUNT_LD...	Vstress_AB	1.621
425	EIC_SHUNT_LD...	Vstress_Serialiser	1.629
425	EIC_SHUNT_LD...	Vstress_Digital_OVP	1.64
425	EIC_SHUNT_LD...	Vstress_Analog	1.591
425	EIC_SHUNT_LD...	Vstress_Services	1.585
425	EIC_SHUNT_LD...	Vin_relVSS_final	1.664 V
425	EIC_SHUNT_LD...	PWR_TOT	3.913 W
425	EIC_SHUNT_LD...	PWR_TOT_Load	1.805 W
425	EIC_SHUNT_LD...	PWR_TOT_Shunt	989.8 mW
425	EIC_SHUNT_LD...	PWR_Additional_TOT	116.8 %
425	EIC_SHUNT_LD...	PWR_Efficiency_TOT	46.13 %
425	EIC_SHUNT_LD...	Chain_Current	1.929 A

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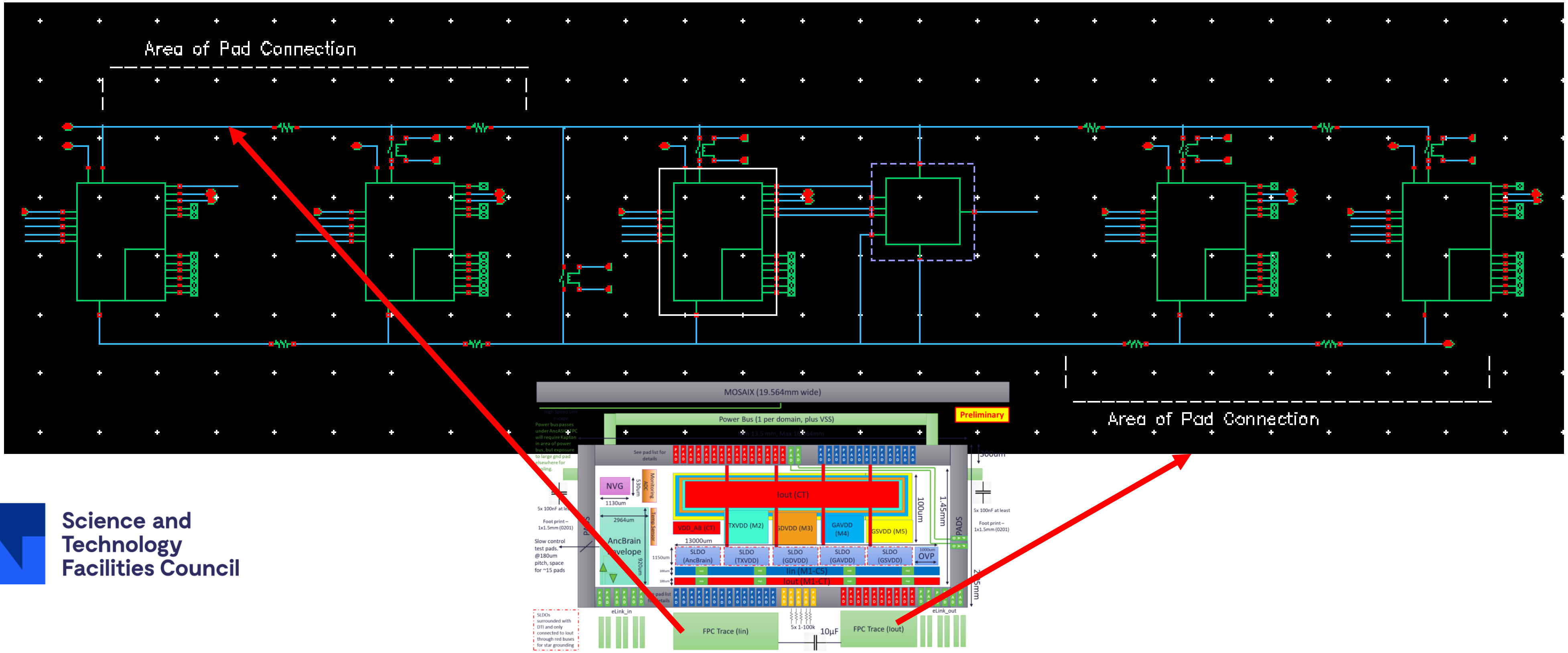
SLDO_5

Power Bus Resistances

Power Bus Resistances

Model

- Input power buses are M3-CT stripes, 200um wide, ~75% occupancy
- Estimate 0.6 ohm resistance, split into 4 segments of 0.15
- Set left hand 2 of Iin to 0 and right hand 2 of Iout to 0 to represent pad locations
- Pads and bond wires present. Pads have no resistance. 5mm bondwire = 0.25 ohm

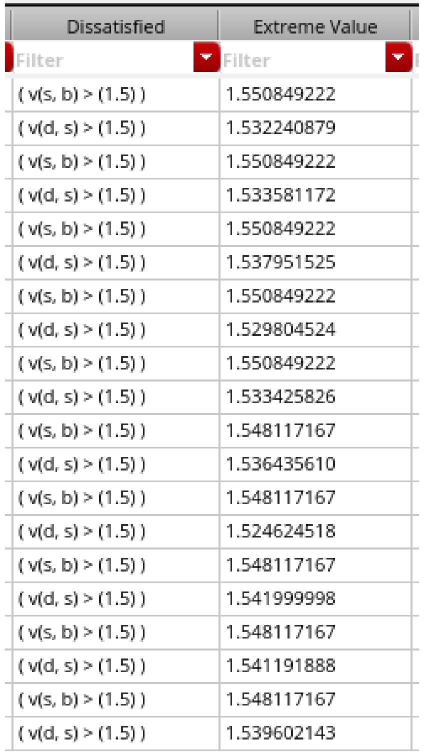


Power Bus Resistances

Effect of Power Bus Resistance

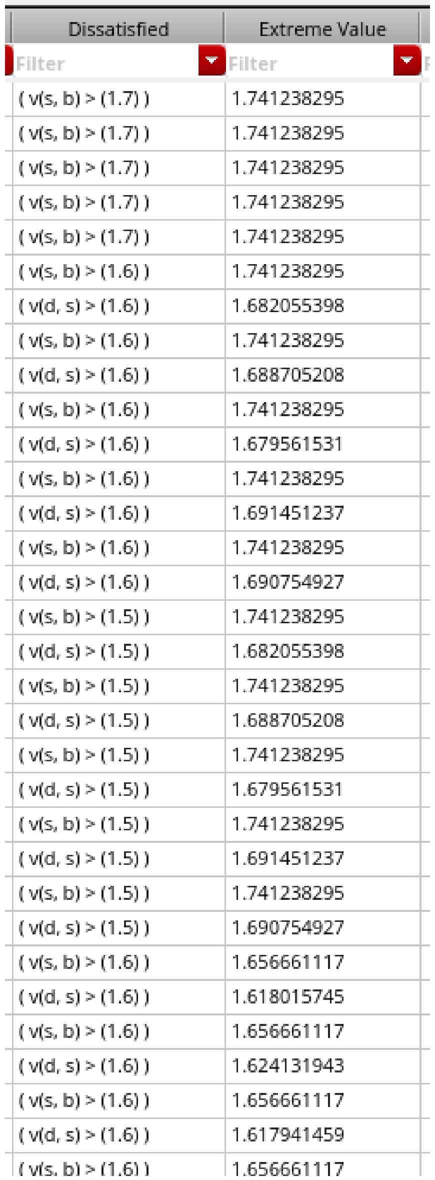
- Device can remain functional for power bus resistances of 1 ohm (i.e. 4 ohms total)
- Achieving this require increasing the current supply, and increasing the OVP voltage limit
- This leads to reduced efficiency (the cost of continuing to function)
- At the 1 ohm level, devices are still within the “abs” operating range, but getting a bit close…
- Select 0.15 ohms as this maintains effectively the same performance as 0 ohm

0.15 ohm

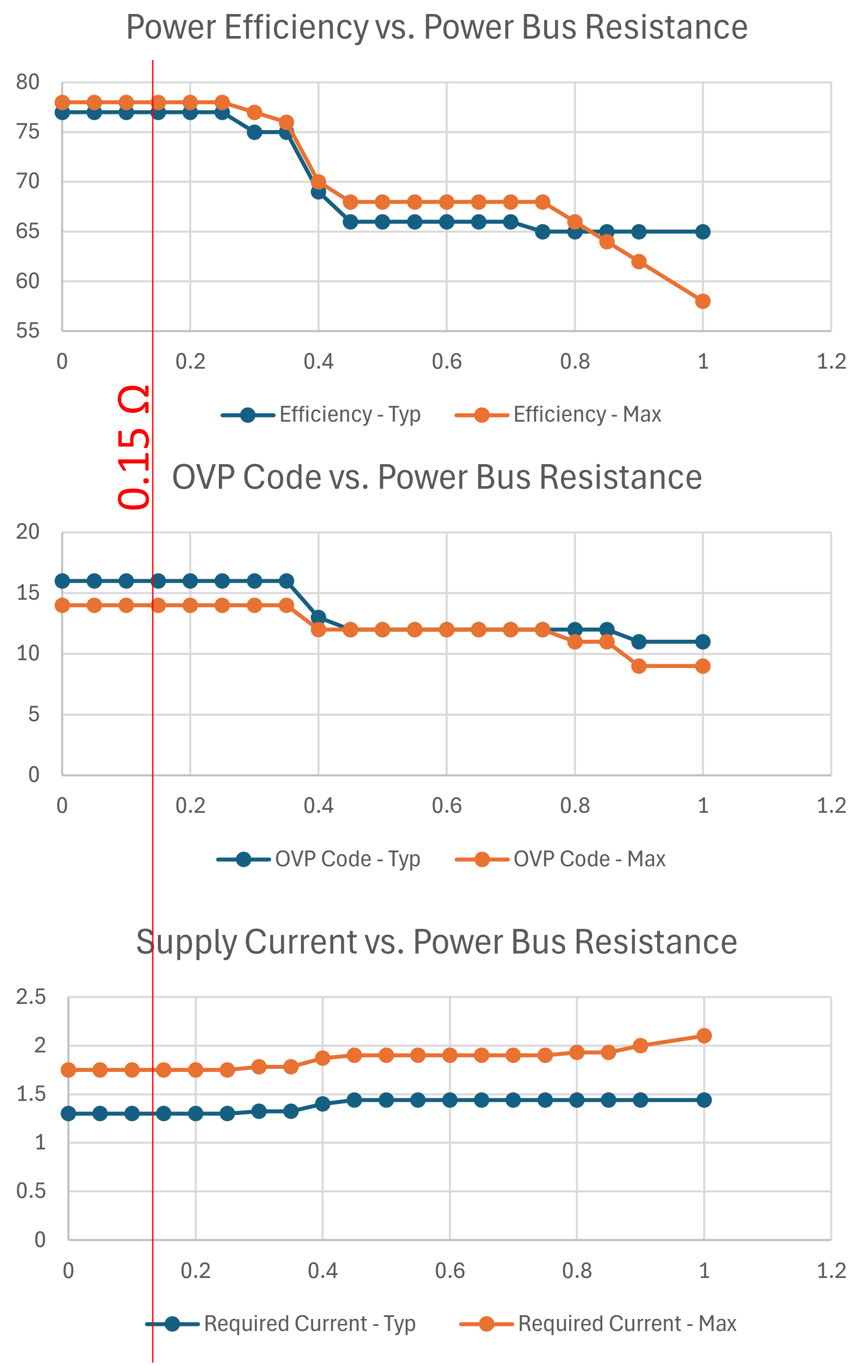


Dissatisfied	Extreme Value
Filter	Filter
(v(s, b) > (1.5))	1.550849222
(v(d, s) > (1.5))	1.532240879
(v(s, b) > (1.5))	1.550849222
(v(d, s) > (1.5))	1.533581172
(v(s, b) > (1.5))	1.550849222
(v(d, s) > (1.5))	1.537951525
(v(s, b) > (1.5))	1.550849222
(v(d, s) > (1.5))	1.529804524
(v(s, b) > (1.5))	1.550849222
(v(d, s) > (1.5))	1.533425826
(v(s, b) > (1.5))	1.548117167
(v(d, s) > (1.5))	1.536435610
(v(s, b) > (1.5))	1.548117167
(v(d, s) > (1.5))	1.524624518
(v(s, b) > (1.5))	1.548117167
(v(d, s) > (1.5))	1.541999998
(v(s, b) > (1.5))	1.548117167
(v(d, s) > (1.5))	1.541191888
(v(s, b) > (1.5))	1.548117167
(v(d, s) > (1.5))	1.539602143

1 ohm



Dissatisfied	Extreme Value
Filter	Filter
(v(s, b) > (1.7))	1.741238295
(v(s, b) > (1.7))	1.741238295
(v(s, b) > (1.7))	1.741238295
(v(s, b) > (1.7))	1.741238295
(v(s, b) > (1.7))	1.741238295
(v(s, b) > (1.6))	1.741238295
(v(d, s) > (1.6))	1.682055398
(v(s, b) > (1.6))	1.741238295
(v(d, s) > (1.6))	1.688705208
(v(s, b) > (1.6))	1.741238295
(v(d, s) > (1.6))	1.679561531
(v(s, b) > (1.6))	1.741238295
(v(d, s) > (1.6))	1.691451237
(v(s, b) > (1.6))	1.741238295
(v(d, s) > (1.6))	1.690754927
(v(s, b) > (1.5))	1.741238295
(v(d, s) > (1.5))	1.682055398
(v(s, b) > (1.5))	1.741238295
(v(d, s) > (1.5))	1.688705208
(v(s, b) > (1.5))	1.741238295
(v(d, s) > (1.5))	1.679561531
(v(s, b) > (1.5))	1.741238295
(v(d, s) > (1.5))	1.691451237
(v(s, b) > (1.5))	1.741238295
(v(d, s) > (1.5))	1.690754927
(v(s, b) > (1.6))	1.656661117
(v(d, s) > (1.6))	1.618015745
(v(s, b) > (1.6))	1.656661117
(v(d, s) > (1.6))	1.624131943
(v(s, b) > (1.6))	1.656661117
(v(d, s) > (1.6))	1.617941459
(v(s, b) > (1.6))	1.656661117



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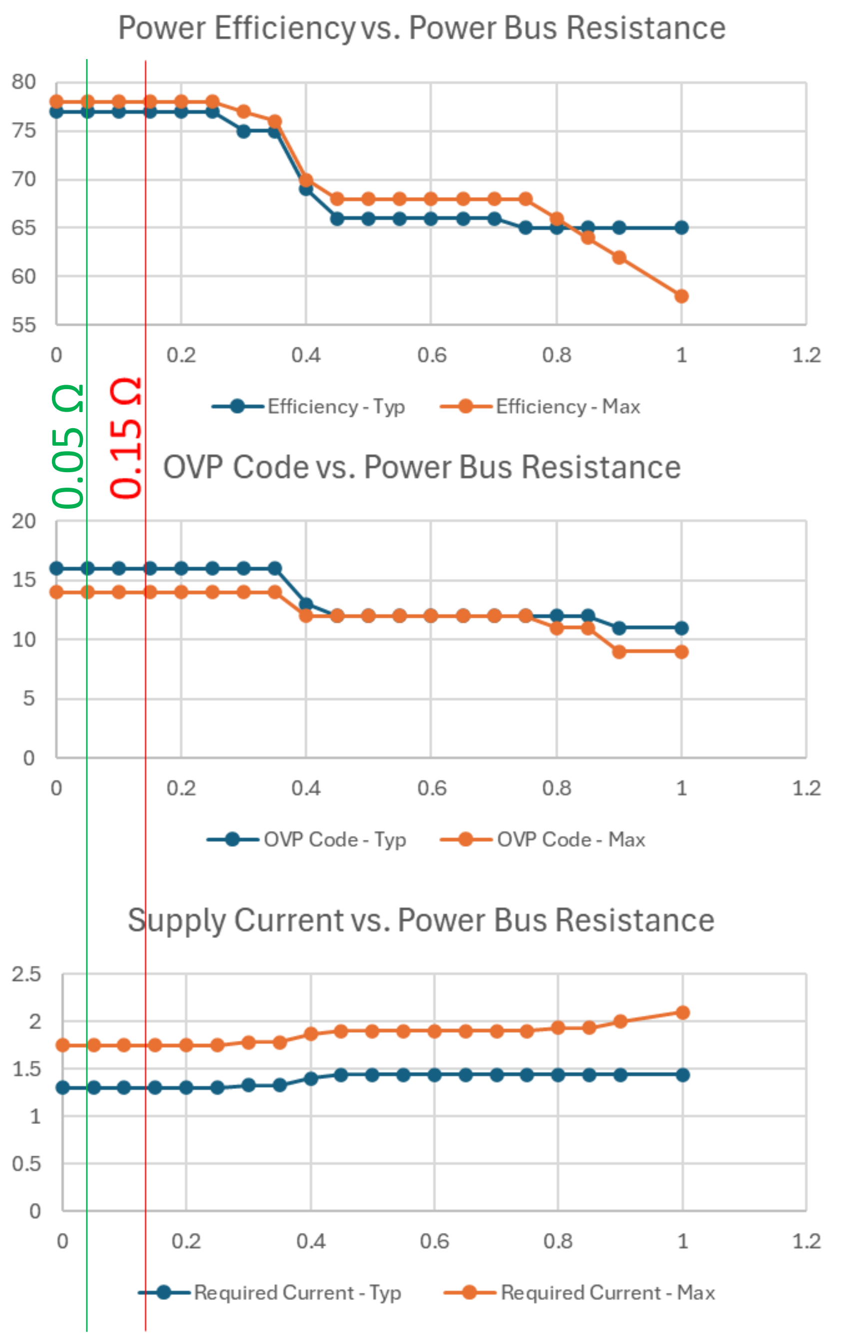
Extracted

Resistance values

- Bus resistance values can be extracted from the parasitics tool, and from simulation
- Result is well below previous estimates

Supply	Resistance (mohm)	Notes
Iin	110	Represents the full bus resistance from the block of input pads to a nominal test point on the other side
Iout	196	Represents the full bus resistance from the block of input pads to a nominal test point on the other side
GDVDD	29.1	
GAVDD	29.0	
TXVDD	29.3	
GSVDD	30.8	
ABVDD	12.7	



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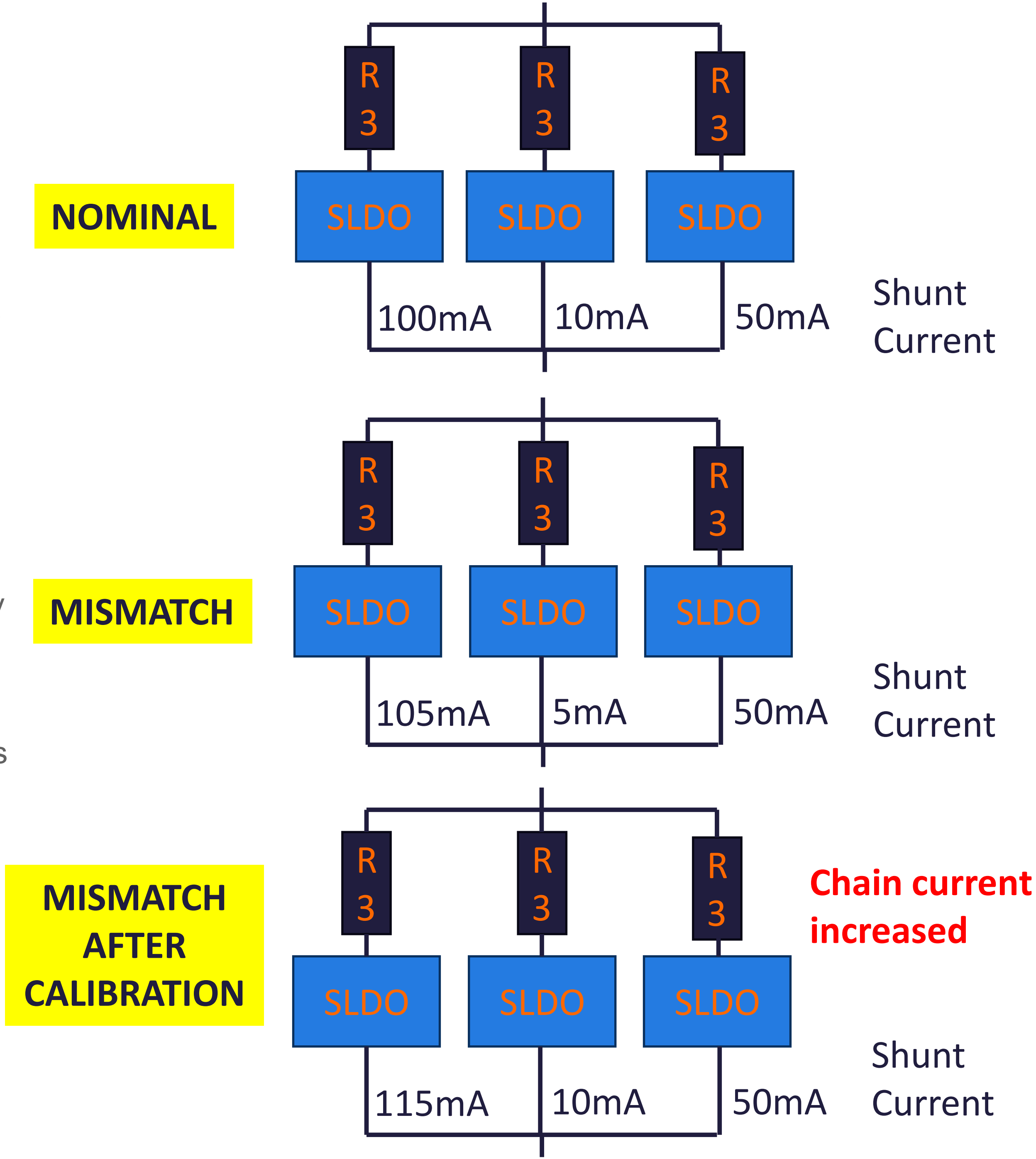
Calibration

R3 Calibration

- An example of this is in the diagrams to the right. Imagine 3 SLDOs with currents of 1A, 100mA and 500mA. Nominal shunt percentage of 10% would lead to the shunt current shown.
- Mis-match within the device will lead to non nominal spread. Since 5mA is below the 10ma threshold for detecting a load overcurrent and shutting down, the middle device shuts off
- This can be corrected by increasing the shunt current, but the incorrect split of current still exists, so the chain current actually needs to be increased by more than the “missing” 5mA, and even more current is wasted in the other SLDOs
- The solution to this is to increase not the chain current, which is global, but to decrease R3 for supplies that do not start, compensating instead for the individual mismatch



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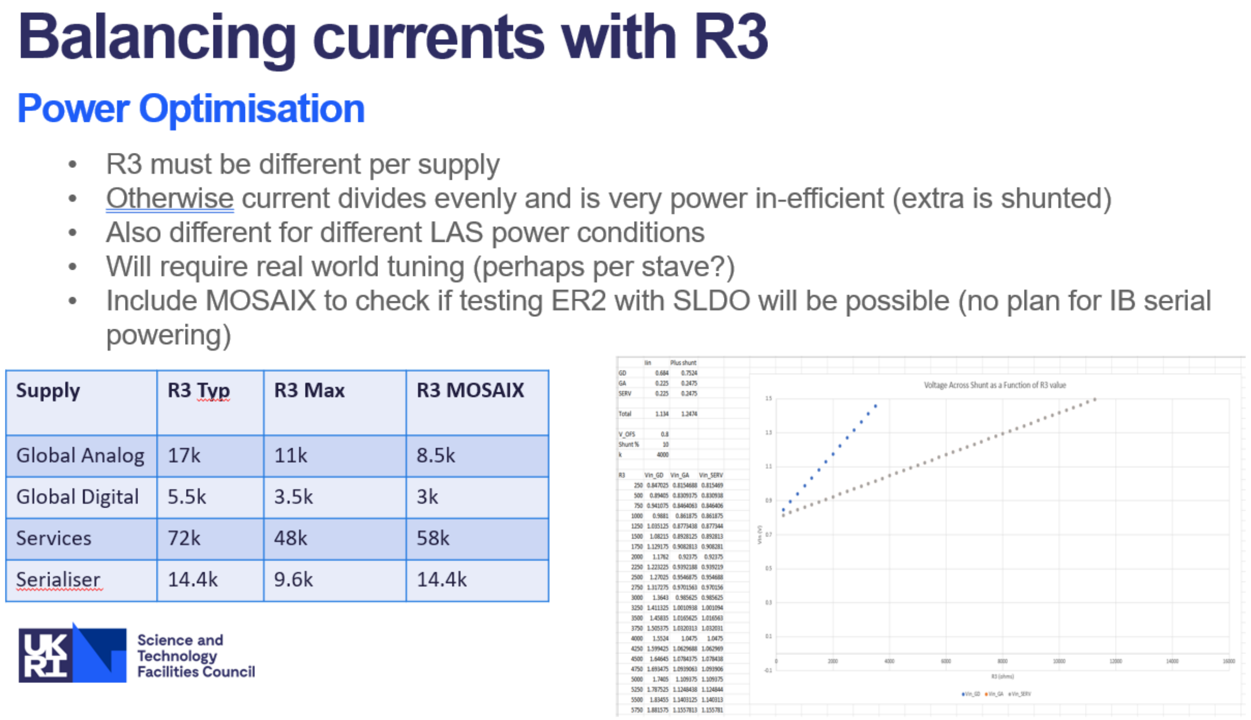
Calibration

Additional Points

- Two important further notes on this:
    - This is actually a power caveat mentioned during MPW2 design, but was at the time thought of in the context of R3 tolerance. We can now see same effect occurs due to SLDO mis-match.
    - This is only really happening because we operate in Mode 0. In Mode 1, everything will probably start because the shut down is not enabled. Have not tested this. It would still have a lower shunt percentage however.



Balancing currents with R3

Power Optimisation

- R3 must be different per supply
- Otherwise current divides evenly and is very power in-efficient (extra is shunted)
- Also different for different LAS power conditions
- Will require real world tuning (perhaps per stave?)
- Include MOSAIX to check if testing ER2 with SLDO will be possible (no plan for IB serial powering)

Supply	R3 Typ	R3 Max	R3 MOSAIX
Global Analog	17k	11k	8.5k
Global Digital	5.5k	3.5k	3k
Services	72k	48k	58k
Serialiser	14.4k	9.6k	14.4k

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	Iin	Plus shunt
GD	0.684	0.7524
GA	0.225	0.2475
SERV	0.225	0.2475
Total	1.134	1.2474
V_OFS	0.8	
Shunt %	10	
k	4000	

R3	Vin_GD	Vin_GA	Vin_SERV
250	0.847025	0.8154688	0.815469
500	0.89405	0.8309375	0.830938
750	0.941075	0.8464063	0.846406
1000	0.9881	0.861875	0.861875
1250	1.035125	0.8773438	0.877344
1500	1.08215	0.8928125	0.892813
1750	1.129175	0.9082813	0.908281
2000	1.1762	0.92375	0.92375
2250	1.223225	0.9392188	0.939219
2500	1.27025	0.9546875	0.954688
2750	1.317275	0.9701563	0.970156
3000	1.3643	0.985625	0.985625
3250	1.411325	1.0010938	1.001094
3500	1.45835	1.0165625	1.016563
3750	1.505375	1.0320313	1.032031
4000	1.5524	1.0475	1.0475
4250	1.599425	1.0629688	1.062969
4500	1.64645	1.0784375	1.078438
4750	1.693475	1.0939063	1.093906
5000	1.7405	1.109375	1.109375
5250	1.787525	1.1248438	1.124844
5500	1.83455	1.1403125	1.140313
5750	1.881575	1.1557813	1.155781

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