



EIC-AncBRAIN:

A Slow Control & Communication Management System of AncASIC

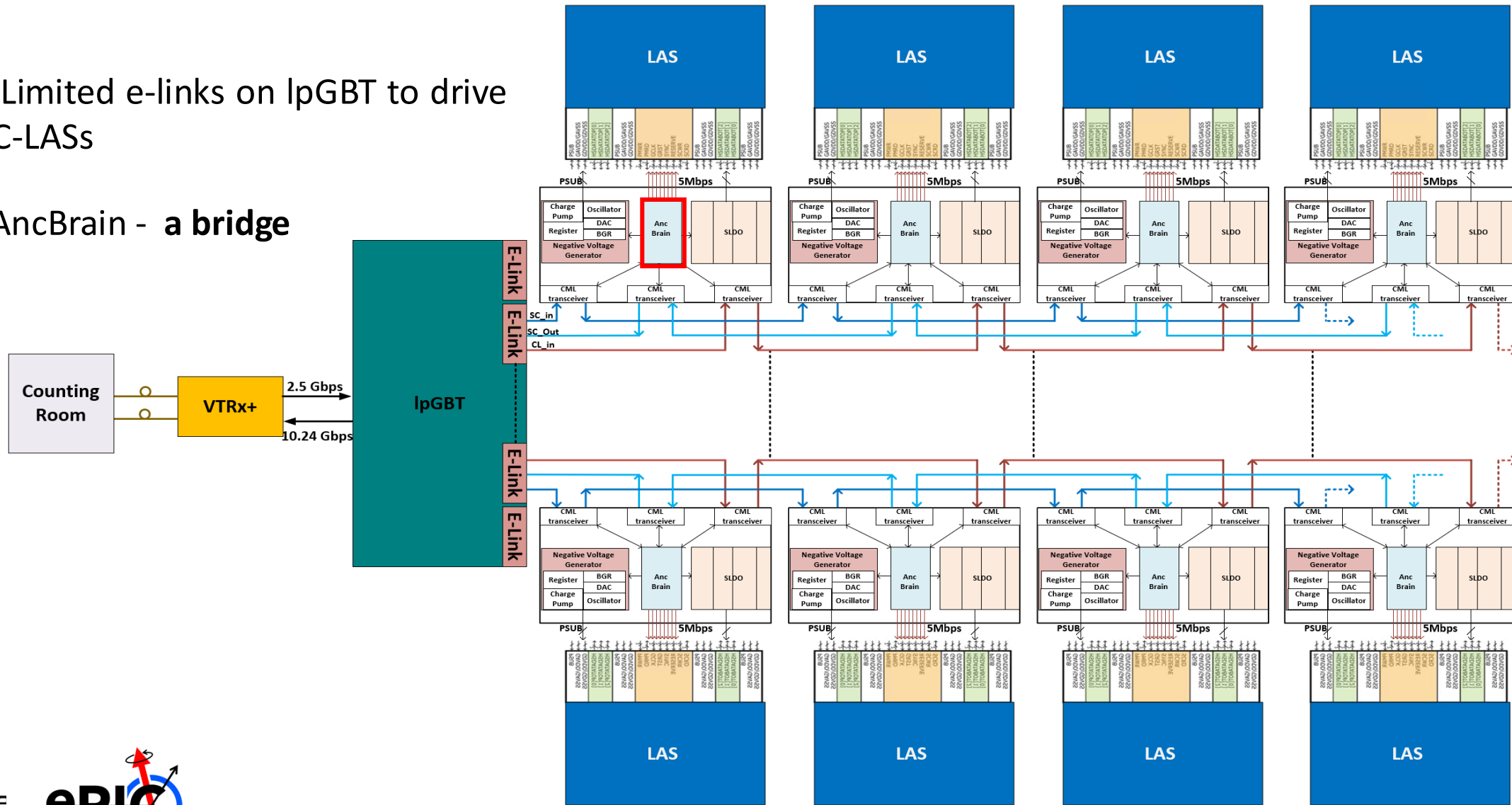
Date: 03/31/2026

Contribution: Arif Iqbal, Dominik Gorni, Grzegorz W. Deptuch



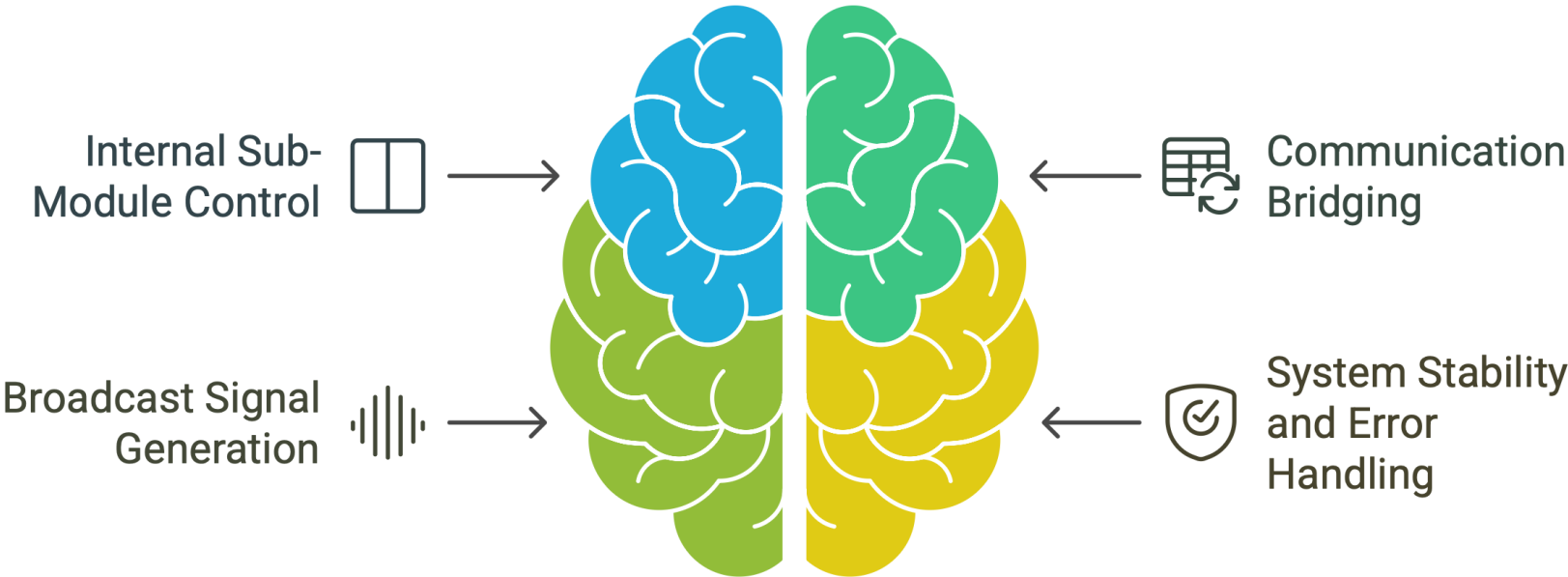
The Bottleneck

- **Challenge:** Limited e-links on IpGBT to drive multiple EIC-LASs
- **Solution:** AncBrain - a bridge

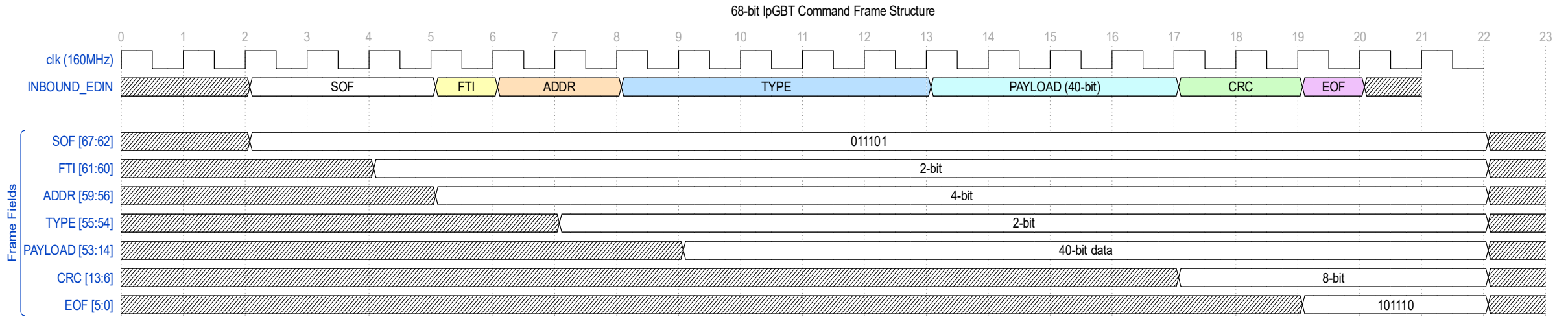


AncBrain: Key Functionalities

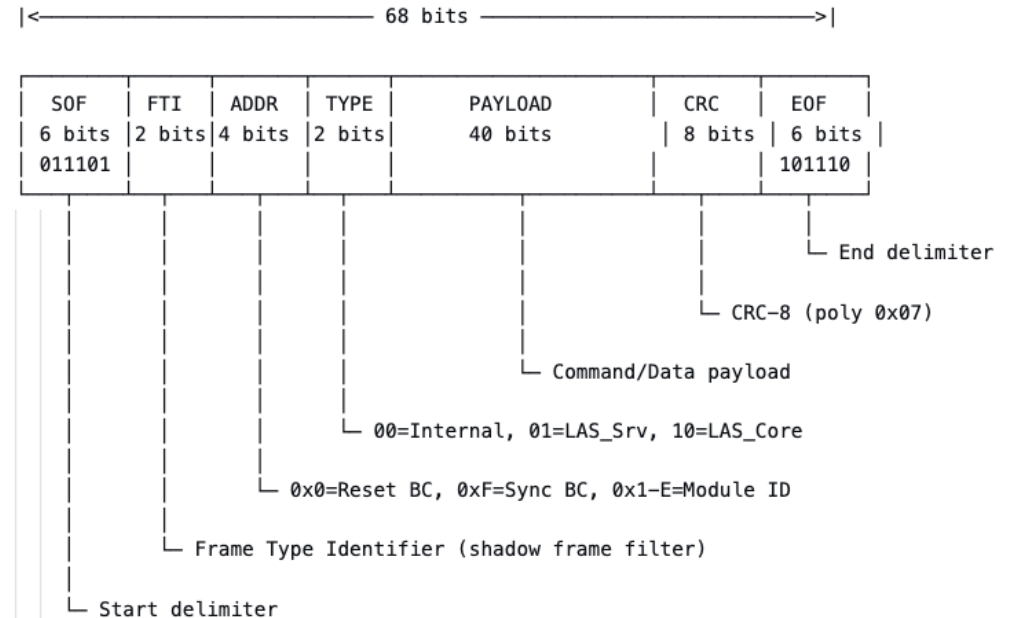
Core Operations Inside AncBrain



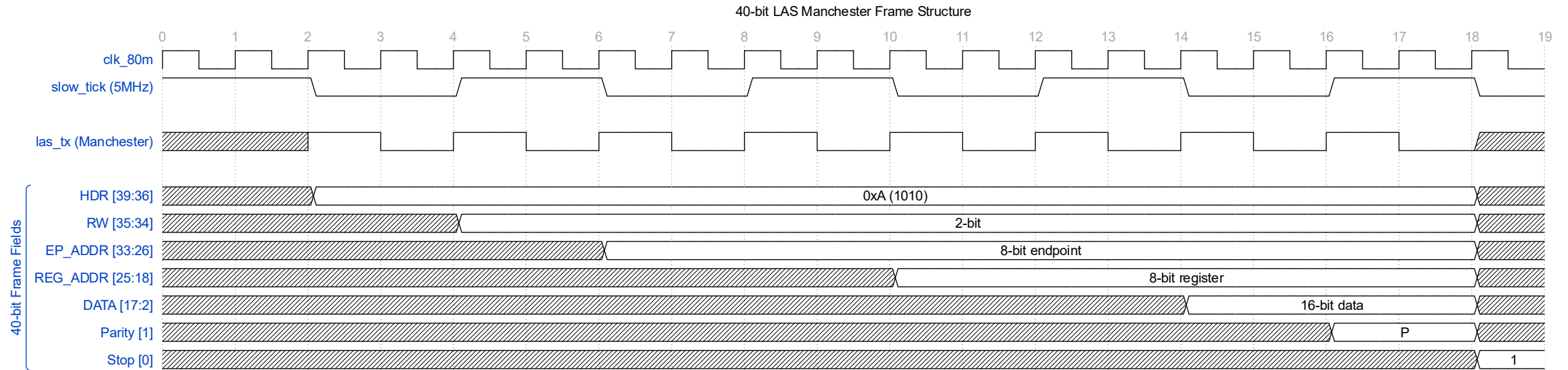
68-bit Frame



Total: 68 bits | SOF=6'b011101, EOF=6'b101110 | FTI=2-bit Frame Type ID | CRC-8 poly=0x07 (over bits [59:14])



40-bit MOSAIX Payload



Manchester encoded @ 5Mbps effective | Half-bit: 50-125ns | Full-bit: 150-225ns

40-bit LAS Payload (DATA_TYPE_LAS_SRV = 2'b01 / DATA_TYPE_LAS_CORE = 2'b10)

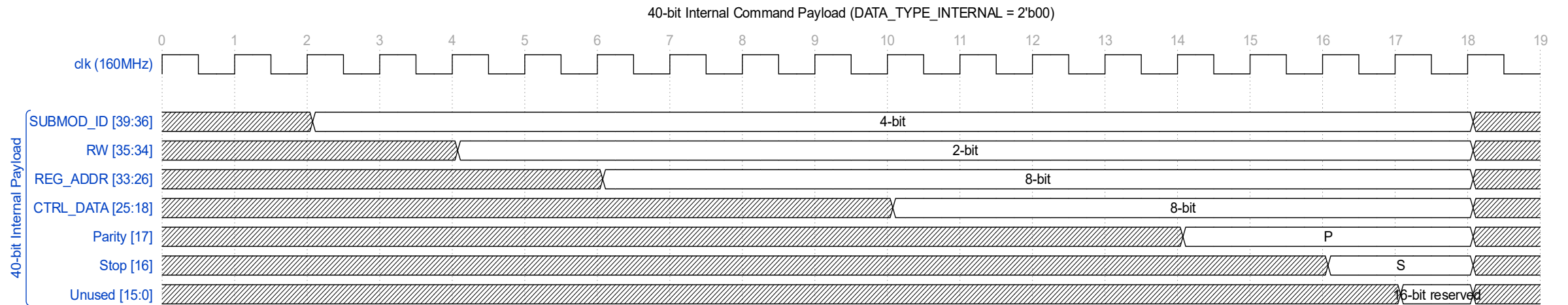
← 40 bits →

HDR	OPCODE	EP_ADDR	REG_ADDR	REG_DATA	P	STOP
4 bits	2 bits	8 bits	8 bits	16 bits	1 b	1 b
1010						1



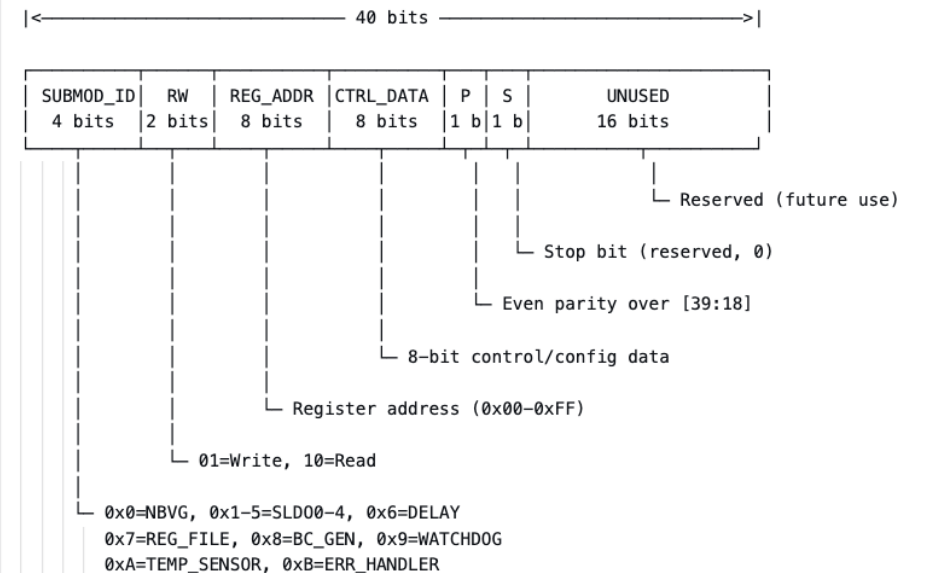
Manchester encoded @ 5Mbps effective | Half-bit: 50-125ns | Full-bit: 150-225ns

40-bit Internal Payload



Parity: even parity over bits [39:18] | RW: 01=Write, 10=Read

40-bit Internal Command Payload (DATA_TYPE_INTERNAL = 2'b00)



Error Map

TIER 0: CRITICAL SYSTEM ERRORS (Safety-Critical)

Code	Error Name	Tier	Priority	Sev	Status	Integration	Source Module	Implementation Notes
0x01	ERR_TEMP_CRITICAL	T0	4	CRIT	X	IMM	temp_sensor	TODO: Add temp sensor + comparator**
0x02	ERR_POWER_FAILURE	T0	2	CRIT	X	IMM	power_monitor	Active: follow the overcurrent signal from SLDO May require masking other error signals
0x04	ERR_VOLTAGE_OUT_RANGE	T0	4	CRIT	X	IMM	voltage_monitor	TODO: Comparator

**should there be any on chip action by AncBrain for overheating is under discussion and maybe included for future versions.

TIER 1: COMMUNICATION/LINK ERRORS

Code	Error Name	Tier	Priority	Sev	Status	Integration	Source Module	Implementation Notes
0x10	ERR_PROTOCOL_ERROR	T1	-	ERR	X	HYB	frame_chk	TODO: Add protocol violation detector or check if other link layer error signal serve the same purpose
0x11	ERR_CRC_ERROR	T1	-	ERR	✓	REG	frame_chk	Reg only. Control room will do the polling
0x14	ERR_DATA_TYPE_ERROR	T1	11	ERR	✓	IMM	cmd_parser	Active: data_type_err_pulse (reserved type 0b11)
0x19	ERR_LAS_TIMEOUT_NO_RESPONSE	T1	13	ERR	✓	IMM	LAS interface	Active: las_timeout_pulse
0x1C	ERR_LINK_FAILURE	T1	45	ERR	✓ (Partial)	IMM	deser65	Active: link_failure_pulse (SOF timeout 5ms) actual timeout will be configured after the completion of the design with all the timing analysis at hand

TIER 2: COMMAND VALIDATION ERRORS

Code	Error Name	Tier	Priority	Sev	Status	Integration	Source Module	Implementation Notes
0x20	ERR_PARITY_ERROR	T2	24	ERR	✓	IMM	cmd_parser	Active: parity_err_pulse
0x21	ERR_INVALID_COMMAND	T2	20	ERR	✓	IMM	cmd_parser	Active: invalid_cmd_pulse (no valid type)
0x23	ERR_INVALID_ADDRESS	T2	25	ERR	✓	IMM	cmd_parser	Active: invalid_addr_pulse + subcode (addr)
0x24	ERR_INVALID_RW_FIELD	T2	21	ERR	✓	IMM	cmd_parser	Active: invalid_rw_pulse
0x25	ERR_PAYLOAD_STRUCTURE	T2	22	ERR	✓	IMM	cmd_parser	Active: payload_struct_pulse (unused ≠ 0)
0x26	ERR_COMMAND_LENGTH	T2	23	ERR	✓	IMM	cmd_parser	Active: cmd_length_pulse

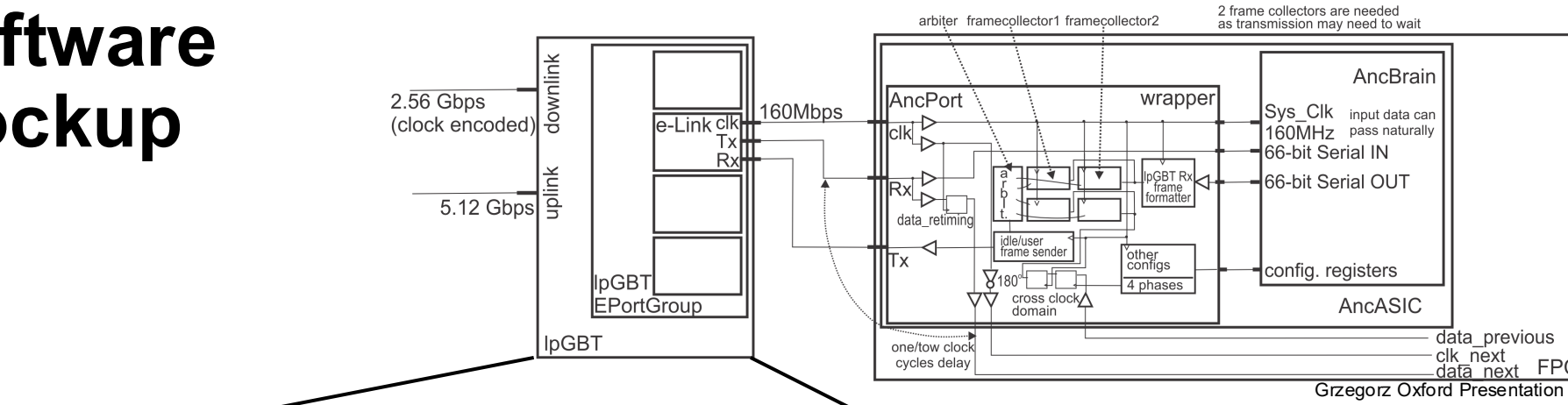
TIER 3: EXECUTION LAYER ERRORS

Code	Error Name	Tier	Priority	Sev	Status	Integration	Source Module	Implementation Notes
0x36	ERR_OPERATION_FAILED	T2	-	ERR	✓	IMM	core_fsm	Active: operation_failed_pulse (LAS done, no valid resp)
0x37	ERR_STATE_VIOLATION	T2	-	ERR	✓	IMM	core_fsm	Active: state_violation_pulse (invalid FSM transition)

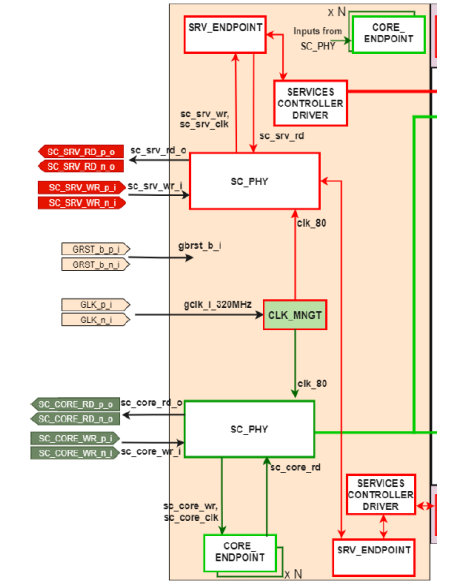
TIER 4: INTERNAL/DEBUG ERRORS

Code	Error Name	Tier	Priority	Sev	Status	Integration	Source Module	Implementation Notes
0xF0	ERR_INTERNAL_ERROR	T4	40	INFO	✓	IMM	core_fsm	Active: internal_err_pulse (timeout in RESPONSE_WAIT)
0xF1	ERR_SIMULATION_ERROR	T4	41	INFO	✓	SUP	testbench	Sim only: Testbench error injection
0xF2	ERR_DEBUG_ASSERTION	T4	42	INFO	✓	SUP	assertions	Sim only: SVA assertion failure
0xF3	ERR_COVERAGE_ERROR	T4	43	INFO	✓	SUP	coverage	Sim only: Coverage collection issue
0xFF	ERR_UNKNOWN	T4	44	INFO	✓	IMM	core_fsm	Active: unknown_err_pulse (catch-a)

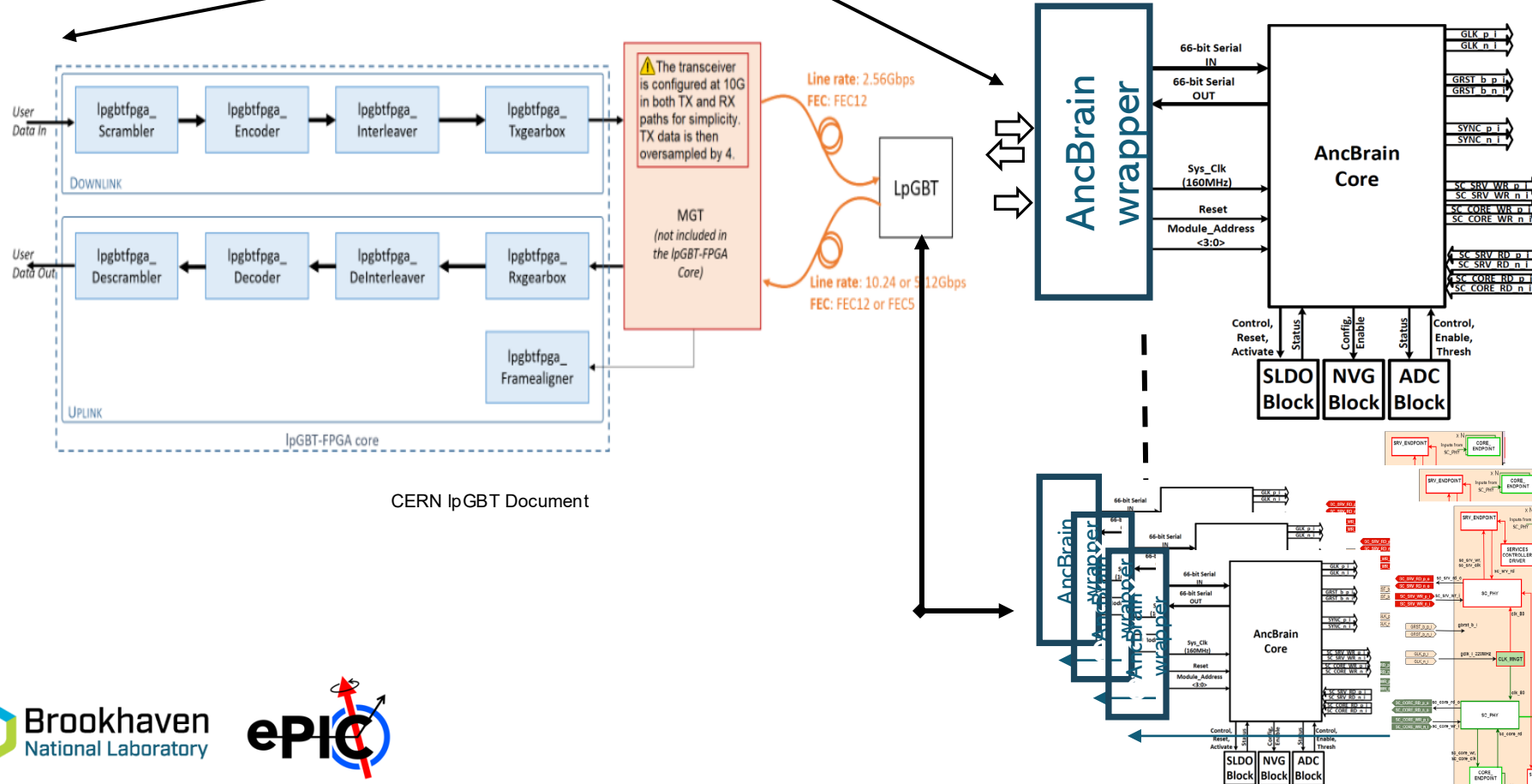
Software Mockup



MOSAIX / EIC-LAS interface

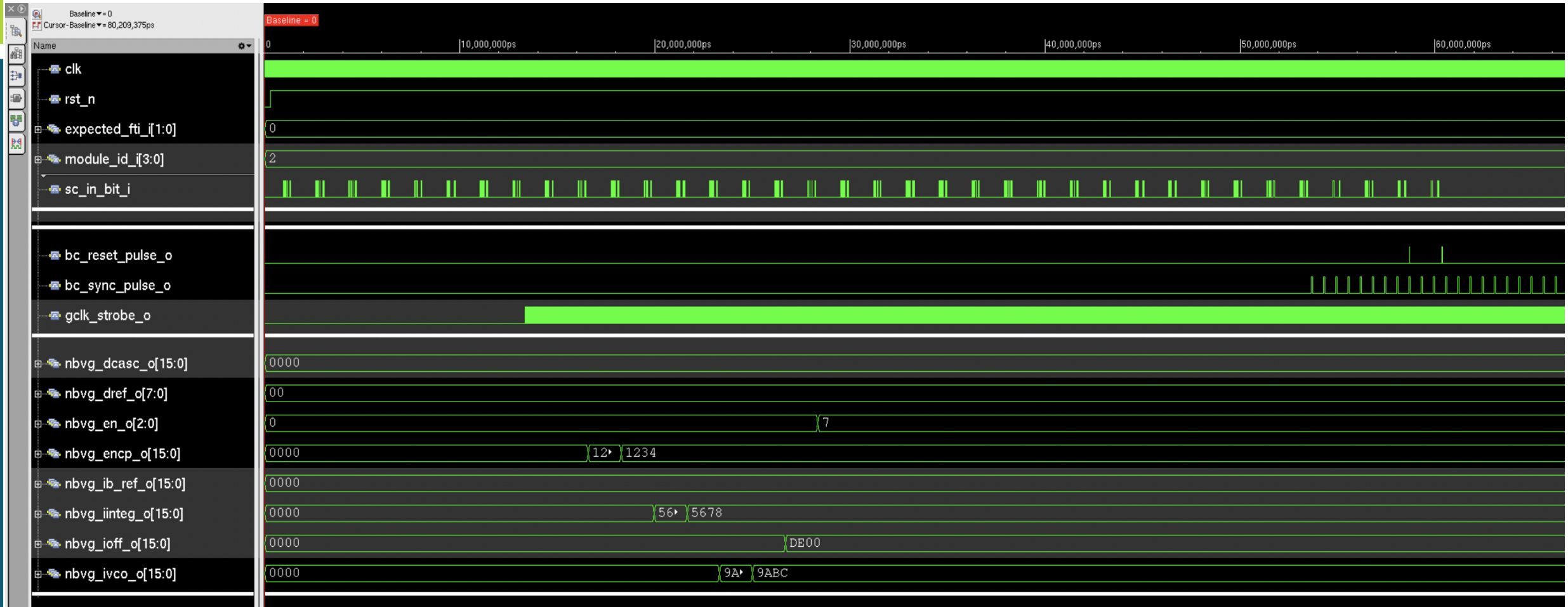


MOSAIX Documentation



CERN IpGBT Document

Functional Verification



Synthesis Report (Preliminary)

2.1 Area Summary

Metric	Value
Total Leaf Cells	8,387
Sequential Instances	3,822
Combinational Instances	4,565
Hierarchical Instances	126
Cell Area	117,964 μm^2
Net Area	37,824 μm^2
Total Area	155,788 μm^2

2.4 Synthesis Timing (WC: 1.08V / 125C)

Path Group	WNS (ns)	TNS (ns)	Violating Paths
reg2reg	+3.3	0.0	0
reg2cgate	No paths	0.0	0
in2reg	+1,610.6	0.0	0
reg2out	+2,856.2	0.0	0
All	+3.3	0.0	0

2.5 Synthesis Power (WC: 1.08V / 125C)

Component	Power
Leakage Power	45.36 μW
Dynamic Power	6.89 mW
Total Power	6.93 mW

PnR Report (Preliminary)

3.6 Post-PnR Area Summary

Metric	Value
Standard Cells	11,374
Physical-Only Cells	11,539 (fillers/decap/tie)
Total Instances	22,913
Total Cell Area	133,089 μm^2
Core Utilization	65.95%
With Fillers	100.0%

3.2 Signoff Setup Timing Detail (Quantus QRC + SI)

Path Group	WNS (ns)	TNS (ns)	Violating	Total Paths
reg2reg	+0.107	0.000	0	6,553
reg2cgate	+0.541	0.000	0	124
in2reg	+0.247	0.000	0	27
reg2out	+2.909	0.000	0	174
in2out	+3.208	0.000	0	1
All	+0.107	0.000	0	6,866

3.3 Signoff Hold Timing

Path Group	WNS (ns)	TNS (ns)	Violating	Notes
reg2reg	-0.020	-0.223	71	BC view (1.32V / -40C)
in2out	-0.893	-0.893	1	debug_clk_o (false path)
All (BC)	-0.020	-0.223	71	Fixable with hold buffers

3.7 Post-PnR Power Summary (WC: 1.08V / 125C, 20% toggle)

Component	Power (mW)	Percentage
Internal Power	9.986	71.0%
Switching Power	4.030	28.6%
Leakage Power	0.052	0.4%
Total Power	14.07	100%

PnR Report (Preliminary)

5. Synthesis vs. PnR Comparison

Metric	Synthesis (Genus)	Signoff (Innovus)	Delta
Cell Count	8,387	11,374	+2,987 (+36%)
Cell Area (um ²)	117,964	133,089	+15,125 (+13%)
Setup WNS (ns)	+3.300	+0.107	-3.193
Total Power (mW)	6.93	14.07	+7.14 (+103%)
Leakage (uW)	45.36	51.84	+6.48 (+14%)

PnR Report (Preliminary)

1. Design Overview

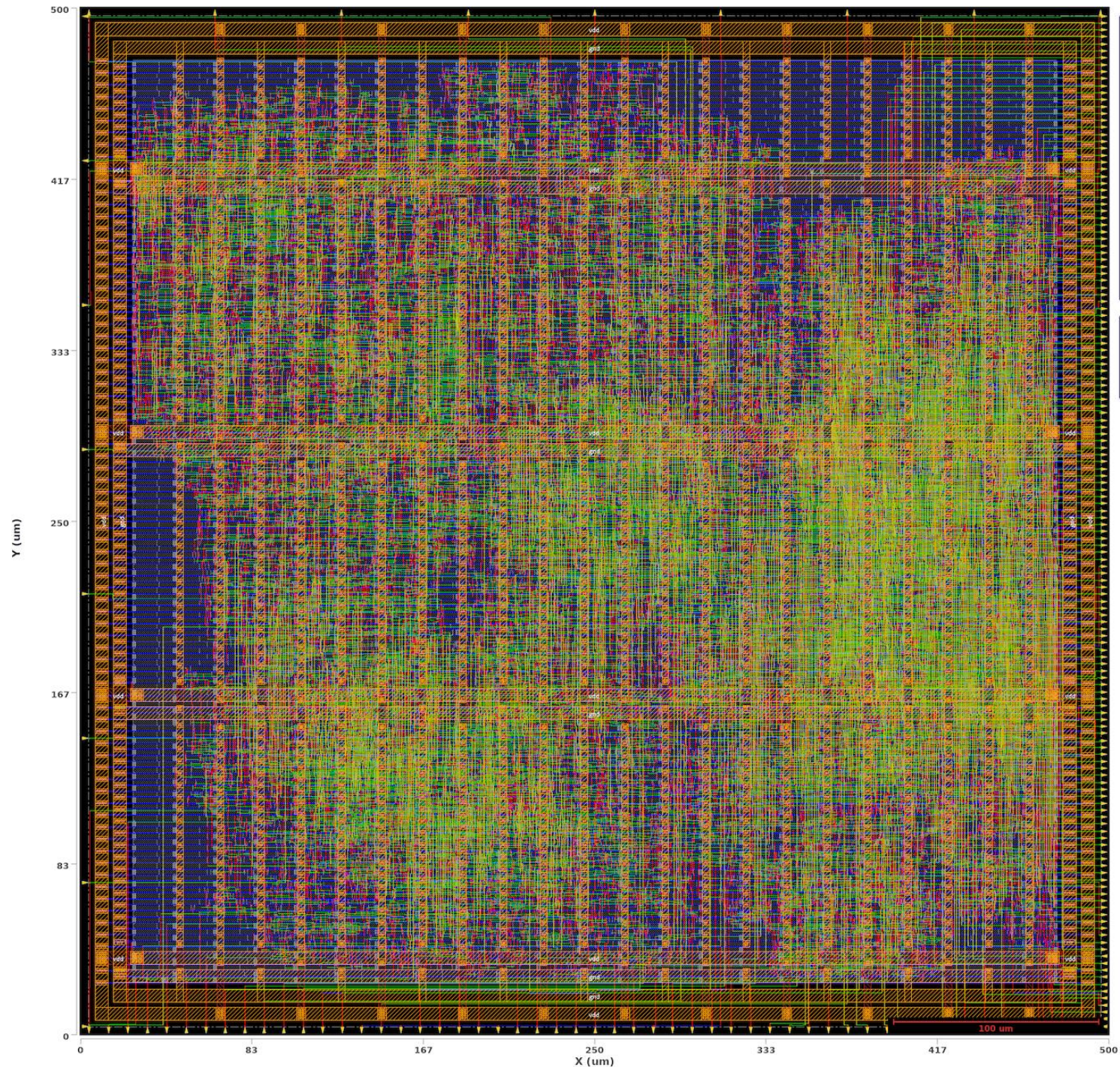
Parameter	Value
Design Name	ancBrain_top
Technology	XFAB XT011 110nm HV SOI CMOS
Standard Cells	D_CELLS_TLLVT (Tapless, Low-Leakage VT)
Metal Stack	MET1-MET5 + METCT (Thick Copper) — xx57
Die Size	499.87 um x 499.87 um (0.25 mm ²)
Clock Domains	clk (160 MHz), clk_80m (80 MHz), gclk_strobe (160 MHz gated)
Supply Voltage	1.08V (core)

Design Metrics

Die Size	499.87 x 499.87 um
Die Area	0.250 mm ²
Std Cells	11,374
Total Instances	22,913
Utilization	65.95%
Setup WNS	+0.107 ns
Setup Violations	0
Hold WNS (BC)	-0.020 ns
Total Power	14.07 mW
Internal	9.99 mW (71%)
Switching	4.03 mW (29%)
Leakage	0.05 mW (<1%)
DRC Violations	0
Connectivity	Clean
Glitch	0 violations
Clock Gating	76% FFs gated
ICG Instances	124

Layer Colors

■	MET1
■	MET2
■	MET3
■	MET4
■	MET5
■	METCT



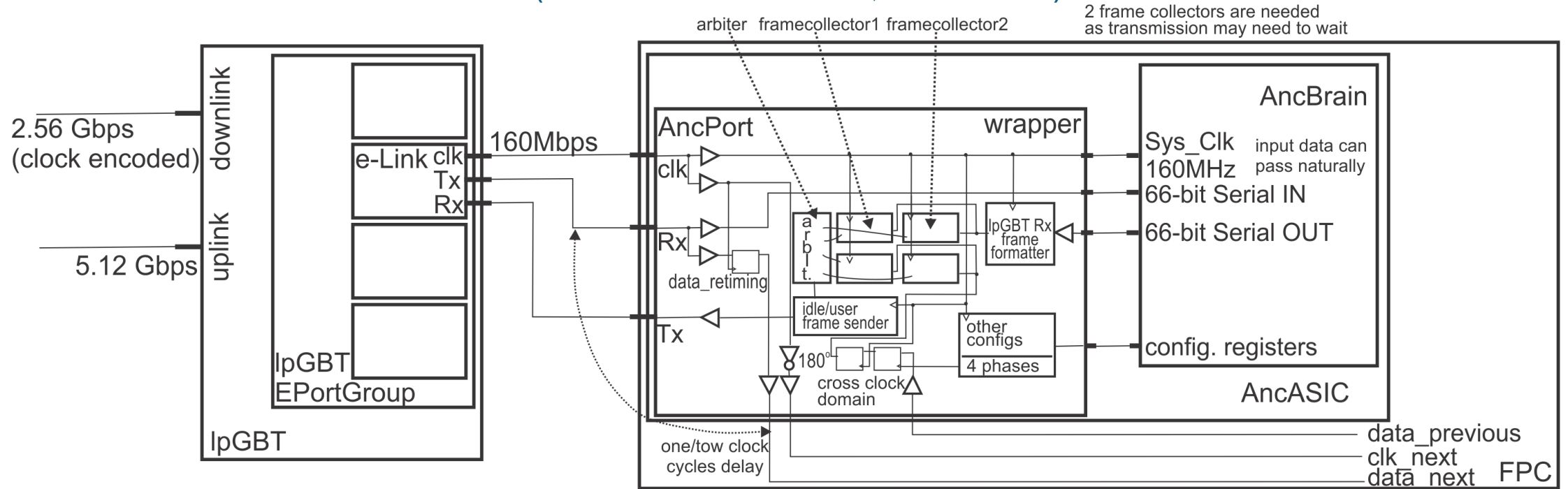
Thank You

AncBrain: Wrapper - 1

Why wrapper is needed?

- Receive 160 MHz clock and provide it to AncBrain
- Interface data stream from e-LinkTX to AncBrain
- Output e-LinkTX data and clock to next AncBrain
- Receive data from previous AncBrain and buffer (it needs use programmed phase and retime data to own clock)
- Receive own data from AncBrain and buffer
- Arbitrate between own data and data from previous AncBrain (any response to any command result in no longer data than 66 bits)
- Construct data frame suitable for e-LinkRx (pad bits to complete full frame, set to right data format)
- Transmit data STREAM to e-LinkRX from AncBrain (when no actual data available, send IDLE data)

specification of wrapper's functionality is underway

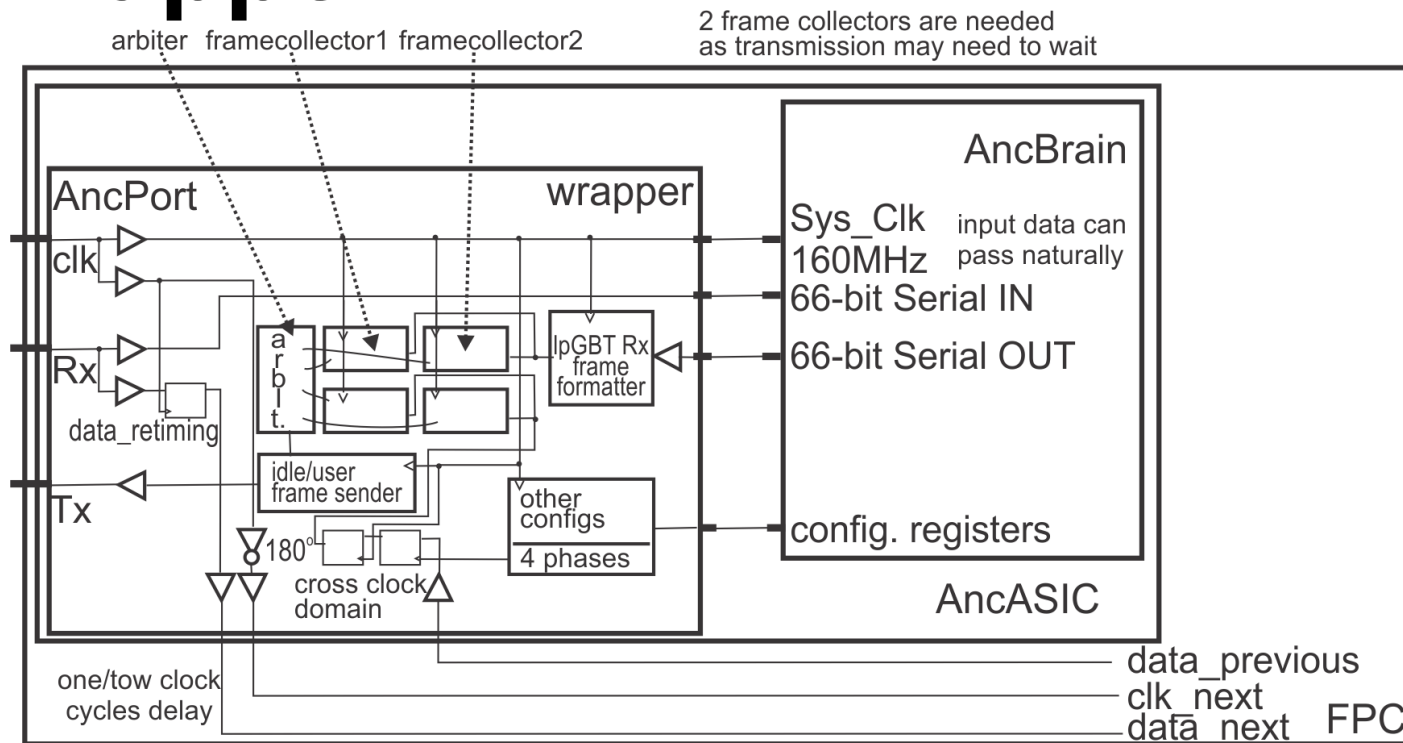


AncBrain: Wrapper - 2

What happens in wrapper

D-channel data from IpGBT Tx can be sent in naturally, though user data needs to be 68 bit

IpGBT Rx frame format needs to be built internally by the wrapper



- downlink data needs to be retimed in each AncASiC in daisy chain, thus 1 or 2 clock delays will be added
- Uplink data from each AncASiC I chain needs to be retimed and brought to local clock domain, thus 1 or 2 clock delays will be added
- Simple retiming using 4 selectable phases is to be executed on incoming data (no IpGBT automatic phase adjustment)
- Selection of phase done in cascade first AncASiC closest to IpGBT for feasibility
- (1) IpGBT Rx frame formatting will be taking 66 bit AncBrain data and putting it into Rx format handshaking with AncBrain
- (2) frame collectors will be used on own frames and incoming frames to manage uplink transmission without collision
- (3) 2 Frame collectors are needed allow resolving collisions (Rx fame is ~2x longer than AncBrain frame)
- (4) Arbiter will be monitoring two directions for frames and commuting between own and incoming data
 - (1), (2), (3) and (4) will result in delays, but should not be critical on uplink – still needs to be estimates
 - [BNL has access to IpGBT model, IpGBT FPGA, IpGBT FPGA simulation, etc. to built complete software mockup](#)