EICROC – Internal/Peer review

1 April 2026

Goal of the reviews is to assess 1) spec and requirements, 2) digital interfaces, 3) status and remaining steps, 4) production outlook, 5) documentation

Christophe's presentation (Part 1)

- Fernando – subtraction of digital noise. What is the mitigation plan for this in the final version?
    - There is more digital noise than seen on ALTIROC – smaller pixels, analog bias lines coupling to the clock? New versions are shielding from the analog line. Pixel is too small to move them further apart, but shielding should solve the issue (early prototypes indicate it has mitigated the problem). → EICROC0A.
    - Specifications for the EICROC not yet frozen. EICROC2 is the one for EIC.
    - Noise ~ 1LSB.
    - Minimum threshold is 3 fC for chip alone, ~7 fC with sensor.
    - Pixel/column addressing issue is due to an incorrectly designed Inverter, but a work-around has been implemented and works for this batch.
    - There is a wafer on hold at TSMC which will have a modified metal layer to fix this problem. Expect chips available in ~2 months and then distributed for testing with sensors – Summer 2026.
    - First measurements of EICROC0A show an improvement of ~1 order of magnitude compared to EICROC0. Still, baseline is not zero and has a slope that needs to be understood. These are very preliminary measurements.
- Alex – does slow control issue affect ALL the chips?
    - Yes, EICROC1, 0A and 0B all affected.
- Tonko – does this issue only affect per-pixel configuration?
    - Yes.
    - Follow-up: so the EICROC1 can still be used for back-end development?
        - Yes, but need to still test a few more things.
- How many EICROC1 chips are available?
    - ~ 69, minus two in-use.
    - Tonko would like to have a few chips as soon as possible.
- On slide 12:
    - what is the efficiency spike on the s-curve on the bottom right plot? We also see this in EICROC0 chips.
        - Not yet understood.

    - Artur: why 3fC used for the pedestal and threshold assessment?
        - Due to charge sharing and due to the fact the charge is always being measured, only TDC is acquired via threshold crossing.
        - Low threshold is also to understand the digital noise and ensure it is under control.
    - Dominique: How did you determine the lower threshold? EICROC0A seems to be much higher in its threshold range (around 300 for EICROC0).
        - Not yet understood.
        - This resulted from the charge injection testing: 2 fC (below threshold) – 4 fC (above threshold). 3 fC is specified then.
- Tonko: the cooling requirements are driven by expectations for the power dissipation. It is currently 2mW/ch for EICROC0 and EICROC1, but the "aim" is ~ 1mW/ch. What do we use? How is this decided?
    - Only discussing the ASIC at the moment.
    - Follow-up: what is the best "target" we can aim for in designing our cooling system.
    - Fernando: 2mW/ch is the spec that has been conveyed to the mechanical engineers for design of cooling systems – that is our spec. If it gets better, great.
    - Christophe: power and digital noise are forefront, so it's one of the main things we want to be optimized.
    - Test boards and their fabrication to be coordinated with BNL.

Alexandre's Talk on Digital-on-top (EICROC2) proposal/plans

- Tonko: Are these rates per hit?
    - 20 Hz/pixel means 20kHz per chip.
    - Follow-up: isn't the figure of merit the total rate per "chip"? Is the bottleneck at a column of pixels or the output of the ASIC?
        - The ASIC.
    - Detector groups need to make sure their individual rates are understood and that this is communicated to the EICROC developers if they differ from current specs.
- Digital architecture documentation will be uploaded to the Indico.
- Readout for 1,024 pixels in one go must have a specification. To be developed by groups as input to final spec.

Christophe's talk (part 2)

- Full detector tests should only be done with "Fixed" chips (~ 2 months for process to fix remaining wafer).
- Tonko: 69 current EICROC1's (bad ones); how many with new fix?
    - There will be an additional 69 "good" chips with the fix in place.
    - Also need to finalize availability of test boards.
- QA and QC needs to be done EXTERNALLY – IJCLab will not do this.
    - Need to decide if a vendor or at ORNL/BNL/etc.
    - Need to define what is needed for the procedure in any place it is done.
    - OMEGA/IJCLab will provide documentation based on previous work with ALTIROC.
    - This is a point requiring more follow-up and planning among all detector groups.
- Lots of discussion on production of final version, in-kind, etc. – things need to be solidified.
    - Schedule shown (2030) was for Roman Pots
        - This will not work for EIC schedules (fTOF, Lumi, RP, etc.)
        - We have had FY28 production for all detectors in P6 for years.
            - This needs to be understood now before freezing P6 for baselining with CD-2.
    - Christophe: number of Wafers at 25
        - Fernando: we have 46 wafers with overage. A minimum of 33 is needed, per number of channels. Then, we will need extras so 46 would be necessary.
        - Christophe: to be adjusted depending on Engineering run or production costs.
    - Dominique: Who will be responsible for production? Possible issue with funds from French collaboration.
        - Fernando: production is In-Kind.

Summary

- Preliminary measurements of the EICROC1 are very encouraging; ~60 chips with fixed inverter issue (spare wafer) to be available for tests with sensors/detectors ~July 2026.
- Specifications for readout and rates from all EICROC detectors to be provided to developers soon.
- Availability of Test Boards to be coordinated with BNL and Tonko very soon.

- QA/QC will need to be performed by collaborating institutions; OMEGA/IJCLab will provide documentation from ALTIROC, for guidance.
- Schedules at OMEGA/IJCLab need to be revised to meet EIC needs. P6 has had EICROC production for all EIC detectors in FY28 for some time now.
- In-Kind contribution is set in EIC project.