EICROC Internal Review
1 apr 2026

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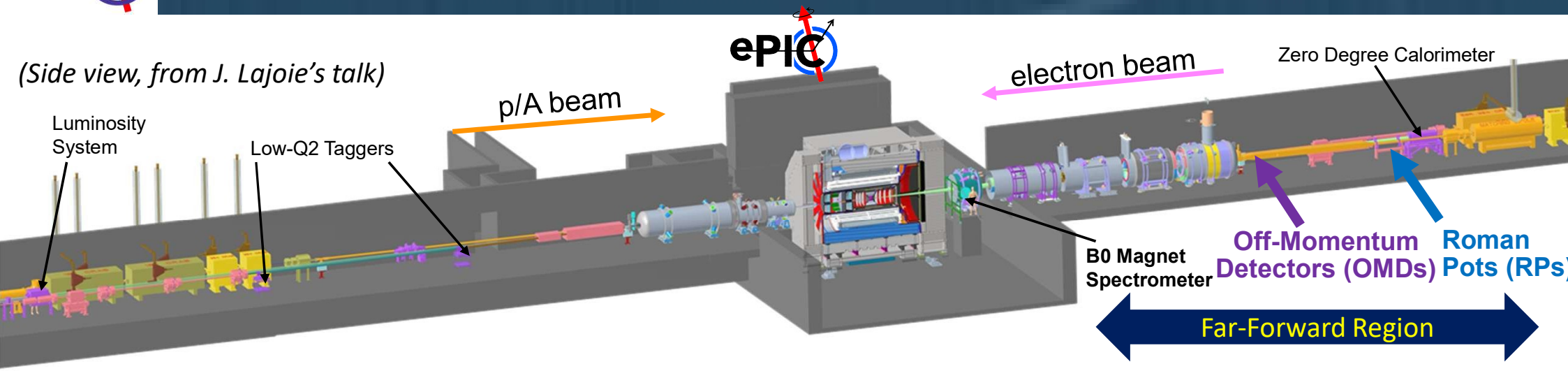
Organization for Micro-Electronics desiGn and Applications

ePIC Detectors & Far-Forward Region



Far-Forward detectors are essential to measure exclusive processes, as Deep Virtual Compton Scattering (DVCS) → Generalized Parton Distributions (GPDs)

❖Roman pots (RP)

- Detect particles scattered at very small angle (< 5 mrad)
- Required to measure exlusive processes on proton targets
  - **DVCS, DVMP…**
  - **All the channels relevant to GPDs of quarks and gluons**

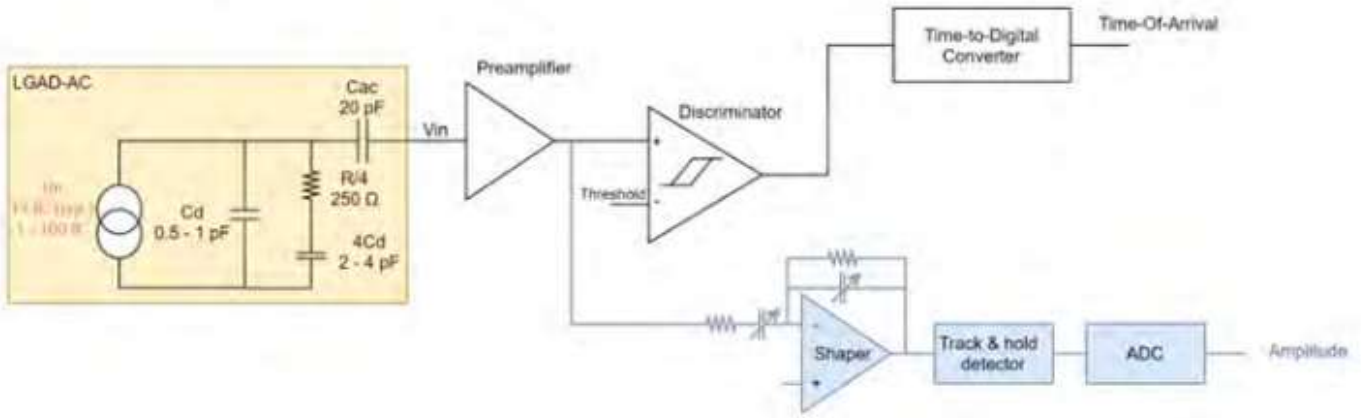
❖Off-Momentum Detectors (OMD)

- Detect small angle particles with a different rigidity than the beam
  - **Access angles down to 0 for rigidity < 0.65**
- Necessary for all tagged measurements
  - **Study of nuclear effects**
  - **Effective neutron target**

EICROC specifications and requirements

- Readout of 32x32 AC-LGAD pixels matrix 500µm*500µm for Roman pots

- Analog requirements :
  - Risetime < 1 ns for Cd < 2 pF
  - Minimum threshold : 5 fC for 10 fC signal
  - Jitter < 30 ps for Q > 10 fC and Cd < 2 pF
  - Charge measurement : 0 – 50 fC with noise < 1 fC
  - Power dissipation < 2 mW/ch
  - Radiation hardness > 10 Mrad, configuration SEE robust

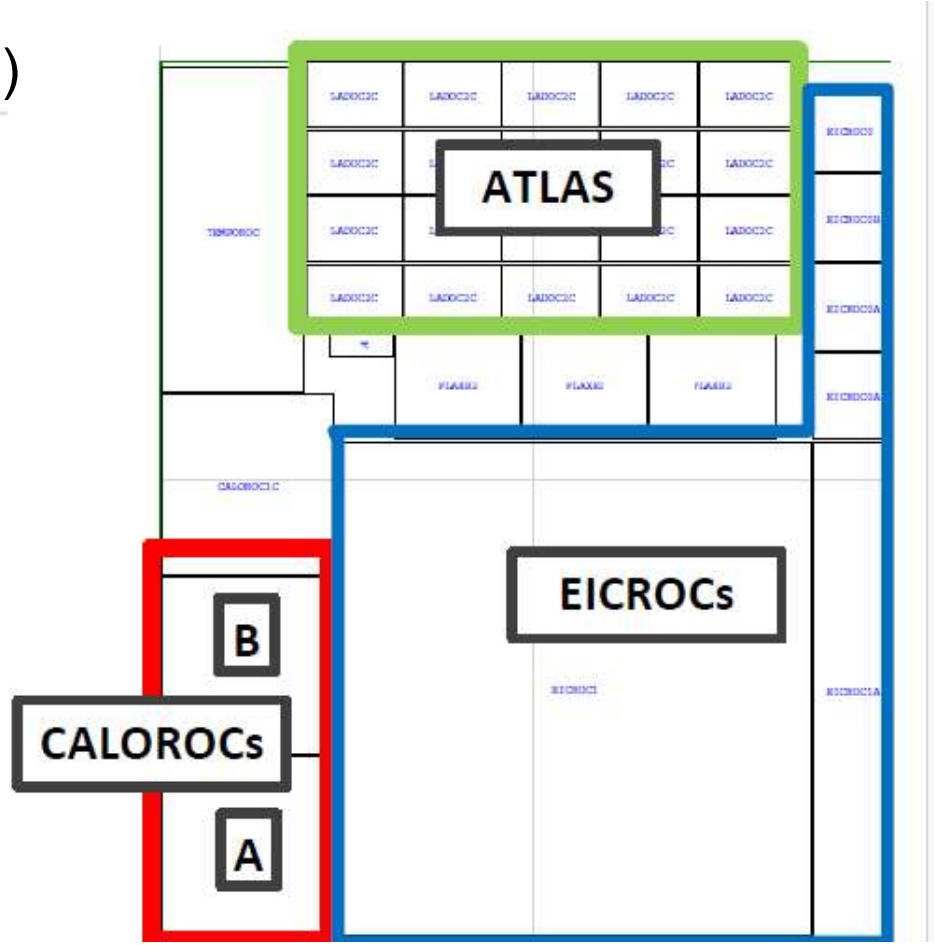


EICROC specifications and requirements (2)

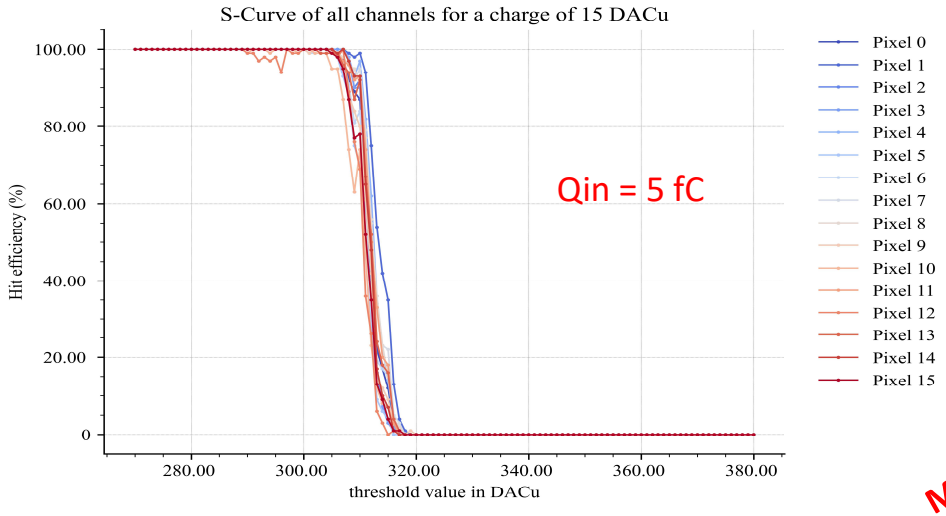
- Digital requirements : will be detailed in A. Soulier's talk
  - Input clock 320 MHz
  - Synchronous controls encoded in fast commands
  - Slow control by I2C
  - Maximum event rate : 100 Hz/pixel (tbc)
  - Output data frequency : 320 MHz differential CLPS
  - Max power 500 µW/pixel

EICROC prototypes

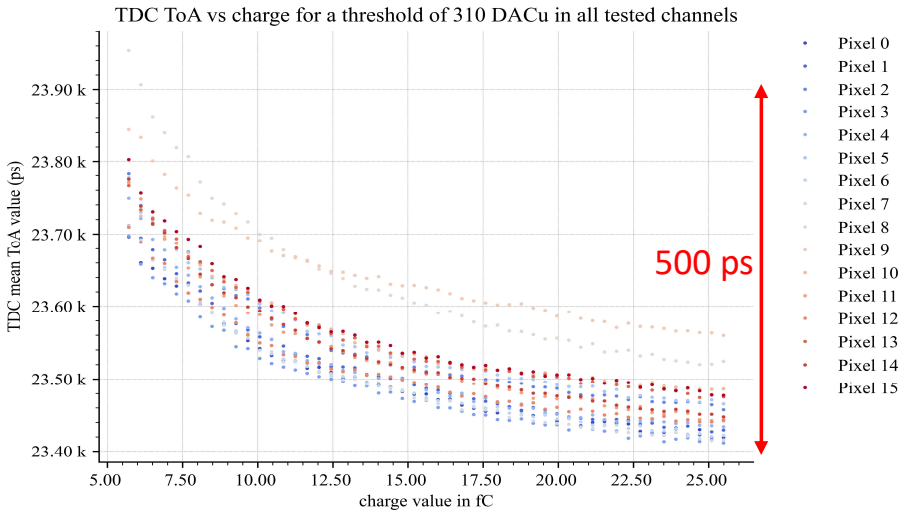
- EICROC0 : 4x4 pixels with simple readout (2022)
- EICROC OA/0B 1/1B fabricated in 2025 engineering run TSMC 130n
  - EICROC0A/B : 4x4 with improved blocks
  - EICROC1/1A : 32x32 and 4x32
- EICROC2 will be fabricated Q1 2027

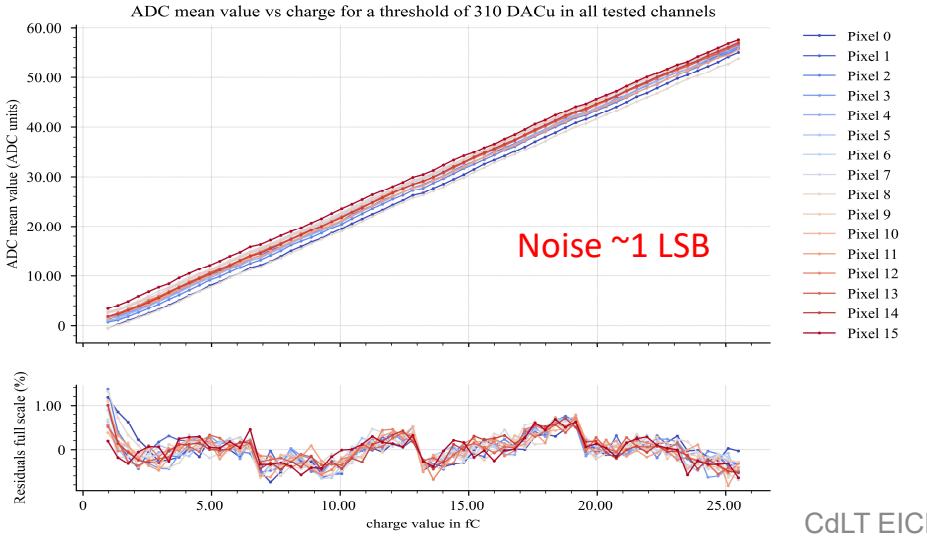


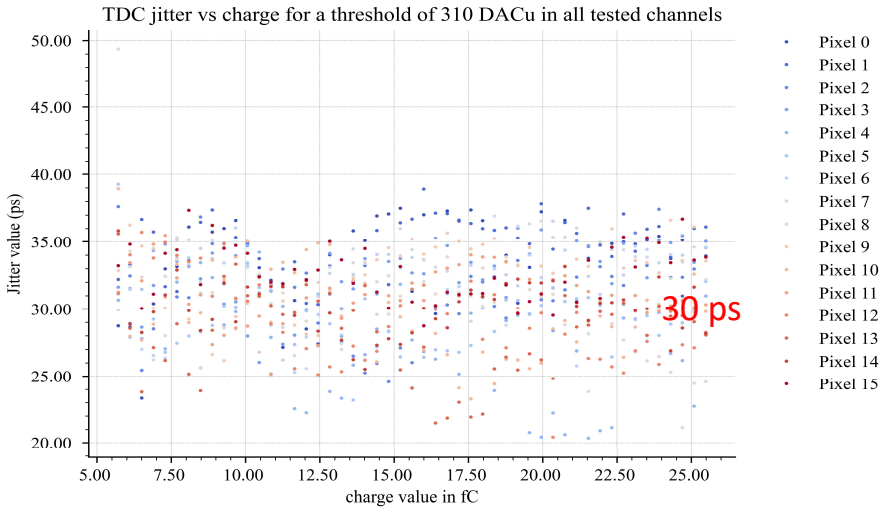
EICROC0 (4x4): ASIC alone characterisation



More in backup



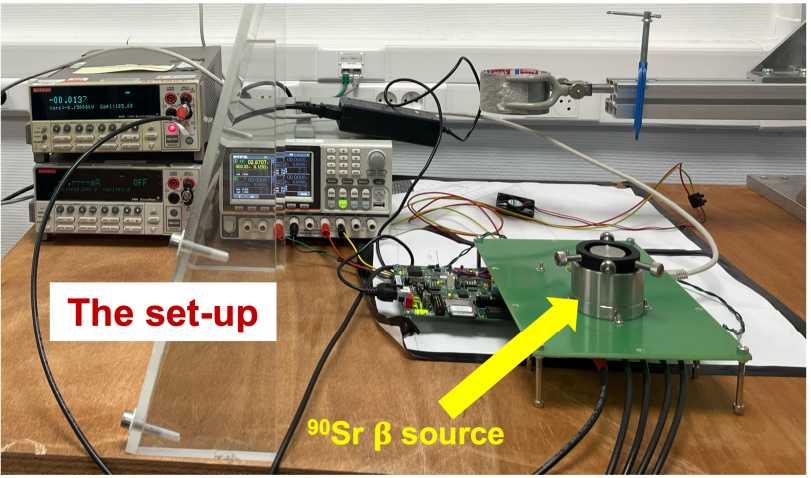




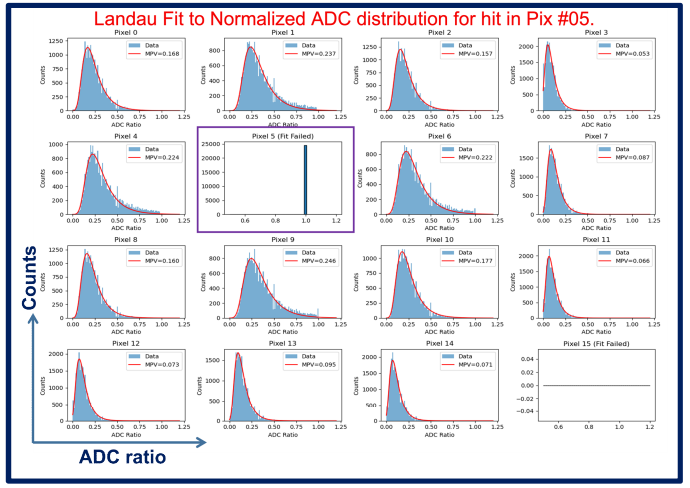
Pixelated AC-LGAD read-out characterization

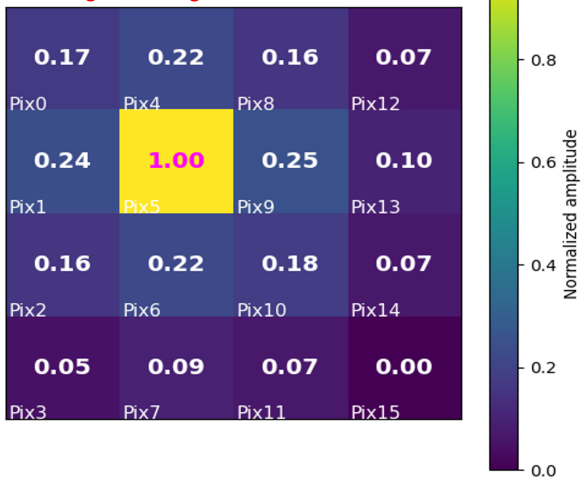
Measurements with ^{90}Sr β source at IJCLab PSI platform (July '25)

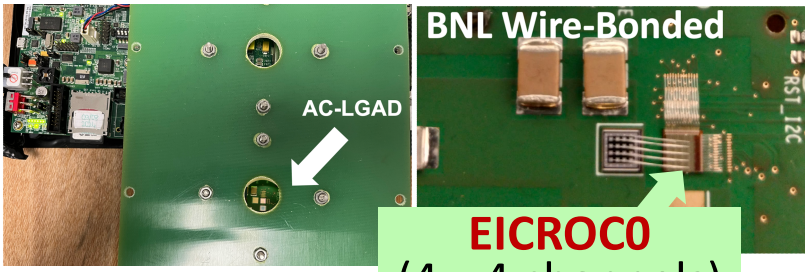
1) digital data stored when the PreAmp signal amplitude of at least 1 channel among the 16 is passing the discriminator threshold
2) long run (~ 10 hours) splitting data into multiple files with r fixed number of events/file



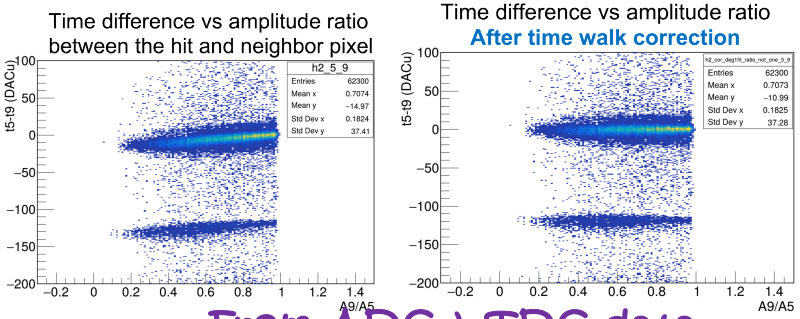
From ADC data







EICROC0
(4 x 4 channels)
CMOS 130 nm



From ADC & TDC data

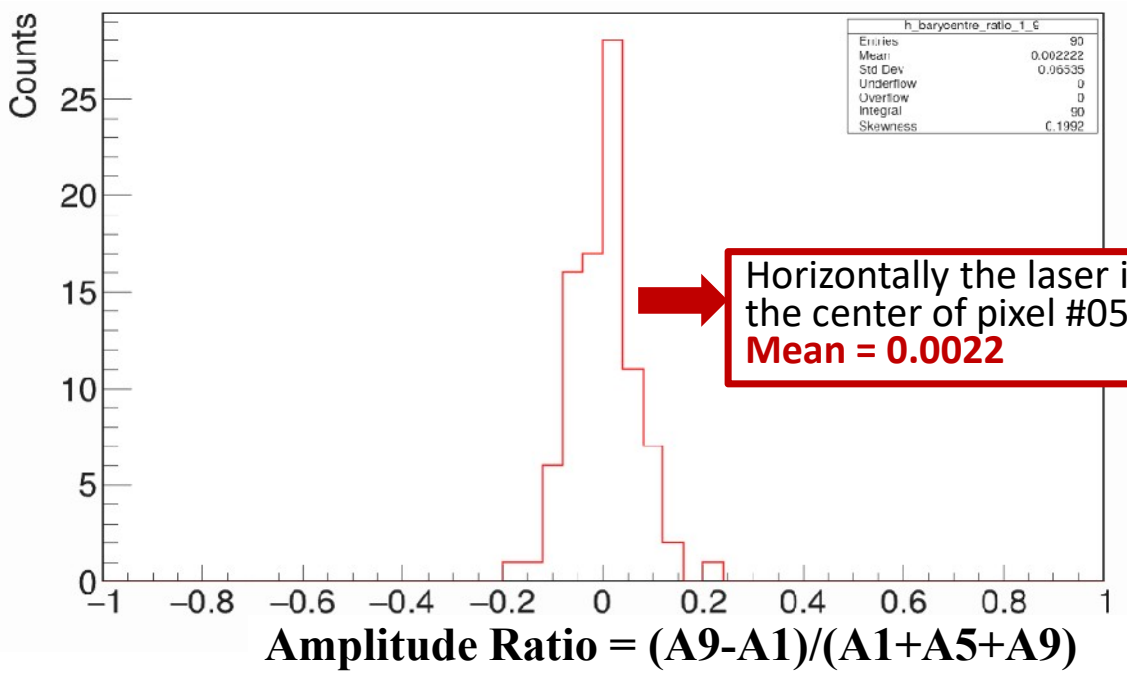
- ADC pedestal subtraction computed from "far" pixel
- More charge sharing (~23%) for adjacent neighbors
- Time walk correction applied successfully to TDC data

Pixelated AC-LGAD read-out characterization
Preliminary results with Infrared Laser

Barycenter calculation from ADC data (Sept. 18, 2025)

Considering pixels **#01, #05 & #09**

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15



Horizontally the laser is shooting the center of pixel #05
Mean = 0.0022

Very encouraging!

Position Accuracy ~ +/- 17 μm
(**RMS 0.065** x 500 μm = 33 μm)

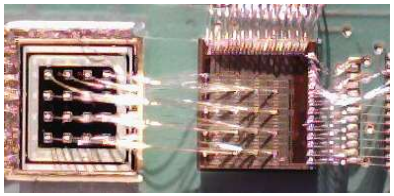
This method to be extended to the whole matrix

Pixelated AC-LGAD read-out characterization With Infrared Laser (Dec. 19th, 2025)

TDC differences between 2 hit neighboring pixels

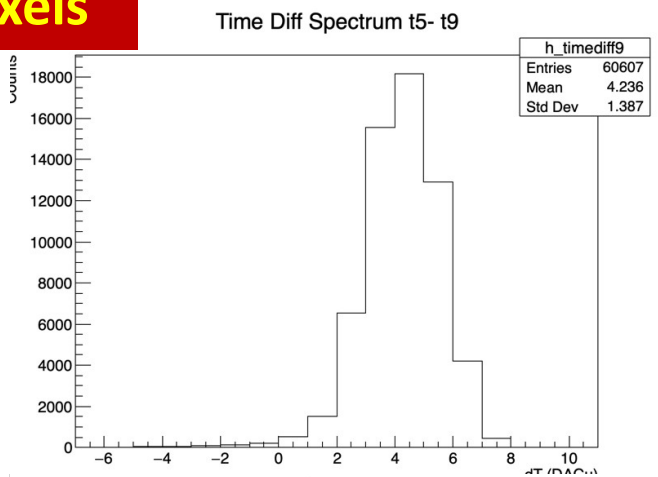
[Assumption: 1 TDC DACu = 25 ps]

Very recent



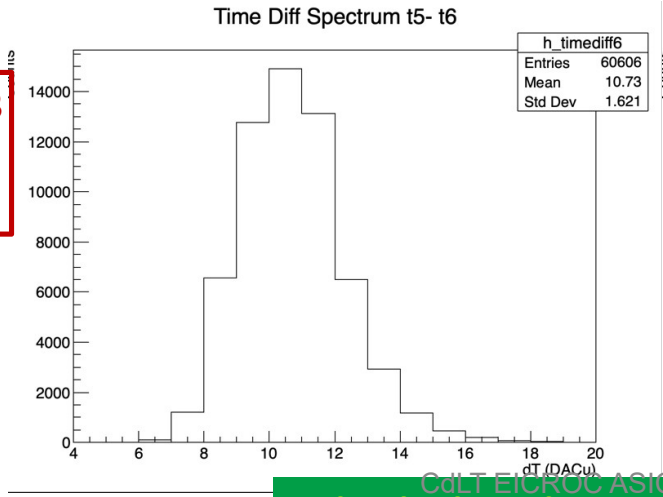
Laser 1 KHz, 77.6% attenuation, ~60 000 evts

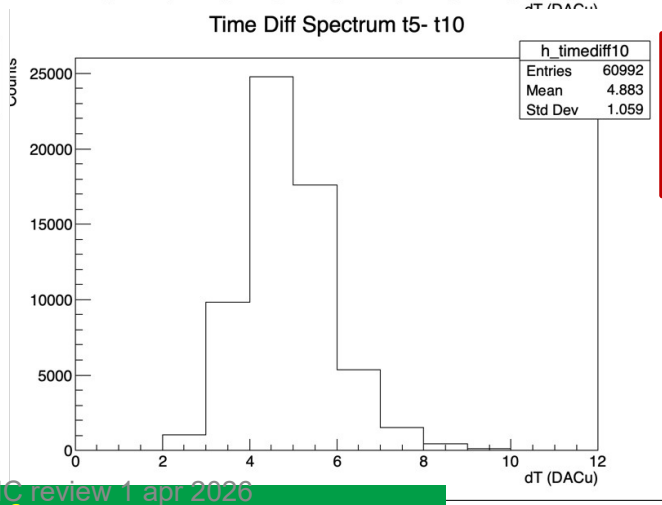
BNL sensor biased at HV = -190V



σ [pix05 – pix09]$_{DACu}$ = 1.387
➜ TDC jitter for individual pixel [= σ / √2]: **24.5 ps**

σ [pix05 – pix06]$_{DACu}$ = 1.623
➜ TDC jitter for individual pixel [= σ / √2]: **28.7 ps**





σ [pix05 – pix10]$_{DACu}$ = 1.059
➜ TDC jitter for individual pixel [= σ / √2]: **18.7 ps**

Individual Pixel jitter from 19 ps up to 29 ps

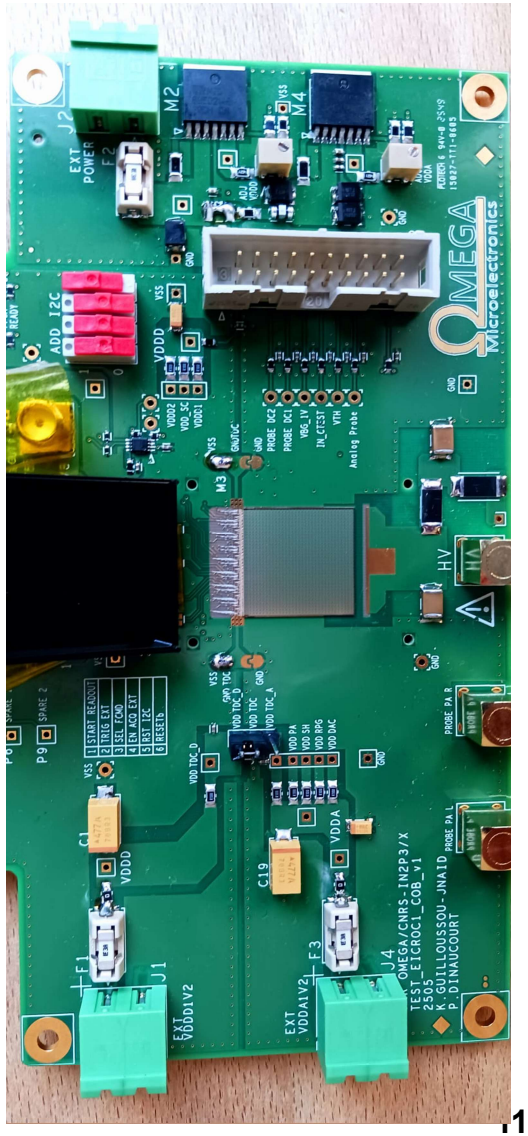
New prototypes EICROC0A/B

- EICROC0A : same as EICROC0 with more testability
  - Each pixel can be by-passed by SC (clock is then turned off)
  - Buffers in SC to allow extension to 4x32
  - Larger dynamic range in pulse injection

- EICROC0B [Adrien]
  - Same preamp/discri/TDC/integrator
  - ADC and driver replaced by peak sensing and Wilkinson ADC
  - Currently ADC path ~1 mW/ch becomes 200 uW/ch

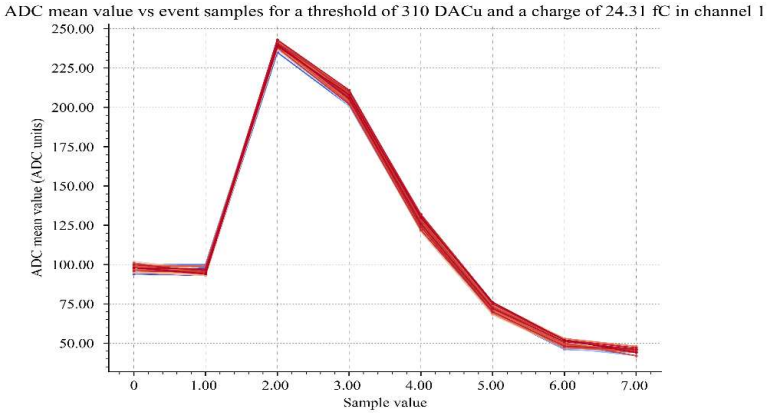
Status of EICROC0A/B/1

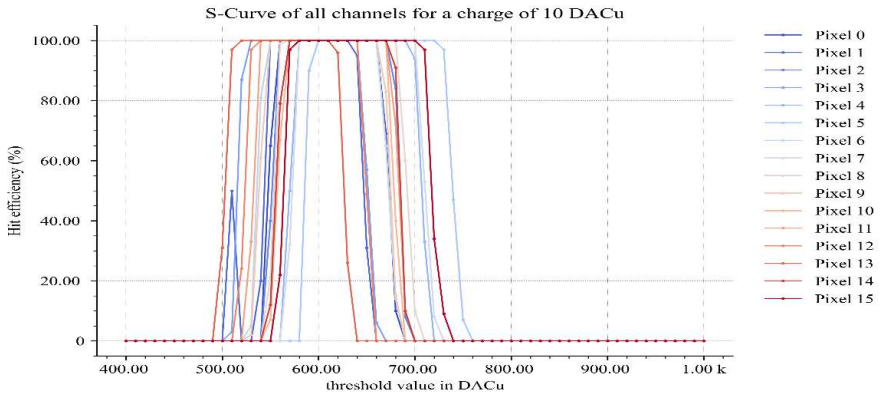
- Chips arrived last month, assembled and wire-bonded beg. of march
- 2 testboards of each 0A/0B/1 : all powered OK
- Issues with the slow control, understood only last week
  - Issue with decoder => all columns addressed simultaneously
  - Work-around tested on EICROCOA now to look at data and performance
  - Simple metal fix possible on the wafer on hold
  - Wait to look at the rest of measurements before releasing fix

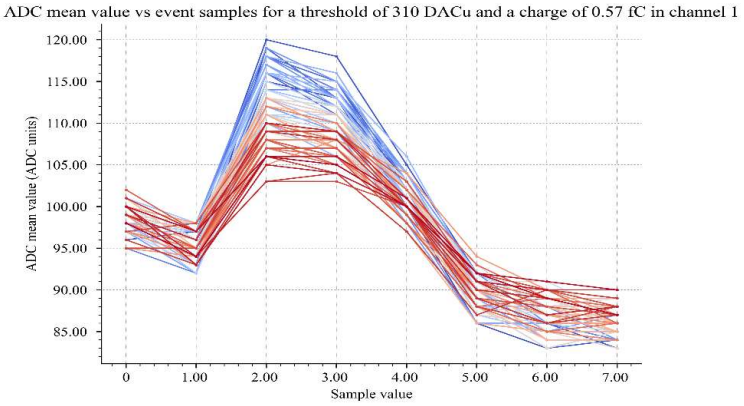


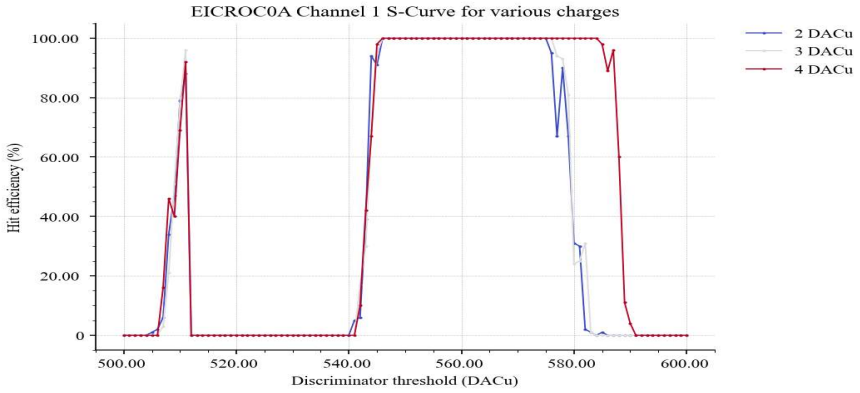
First measurements of EICROC0A

- Only partial configuration is possible : look at ADC data and s-curves
  - Improved ADC baseline, similar minimum threshold (3 fC)







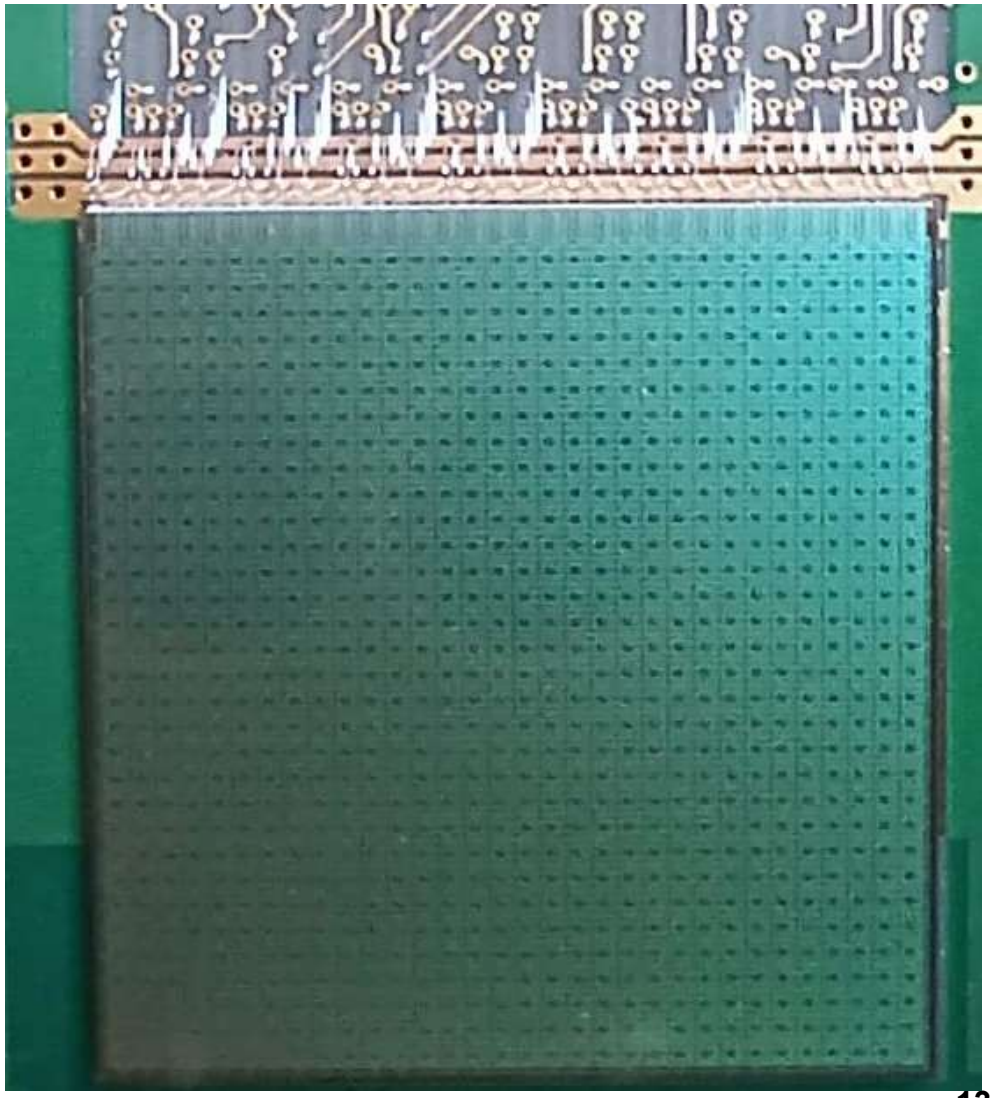


EICROC1

- 32x32 chip : final dimensions

- Goal :
  - test full-scale chip analog performance (IR drops)
  - Allow final sensor characterization
  - Test interface with DAQ : fast commands and 320 Mb/s data output
  - Progress on module/front-end boards

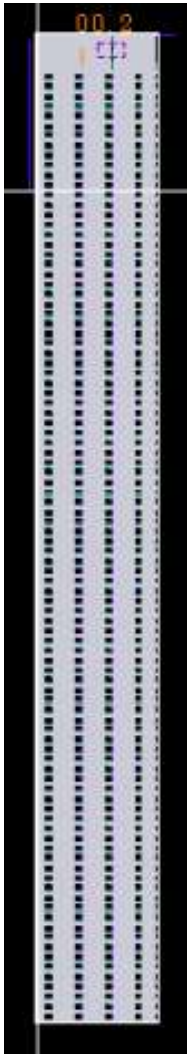
- Caveats :
  - Not (yet) zero-suppressed data
  - Still 2mW/ch
  - Still analog-on-top



EICROC1 description

- Designed as 8 blocks of 4x32
  - Read out sequentially, like EICROC0
  - Pixel similar to EICROC0A
  - 8 CLPS outputs at 40 MHz
  - Clock tree for isochronous calib_pulse distribution

- Common balcony (End of column)
  - Biases and slow control
  - New : fast command decoder (clock, calib_pulse, enable_acquisition, start_readout)
  - Backup clock and cmd_pulse inputs available
  - New : 320 MHz serializer for 1 CLPS output



EICROC1 I/Os

- Digital inputs
  - CLK_320 and FCMD (clock and fast commands) : CLPS
  - RSTb and RSTb_I2C : 1.2 V CMOS active low
  - SDA, SCL and 4b address : I2C slow control 1.2V CMOS
  - SEL_FCMD : 1.2V CMOS to select the backup inputs (below) (default fcmd)
  - Backup inputs : like EICROC0 (clk_160, cmd_pulse, en_acq, start_ro)
  - All unused inputs can be left floating (internal pull-ups/pull-downs)

- Digital outputs
  - 8 x 40 MHz data output (CLPS) by block of 4x32
  - one 320 MHz serialized data output (CLPS)
  - one trigger output (OR of all internal triggers) (CLPS)
  - One digital probe (1.2V CMOS) for debugging

- Analog outputs : for debugging (2 preamp outputs, analog probe, bias probe)

next EICROC2 (2027)

- What is missing in EICROC1 ?
  - Larger rate compatibility ?
  - Derandomizer for successive events (how many ?)
  - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
  - Auto-trigger and zero_suppressed data
  - Power reduction if possible down to ~1 mW/ch

- Clermont Ferrand lab has joined to take responsibility for the DoT
  - Already participated in ATLAS ALTIROC
  - The design and verification should take ~9 months from now

- Technology choice
  - Seems to converge to 130n provided rate remains low enough

Next steps with current prototypes

- Complete measurements possible with current EICROC0A/B/1
  - Currently can configure only one pixel for trigger but read all ADC and TDC data on 0A
  - Test with generator, laser and source foreseen
  - Extend the measurements to EICROC0B and EICROC1
  - Evaluate what tests can be done with sensors and/or DAQ

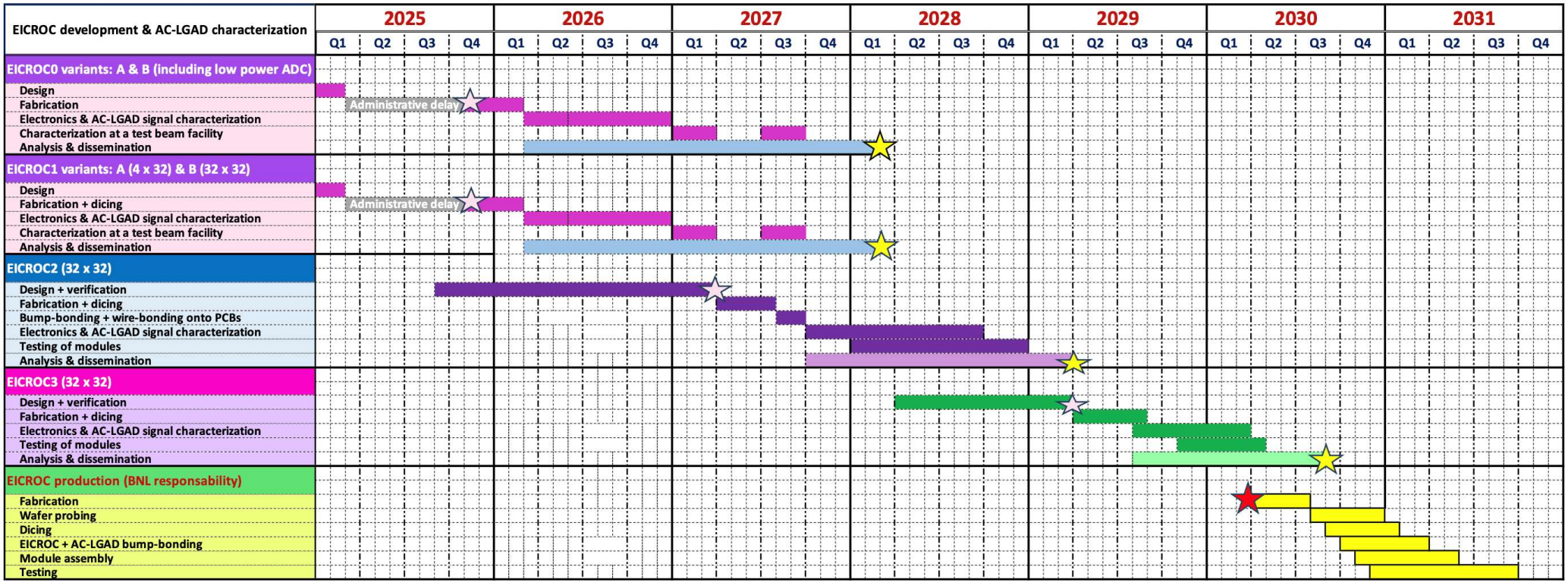
- Prepare metal fix for remaining wafer
  - Very simple so far with V23 and M3
  - Wait for more measurements if there are more modifications needed
  - Metal fix takes ~2 months (mask fabrication, wafer completion, shipping and dicing)
  - Chips with metal fix should be used to do complete tests/validation with detectors

- In parallel prepare EICROC2
  - Will launch only when EICROC1 analog performance has been validated

Production outlook

- EICROC2 (Q1 2027) should be the final prototype
  - DoT and SRO with all functionalities
  - Will be used for detector and SRO DAQ validation
  - Most likely to go to TSMC fab 14 => radiation validation will need to be redone
- Schedule allows a possible EICROC3 iteration for bug fixes
- Production is a single engineering run at TSMC (< 25 wafers)
  - Note that TSMC has stopped MPWs in 130n, but engineering runs continue
  - Production likely to be shared with CALOROCs
- QA/QC
  - Chips will need to be tested at wafer level with probe station
  - Will need to be outsourced

EICROC & AC-LGAD read-out characterization
Timeline



Start of Early Science Program: ~ 2035 ; Roman Pots & OMD installation: not before 2036 → **« On schedule »**

The Team

Roman Pots (& OMD) CNRS/IN2P3 Project
D. Marchand (RS) + O. Brand-Foissac (RT)

WP1 – EICROC Micro-electronics
C. de La Taille

Front-End	C. De La Taille A. Verplancke
Low power ADC	A. Verplancke
TDC	F. Bouyjou E. Delagnes
Overall Design & Documentation	C. De La Taille F. Dulucq K. Guillossou-Jnaid N. Seguin-Moreau L. Serin
PCB	P. Dinaucourt J. Favre
Firmware / Software	B.-Y. Ky
Data acquisition	F. Dulucq
EICROC2 (32x32) Digital architecture, implementation and verification	N. Arveuf G. Blanchard F. Dulucq H. Chanal N. Kachkachi L. Royer A. Soulier (Resp.)

WP2 – EICROC Characterization
D. Marchand / A.-S. Torrento

ASIC Functionnal Response	O. Brand-Foissac F. Bouyjou D. Marchand K. Guillossou-Jnaid N. Seguin-Moreau L. Serin Post-Doc (2026-2028) A. Verplancke
ASIC + AC-LGAD Functionnal Response	O. Brand-Foissac K. Guillossou-Jnaid D. Marchand N. Seguin-Moreau L. Serin Post-Doc (2026-2028) A. Verplancke
Source Beta IR Laser Test beam	O. Brand-Foissac V. Chaumat T. Cornet D. Hohov D. Marchand L. Serin Post-Doc (2026-2028) A-S. Torrento
Dissemination	All people involved in WP1 & WP3

WP3 – Roman Pots Mechanics
R. Dupré / C. Le Galliard

Cooling design: heat flow simulation	C. Le Galliard R. Dupré
Mechanics design	C. Le Galliard
Prototyping	C. Le Galliard Mechanics workshop
Beam tests	C. Le Galliard Instrumentation support Data acquisition support R. Dupré D. Marchand
Detector simulation	R. Dupré Post-Doc (2026-2028) PhD student (2026-2029)
Data analysis	R. Dupré Post-Doc (2026-2028) PhD student (2026-2029)
Dissemination	All people involved in WP3

WP4 – Management
R.S + R. T. (IJCLab)

- Project follow-up
- Reporting / Proposals
- Recruitements
- Periodic meetings
- Project documentation: ATRIUM (C. Le Gallaird) https://atrium.in2p3.fr/6928d9e1-303b-430f-aeb0-1d75aa60970d
- Dissemination

Close collaboration with Brookhaven National Laboratory

Scientific leaders: C. De La Taille (OMEGA) , F. Bouyjou (CEA/Irfu/DEDIP), A. Soulier (LPCA), D. Marchand (IJCLab)

Conclusion & Outlook

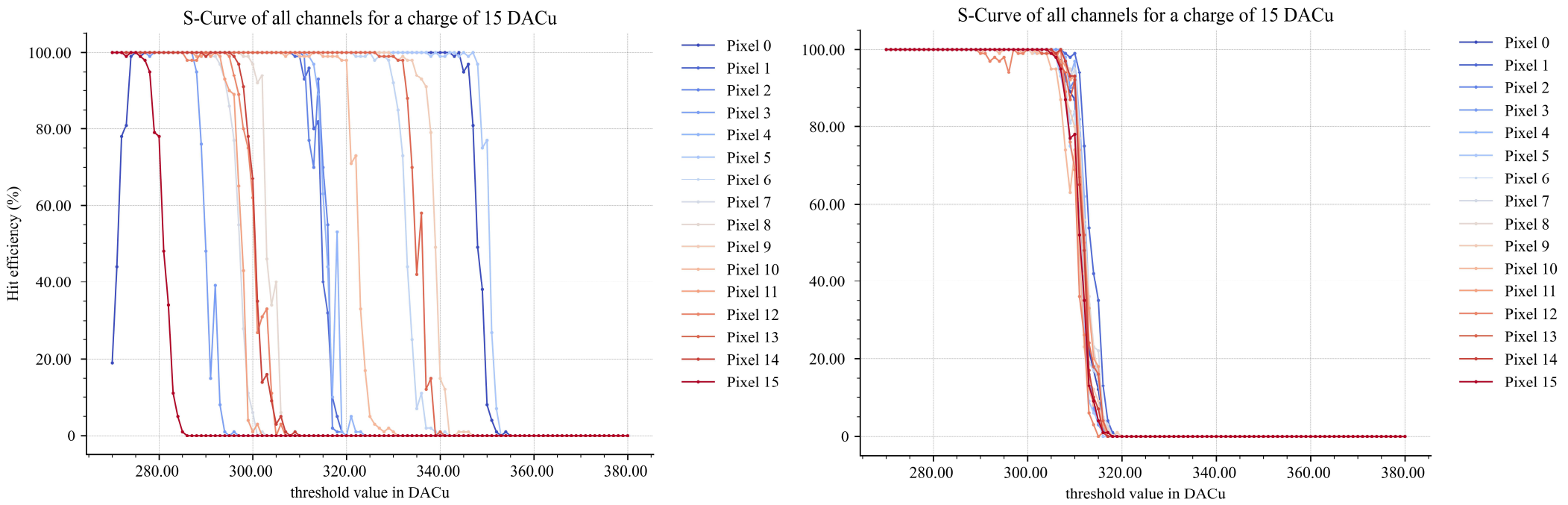
- EICROC0A/B/1 now under test
  - Slow control bug limits extensive characterization but tests still possible and started
  - Metal fix will be done to correct it on wafer kept on hold at TSMC (takes 2 months)
  - Some tests should be possible with sensors and DAQ before metal fix
  - Extensive sensor, detector and DAQ tests should be done with metal fix
- EICROC2 design well under way at Clermont
  - DoT and Streaming readout implemented
  - So far fits in TSMC130n
  - Should be submitted Q1 2027
- EICROC3 should be the production version in 2030
  - Schedule still allows an iteration if necessary
  - Production is only a small engineering run for TSMC

backup

EICROC0 update on measurements : S-Curves [A. Verplancke]

- 6-bit DAC for channel-wise threshold alignement

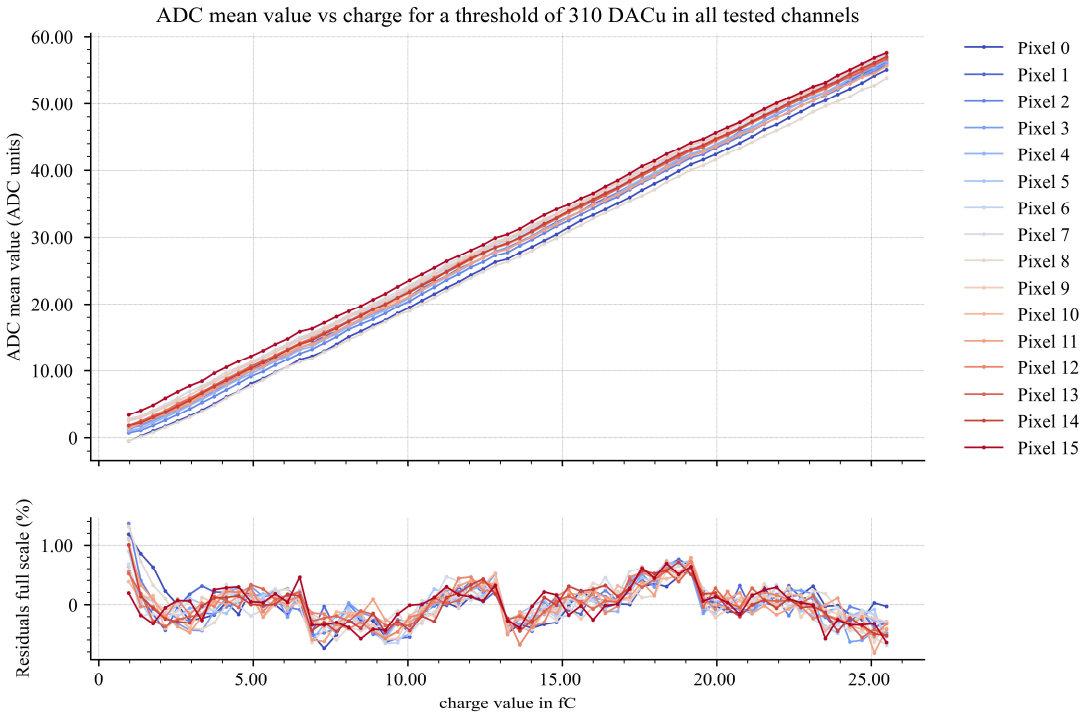
Correction of channels for a charge of 5 fC



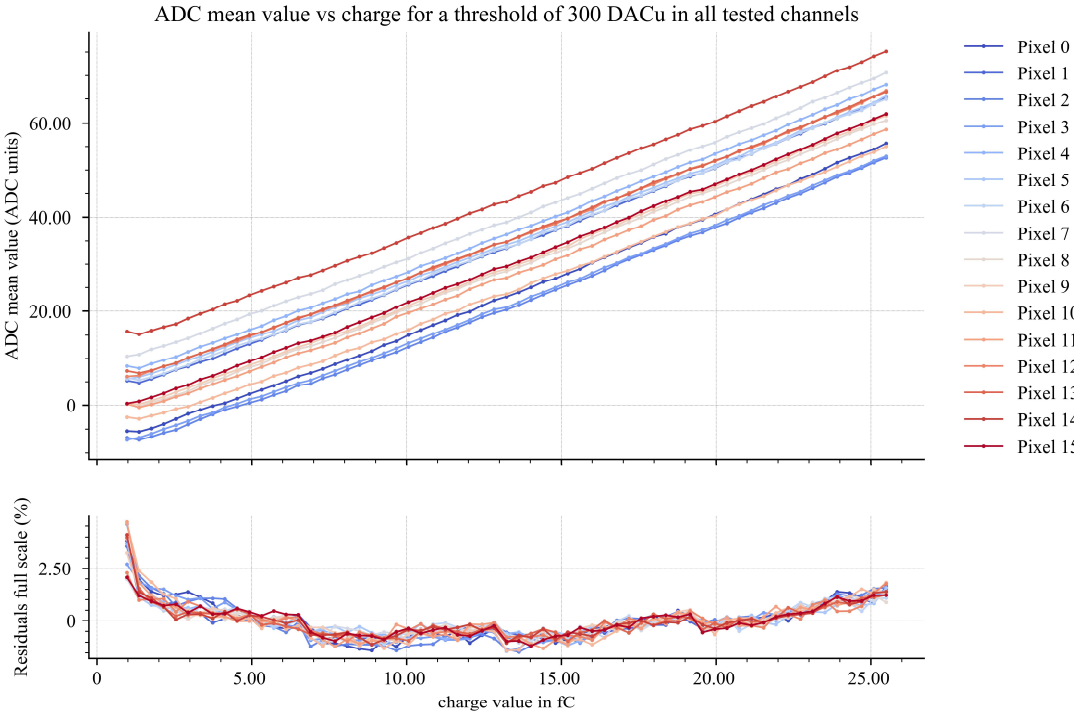
EICROC0 measurements : ADC linearity

- 8 bit 40 MHz SAR ADC [Krakow]
  - Noise ~1 UADC but large common mode noise
  - Signal 50 UADC ~500 um => 1 UADC ~10 um

ADC mean & residuals – no sensor



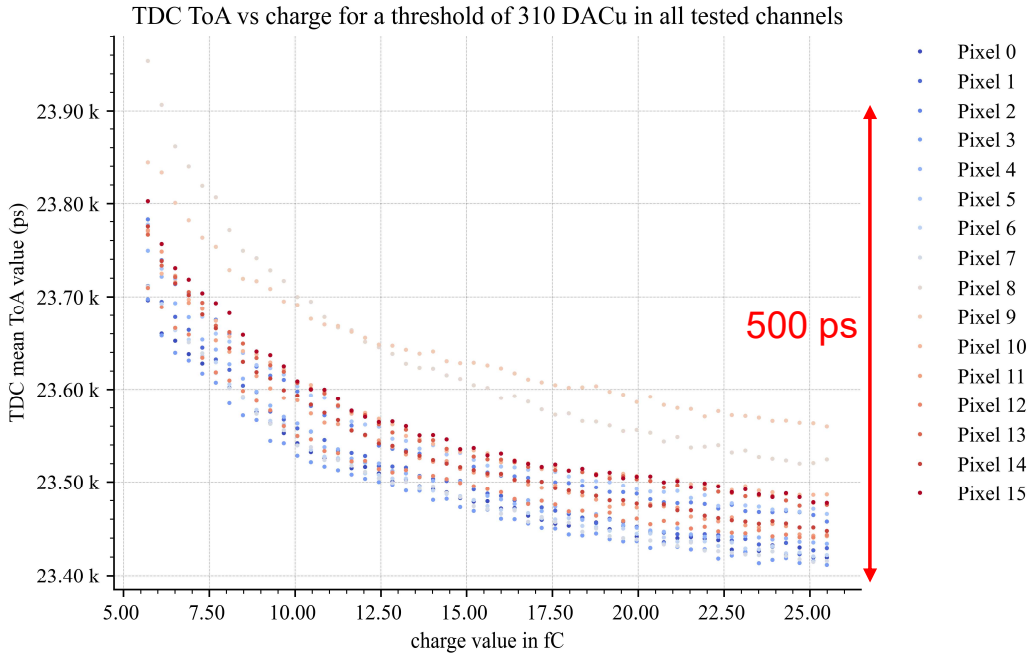
ADC mean & residuals – BNL Flipchip sensor



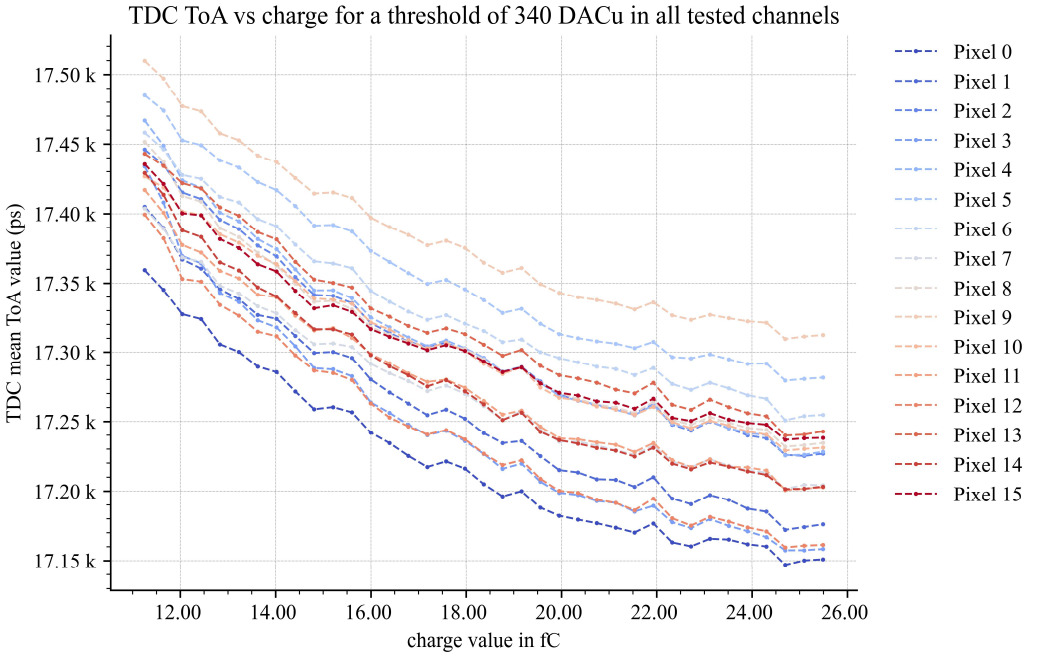
EICROC0 measurements : TDC ToA

- Time walk measurement :~400 ps

TDC ToA – no sensor

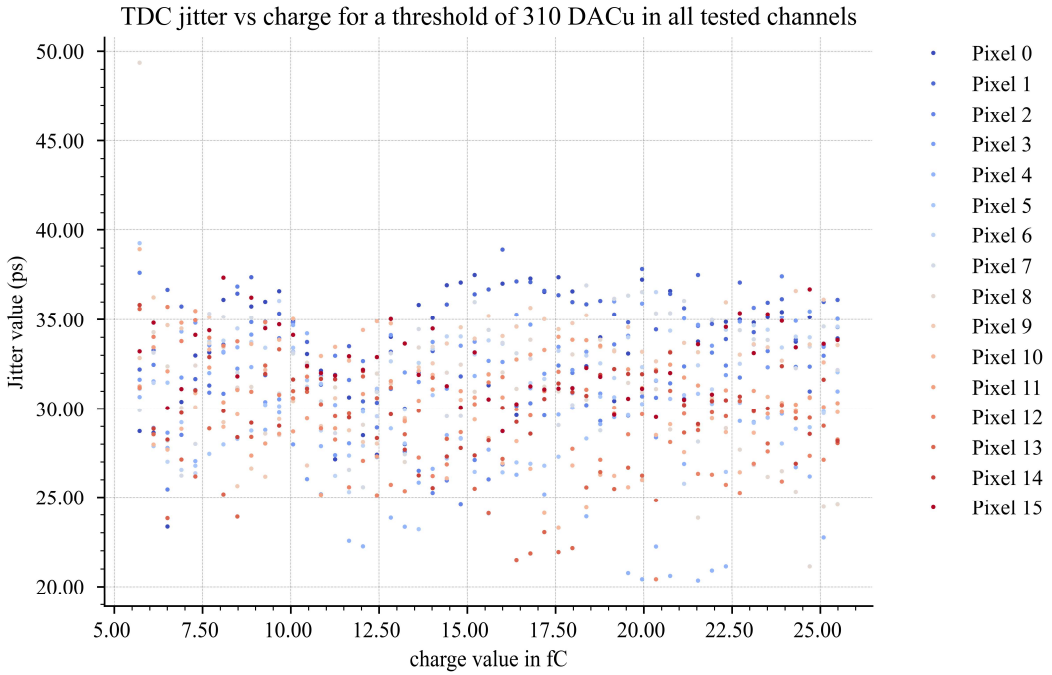


TDC ToA – BNL Flipchip sensor

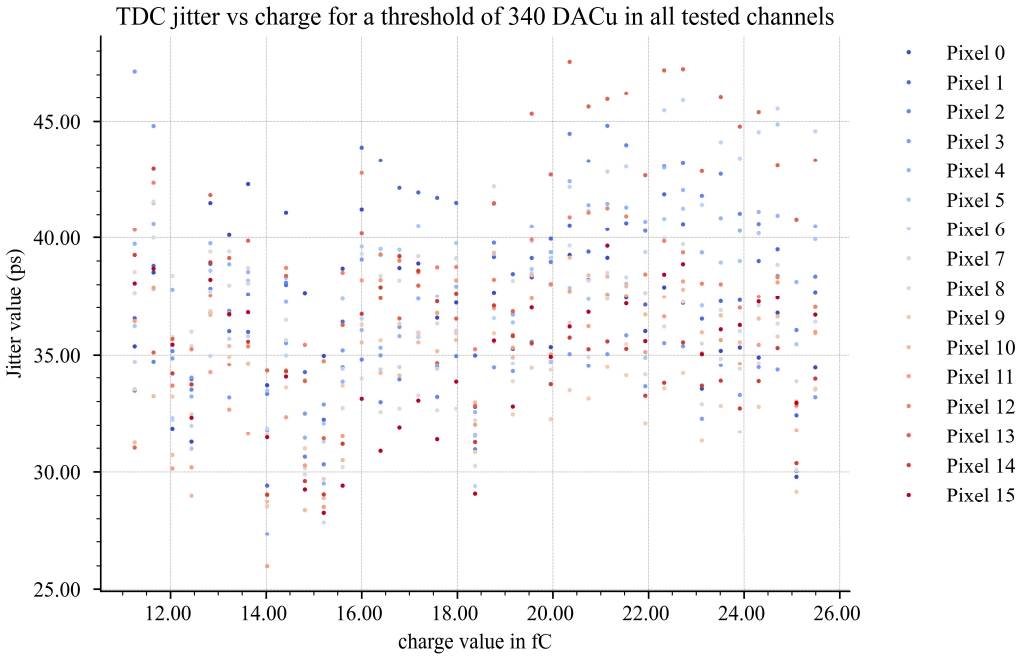


EICROC0 measurements : TDC jitter

TDC jitter – no sensor



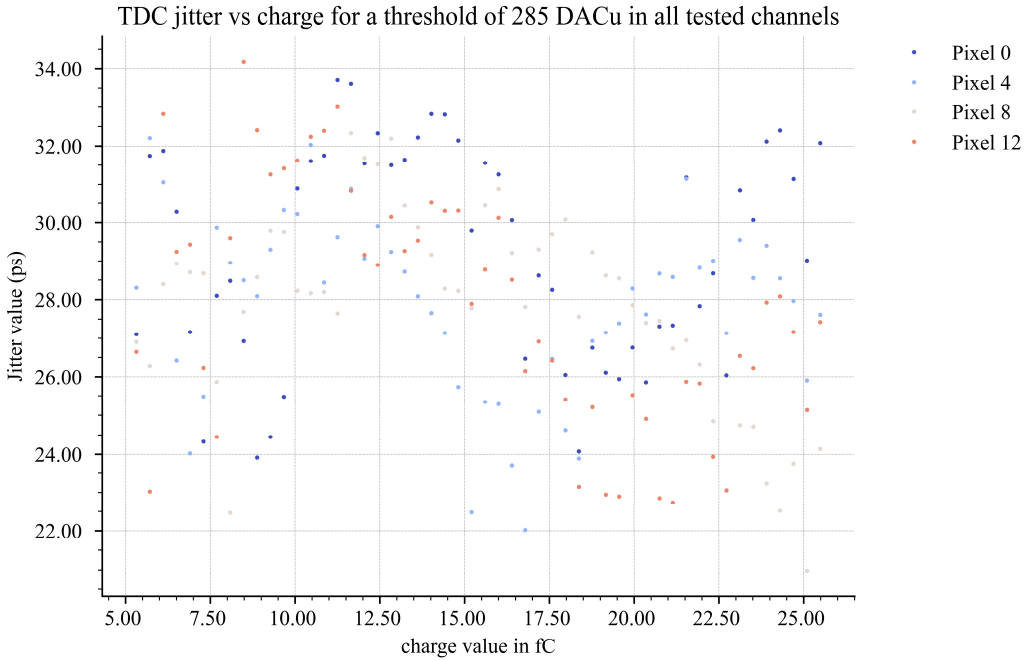
TDC jitter – BNL Flipchip sensor

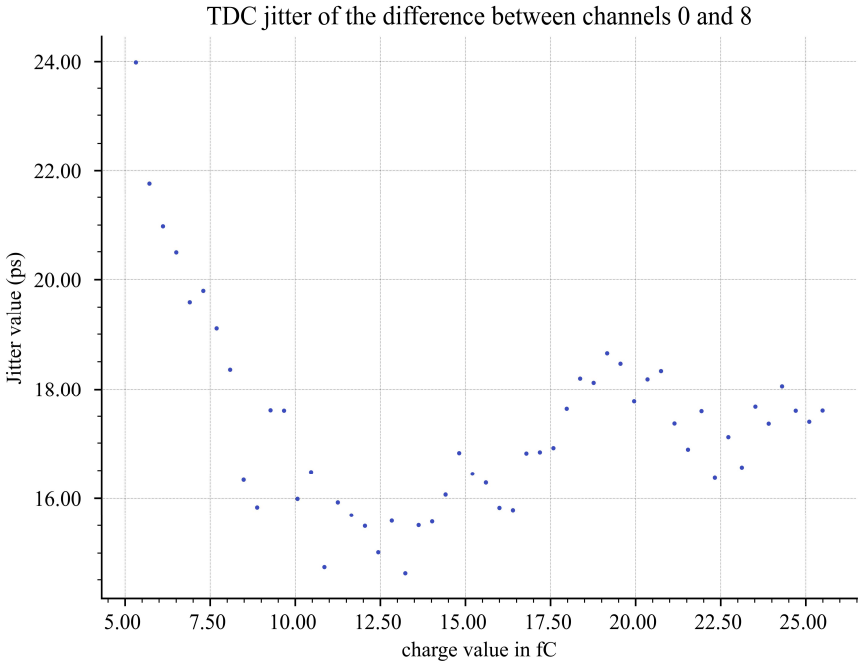


Charge range degraded with sensor, still need to properly calibrate the TDC for each channel and remove correlated noise

EICROC0 measurements : TDC jitter

TDC jitter results for a simultaneous injection in pixels of line 0 (0, 4, 8, 12)





- We can also inject in channels simultaneously with the test pulse to then remove the correlated noise from the TDC measurements
- The plot represents the TDC jitter for the difference of two channels that we injected in simultaneously
- Performance approaching what is measured with the oscilloscope

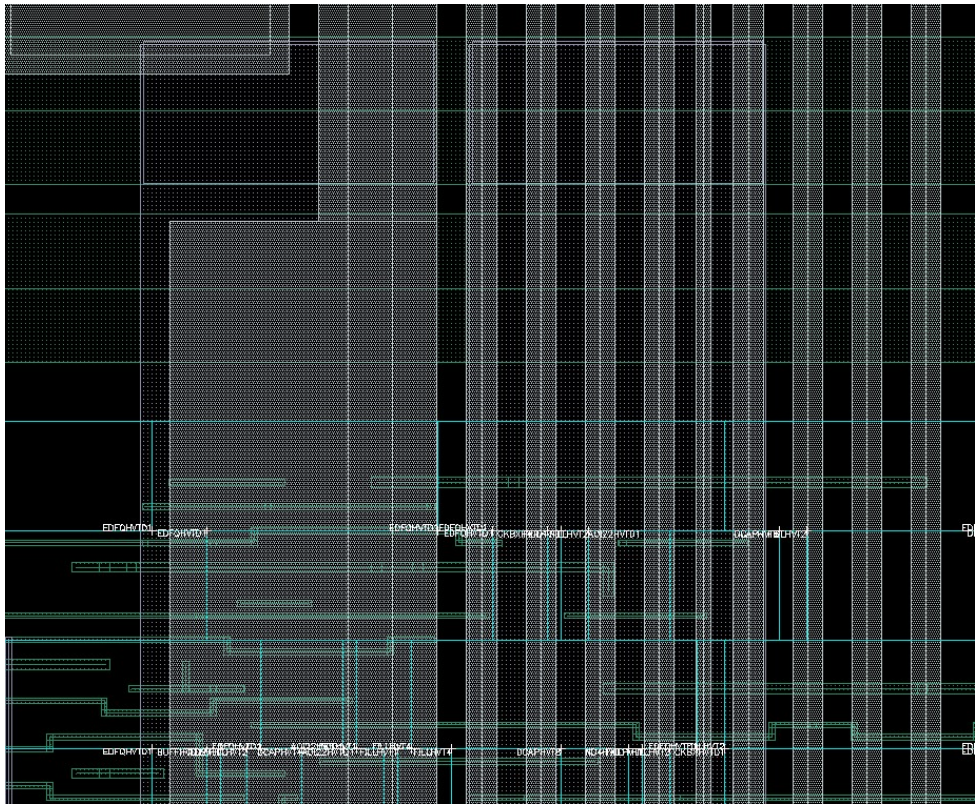
EICROC1 max rate

- Payload and readout speed
  - Each pixels provides 8 samples of 24 bits (12b TDC 12b ADC) at 40 MHz + header
  - 200 bits * 25 ns = 5 us/pixel
  - 128 pixels * 5 us = 640 us => ~1.5 kHz maximum rate per block of 4x32 ~10 Hz/pixel
  - Same rate for full chip with serialized 320 MHz output
  - Spec for RPs is 15 Hz/pixel (max 28 Hz)

- Future improvements
  - Payload reduction to 12b TD C + 5 samples of 8b ADC = 64 bits => ~30 Hz/pixel max rate
  - Zero-suppression : read only channels with hits and their (4-8) neighbours (for barycenters)
  - With 1 hit/column gives ~10 improvement => ~300 Hz/pixel max rate
  - A derandomizer would also be needed

EICROC0 Coupling investigation

- Large coupling seen on the ADC data which was completely hiding the signal up to 20 fC
- Large coupling capacitance between local (pixel) digital block and preamp / shaper bias lines
- Layout improved by adding exclusion zones and a shield between bias lines and digital
- Done in EICROC0A

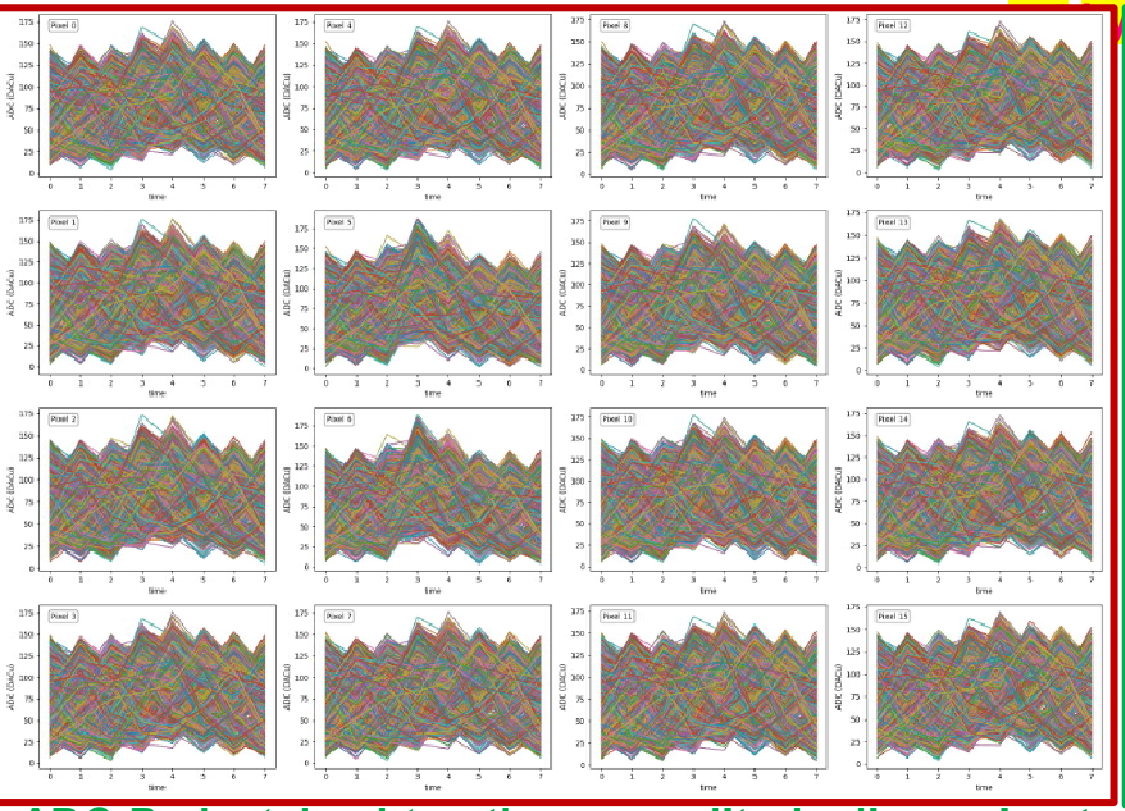


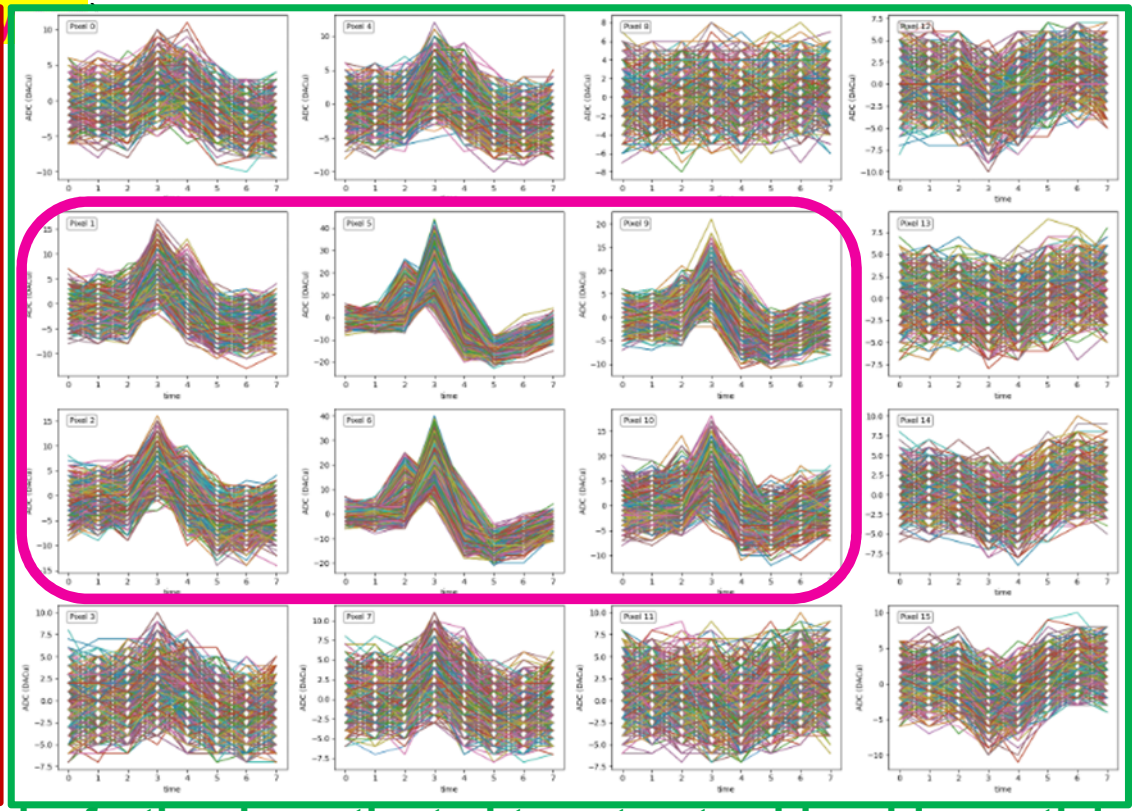
Bias / digital block layout in new EICROC ASICs

Pixelated AC-LGAD read-out characterization
Preliminary results with Infrared Laser (1/2)

Laser: 1 KHz, 70% attenuation (Sept. 18, 2025)

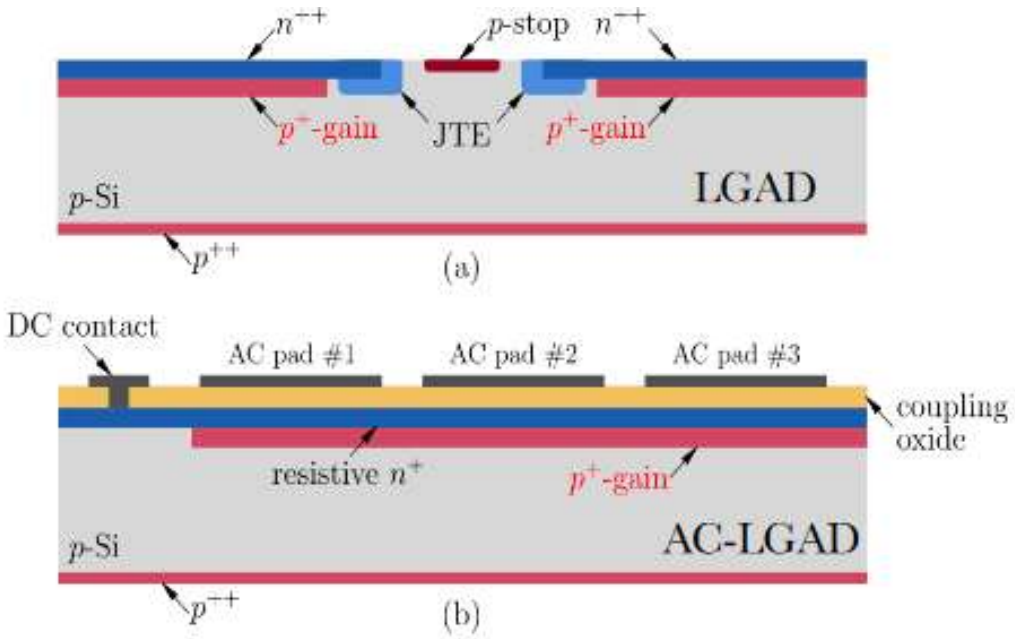
ADC waveforms (8 time samples = 8 points/event): **BEFORE** & **AFTER** **pedestal subtraction** (based on « far » pixel





ADC Pedestal subtraction + amplitude dispersion to be further investigated to extract achievable spatial resolution

Far-Forward Detectors



B0 spectrometer, OMDs & Roman Pots will consist of modules of pixelated AC-LGADs, also Forward Time of Flight system

RPs & OMDs requirements:

- 30 ps Time resolution
- < 50 μm Spatial resolution

Novel generation of Low-Gain Avalanche Diode (LGAD) sensors: « Alternating Current coupled LGAD, referred as AC-LGADs

4D-Tracking

- **Excellent time resolution**, *as LGADs*
- **Very good spatial resolution from charge sharing among neighboring pixels, relying on barycenter computation.**

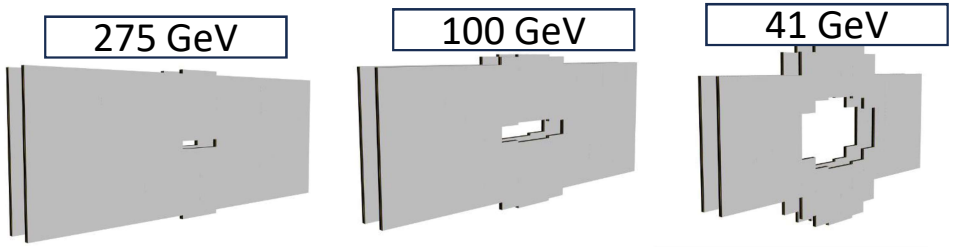
BUT no optimized chip exists yet to read-out pixelated AC-LGADs exploiting their 4D-tracking capabilities

Rationalization of design efforts: all pixelated AC-LGAD to be read-out by the same large scale (32 x 32 channels) ASIC: EICROC (EIC Read-Out Chip)

RP AC-LGAD + EICROC mounted on **movable plates and** in **vacuum** ⟺ **Very low power read-out chip + challenging cooling system**

Roman Pots design *(still under development)*

« Aperture » of the RP inversely ∝ dispersion of the scattered proton « beam » versus incoming proton energy



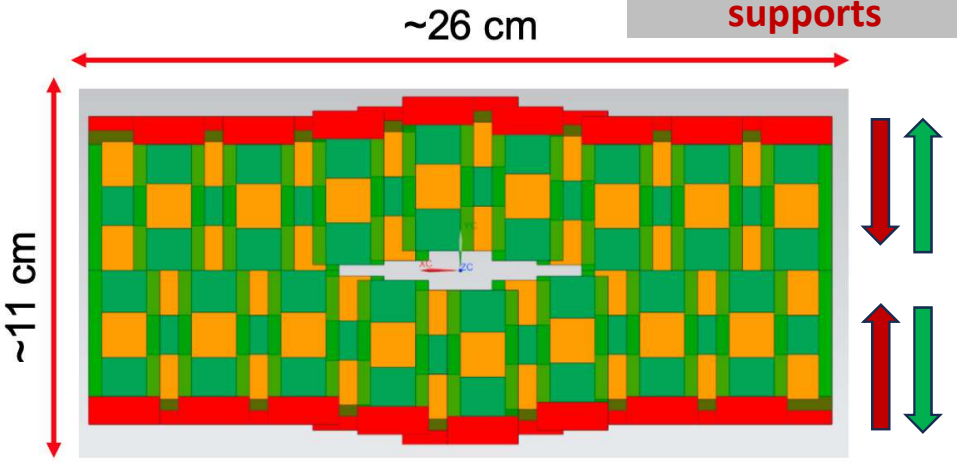
1 module = AC-LGAD + EICROC bump-bonded

EICROC (32 x 32)

AC-LGAD (32 x 32)

~ 1-2 W

Movable AC-LGAD supports



2 layers staggered composed of 16 modules each to provide full active-area coverage

1 stave = 3 modules staggered ~ 3-6 W