

EICROC2 digital architecture proposal Annual review

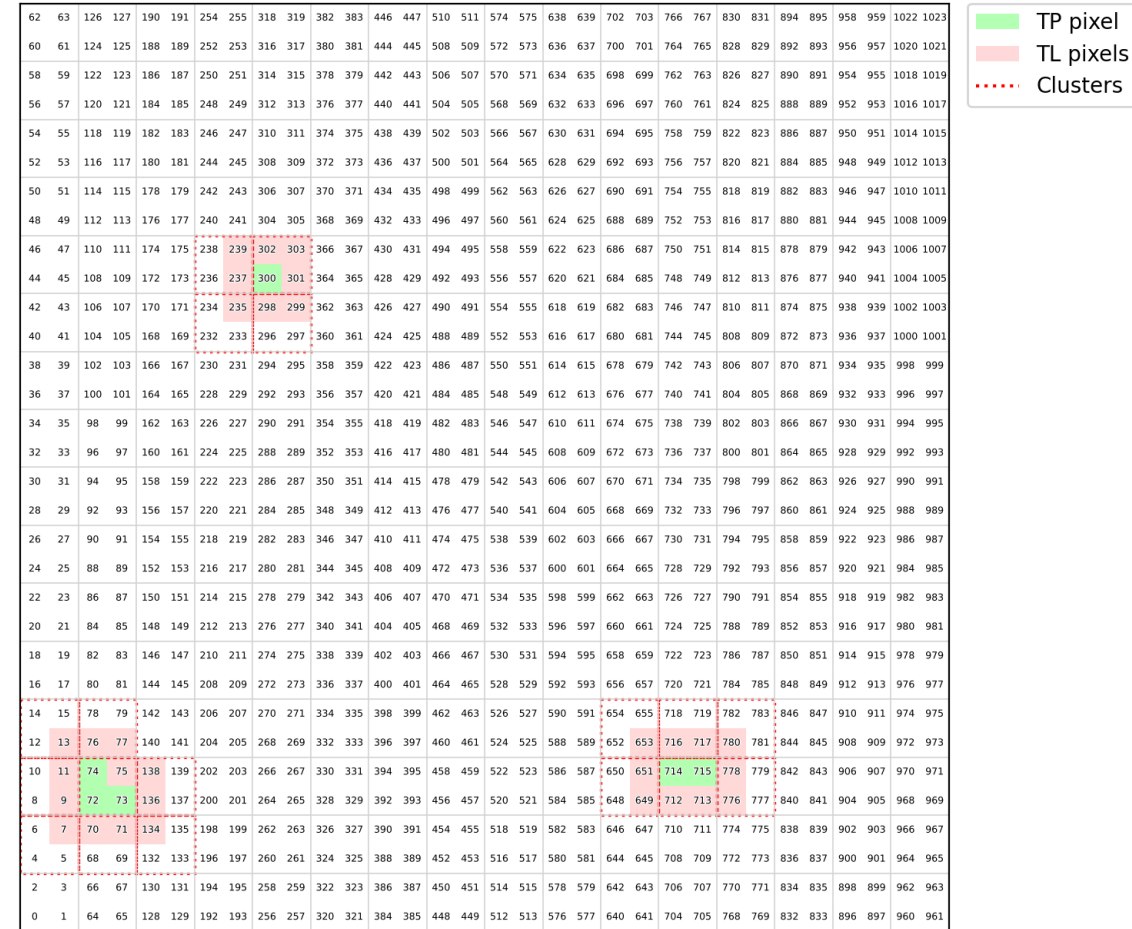
1st Apr 2026

Specifications for digital part of EICROC2



Specifications :

- 32x32 pixels
- 500μm pitch
- TSMC 130nm technology if possible
- Architecture must readout pixels hit and their neighbors
- Timestamped events (BCID)
- Digital area 120x500μm per pixel (<25% of pixel's size)
- Digital power <500μW per pixel
- Radiation tolerant (triplicated design)
- Read fast enough to limit data loss (< 0.05%)
- Normal operation hit rate : 20 Hz
- Maximum hit rate : 200 Hz



Digital interfaces : Commands and controls

Input clock :

- 320 MHz

Configuration :

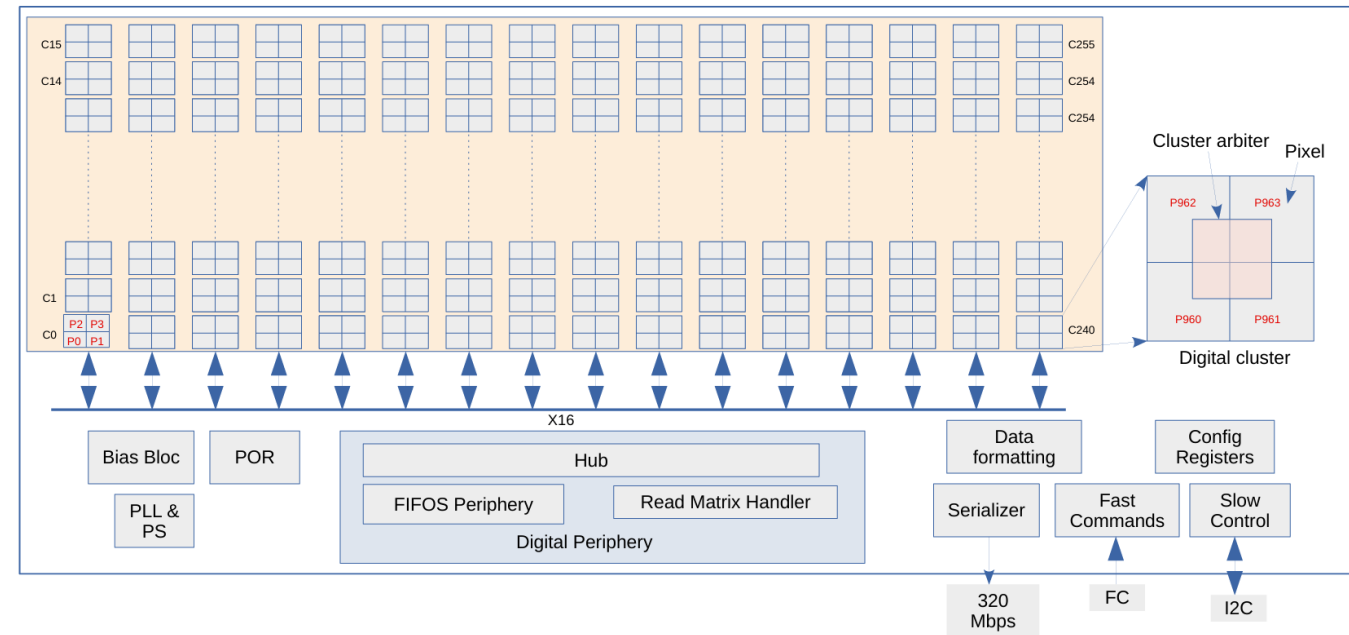
- I2C slave with wishbone interface to address registers
- Triplication + auto-correction

Fast Commands :

- Reuse fast commands from CALOROC

Data output :

- Serialized at 320 MHz, CLPS output
- Data formatting not discussed yet
- Probably encoding 8b/10b



Design plans overview

Architecture / RTL :

Based on **clusters of 4 pixels**, controlled by the periphery

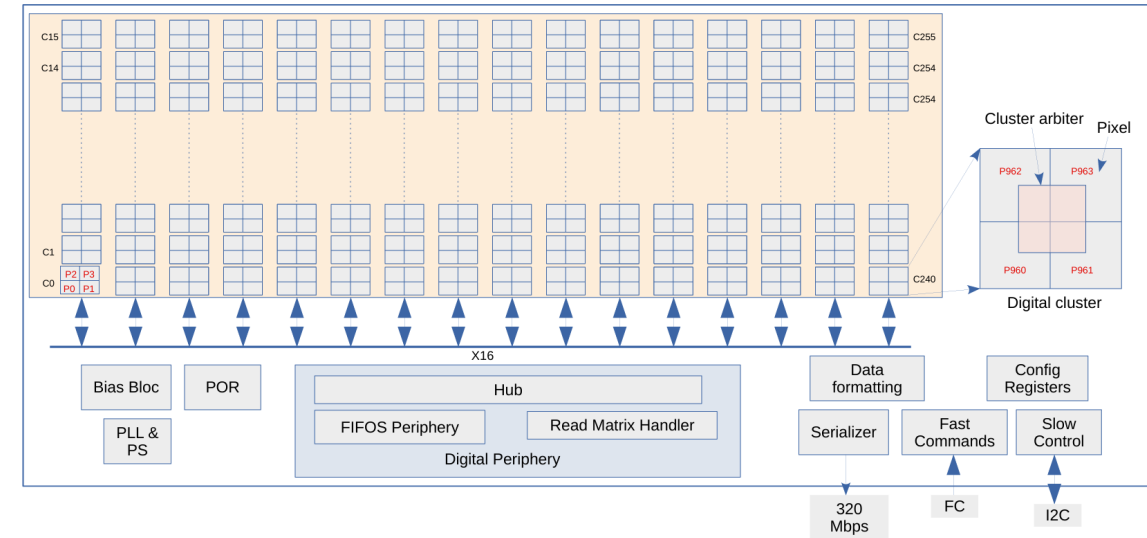
- Presented to local experts
- Document detailing the architecture is available
- Triplication using TMRG tool
- Architecture performance analyses (dead time, data loss, area, power consumption)

Physical implementation :

- 3-step implementation (cluster / column / top)
- Verifications : Timing, glitch analyses, DRV, DRC / LVS
- Power analyses : power consumption and Voltage Drop analyses

Verification using UVM :

- Set of tests : configuration, hits injection, fastcommands, ...
- Coverage
- Targets : RTL, Triplicated RTL, Post layout netlist
- Faults injection simulations (simulate bit-flips from radiation effects)



Global progression - RTL

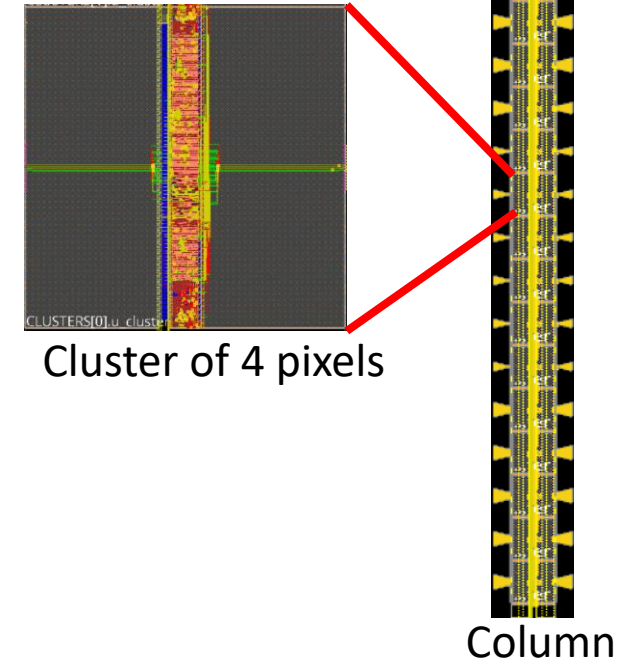
- First version of readout is available, simulations are on going
- Triplication is on going (Only config/controls, no triplication on data path)
- Readout data is stored in periphery for now
- Some periphery blocks RTL are not started yet

Block	RTL	TMR	Synth
Cluster	●	●	●
Column	●	●	●
I2C	●	●	●
FastCommands	●	●	●
DataFormatting	●	●	●
Serializer	●	●	●
Periphery Readout	●	●	●
Top	●	●	●

- Done
- On Going
- Not started

Global progression – Physical Implementation

- Digital on top flow for the matrix and digital periphery
- 3-step implementation : cluster / column / top
- First implementation of cluster and column
 - ➔ Check that it fits in allocated area using TSMC130 nm
- Setup of power analyses on going, preliminary results available



Block	Floorplan	CTS	Route	TimingAnalyses	DRC/LVS	PowerAnalyses
Cluster	●	●	●	●	●	●
Column	●	●	●	●	●	●
Top	●	●	●	●	●	●

- Setup of UVM environment just started
- Only one test is available : simple hits injection
- Code coverage

Task	Status
Verification plan	●
Injection Tests	●
Configuration Tests	●
Other Tests	●
Regressions	●
Coverage	●
Target : RTL	●
Target : TMR	●
Target : Post Layout Netlists	●

- LPCA team for EICROC :
 - 2 digital engineers (N. Kachkachi, A. Soulier) + 1 engineer part time on simulations (J. Bonnard)
 - 3 experts helping for specific points (H.Chanal for architecture, L.Royer for mixed-signal/system, N.Arveuf for UVM)
- Code and scripts shared on IN2P3 git
- Documentations shared on box IN2P3 (EICROC specs and Implementation spec)
- SOS server setup at Clermont (only local access for now) : Centralized database for IP sharing
- Available for technical review
- Planned schedule :
 - First iteration of full digital RTL architecture including all blocks : Late Summer 2026
 - First iteration of full chip implementation : Late Autumn 2026

Backup

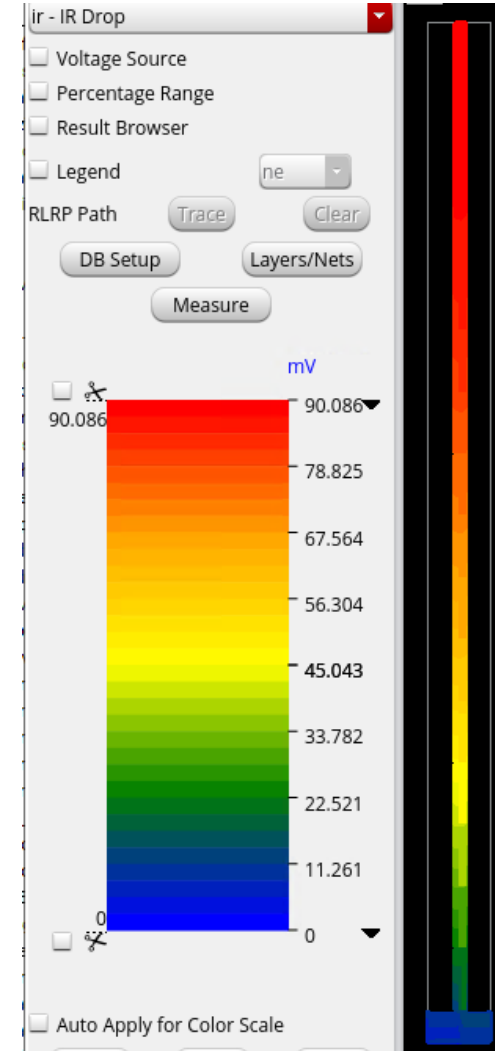
- Power Verification
 - Power consumption analyses for different cases :
 - Idle
 - Normal operating mode
 - Worst case operating mode (maximum activity)
 - Voltage drops analyses :
 - During reset
 - During worst case (maximum activity)
 - Analog powers
- UVM simulations
 - Setup verification plan and associated tests (configuration, hits injection, ...)
 - Simulation of RTL code / Triplicated RTL code / Post layout netlist
 - Faults injection simulations (simulate bit-flips from radiation effects)

- Power analysis flow setup for one case
 - 200Hz hit rate per pixel (aggressive case), typical corner
 - Worst case for ADC/TDC clocks

Clock	Internal Power	Switching Power	Leakage Power	Total Power
clk160_test	0.7277	2.246	0.003016	2.977
clk320_test	1.589	4.614	0.003528	6.207
clkB	0.8444	0.7234	1.134	2.702
clkC	0.8583	0.7542	1.163	2.776
clkA	4.473	1.65	1.167	7.289
Total	8.402	9.983	1.726	20.11

➔ ~314μW per pixel for digital power (preliminary result)

- Basic voltage drop flow is setup for digital power
 - ➔ Doesn't use realistic activity yet



VDD/VSS combined voltage drop