Istituto Nazionale di Fisica Nucleare

with DoE/eRD109 support

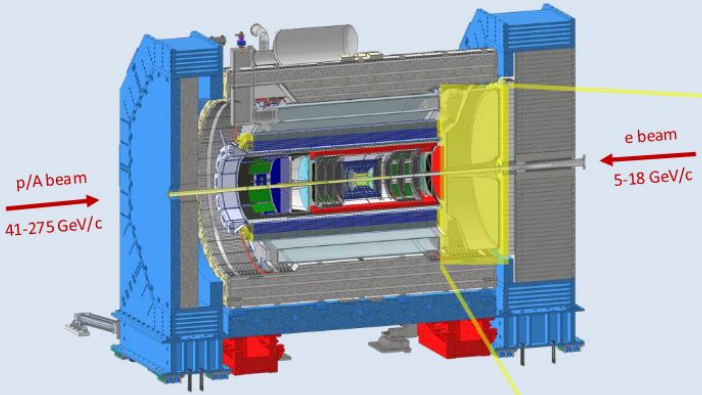
ALCOR Internal Review

Fabio Cossio (INFN Torino)
on behalf of the ALCOR group and dRICH Collaboration

22 April 2026

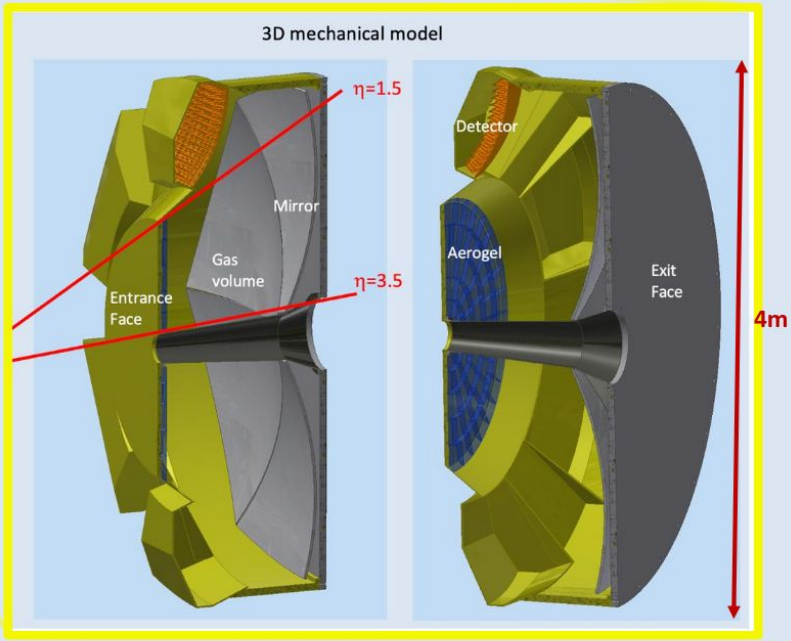
ePIC dRICH

ePIC dRICH



Dual-radiator Ring-imaging Cherenkov Detector (dRICH)

Essential to access flavor information



Goals:

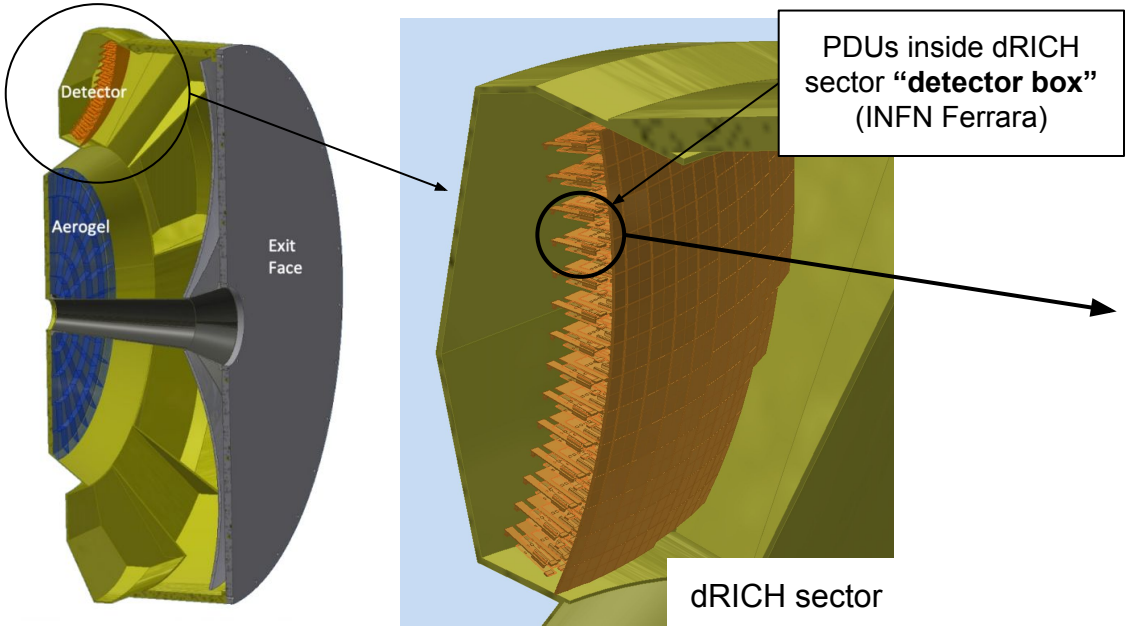
- Hadron 3σ–separation between 3 - 50 GeV/c
- Complement electron ID below 15 GeV/c
- Cover forward pseudorapidity 1.5 (barrel) - 3.5 (b. pipe)

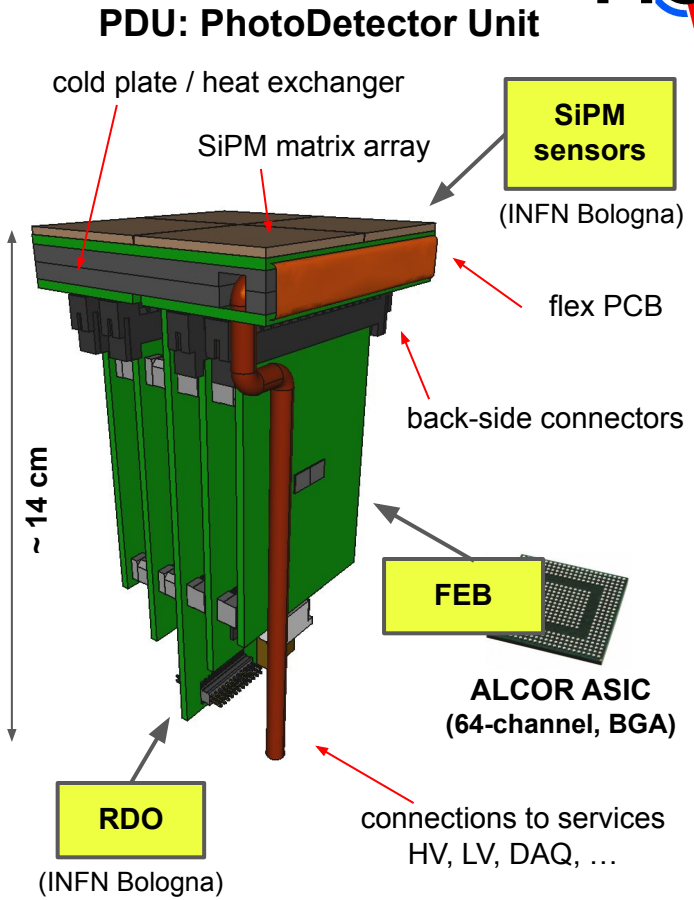
dRICH Features:

- Extended 3-50 GeV/c momentum range --> Dual radiator
- Single-photon detection in high Bfield --> SiPM
- Limited space --> Compact optics with curved detector

M. Contalbrigo RICH2025, Mainz, September 18th, 2025 2

dRICH electronics





- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 6 sectors: 208 PDUs/sector → **1248 PDUs** for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3** (64-channel)
- **319488** readout **channels**

ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

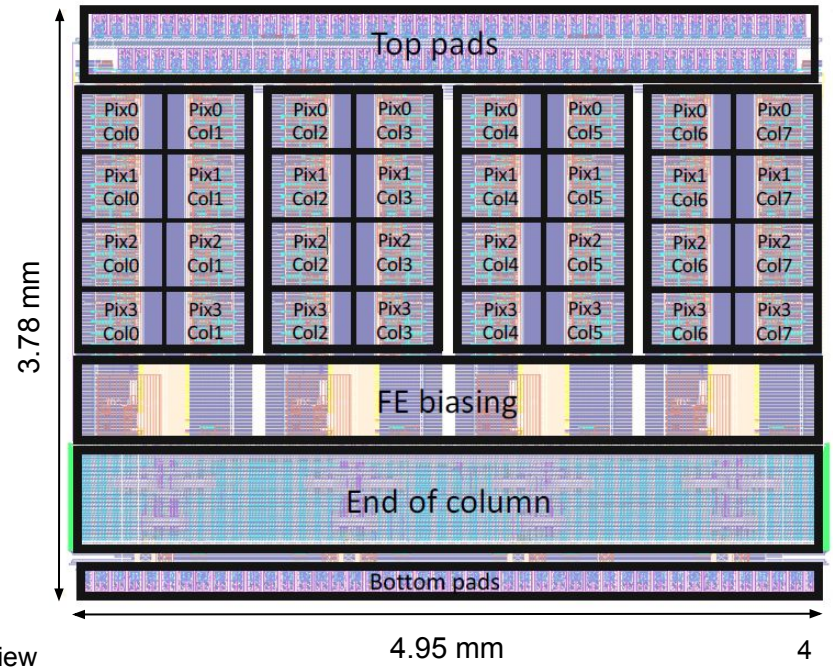
Main requirements:

- provide **single-photon time tagging** of signals coming from SiPM sensors
- cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

ALCOR-32 (ALCOR v2 - v2.1)

- **32-pixel** matrix (8x4) mixed-signal ASIC
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Trigger-less readout with fully digital output: **4 LVDS 320 MHz** DDR Tx links
- **Wire-bonded** on PCB
- Power consumption **~10 mW/channel**
- **0.11 µm CMOS technology**

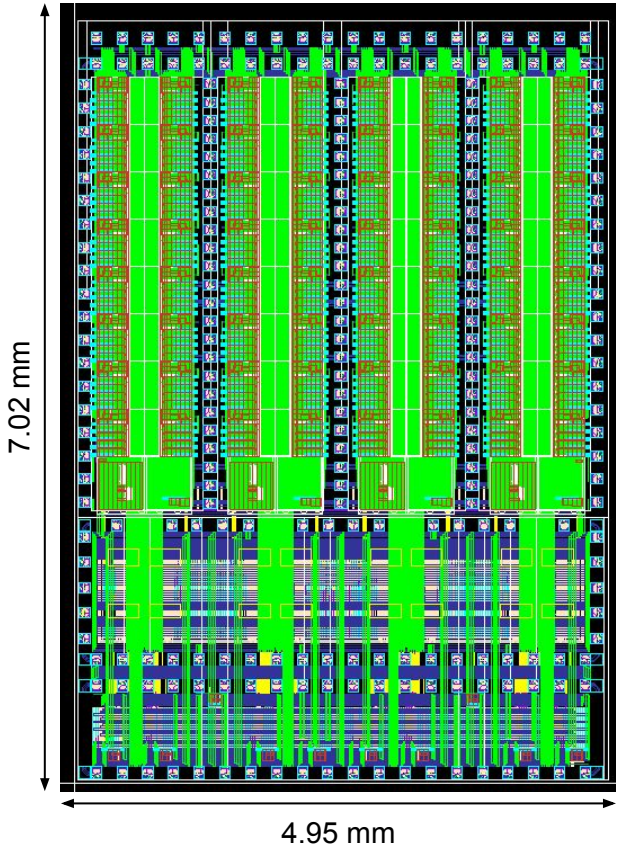
https://doi.org/10.1016/j.nima.2024.169817



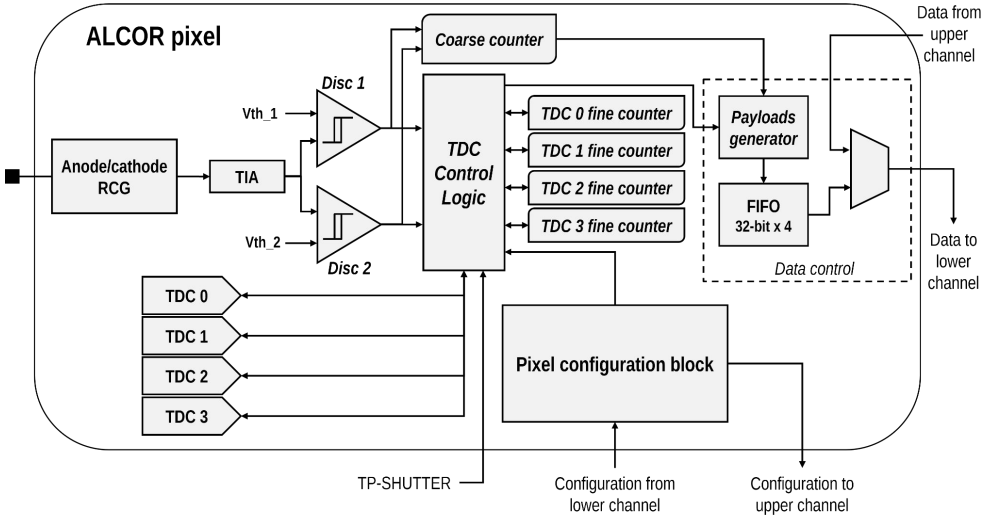
ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

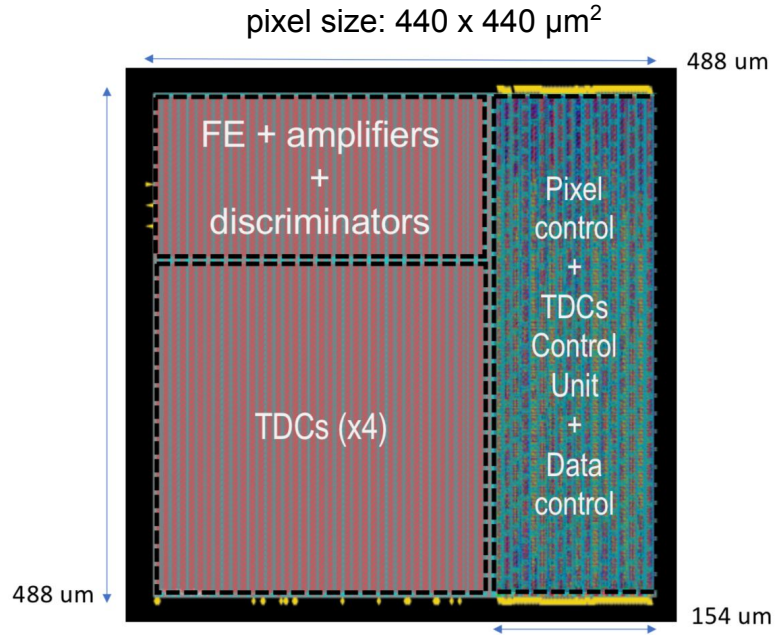
ALCOR-64 (ALCOR v3)

- **64-pixel** matrix (8x8) mixed-signal ASIC
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- **Shutter** to inhibit events digitization (asynchronous with ns time window) and **suppress out-of-time SiPM DCR hits**
- Trigger-less readout with fully digital output: **8 LVDS 394 MHz** DDR Tx links
- Flip-chip **BGA package**
- Power consumption **~12 mW/channel**
- **0.11 µm CMOS technology**



Pixel architecture



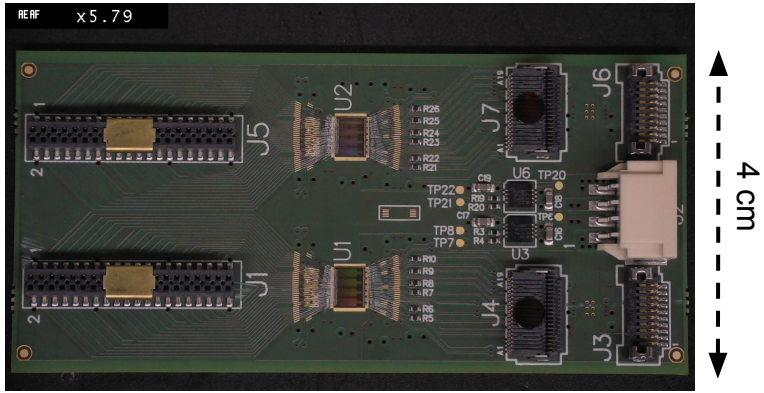


- **Dual-polarity RCG input stage** current conveyor (Z_{in} **= 10-20 Ω**) + **TIA** with 4 gain settings
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC)
- **4 TDCs** based on **analogue interpolation** with **20-40 ps** time-bin (at 394 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- TP-**Shutter** to inhibit events digitization (asynchronous with ns time window in new version) and suppress out-of-time SiPM DCR hits

dRICH prototype readout system

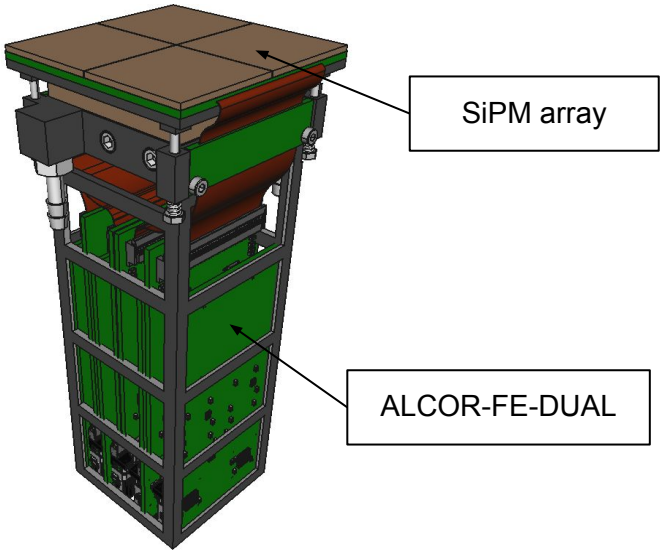
ALCOR-FE-DUAL board

- Two **ALCOR-32** ASICs **wire-bonded** on the PCB
- **4 ALCOR-FE-DUAL** boards for each PDU (**256 channels**)
- System used for **2023-25** ePIC dRICH beam tests



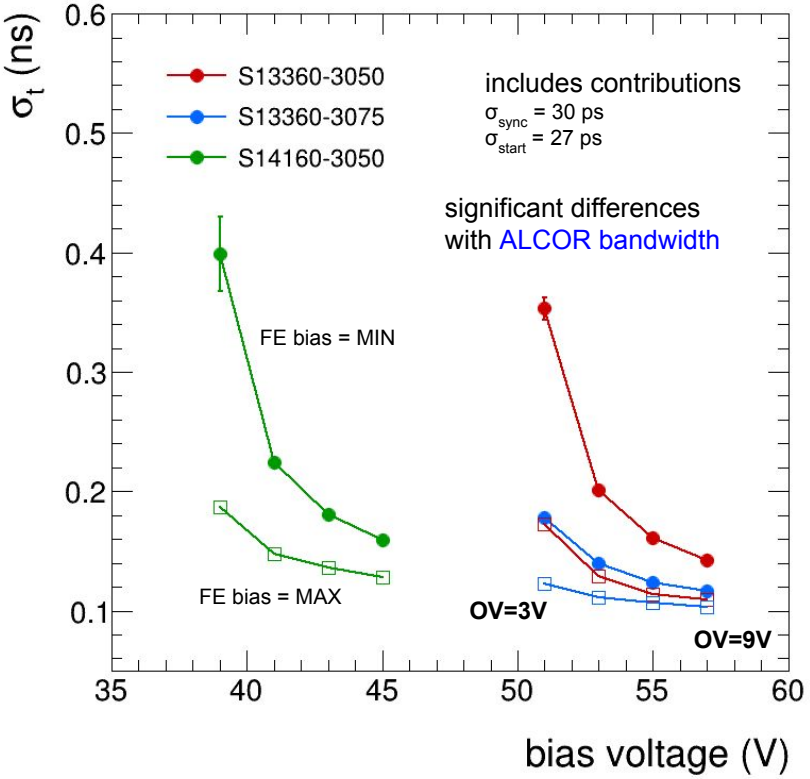
Designed using specifications close to final FEB: very similar space constraints and same number of channels (64)

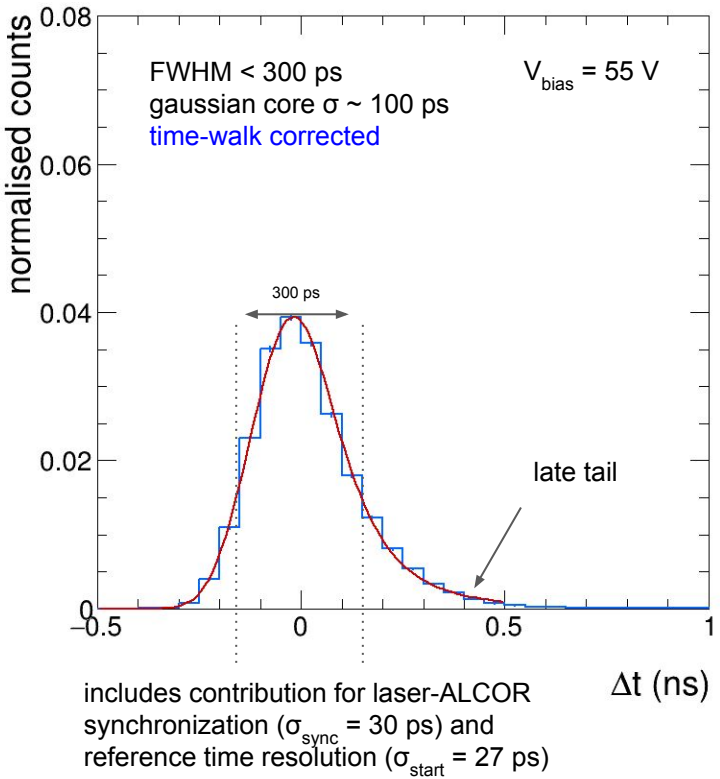
ePIC dRICH Prototype photodetector unit (PDU)



Prototype to test and validate PDU geometry and functionality (no RDO)

Laser timing measurements





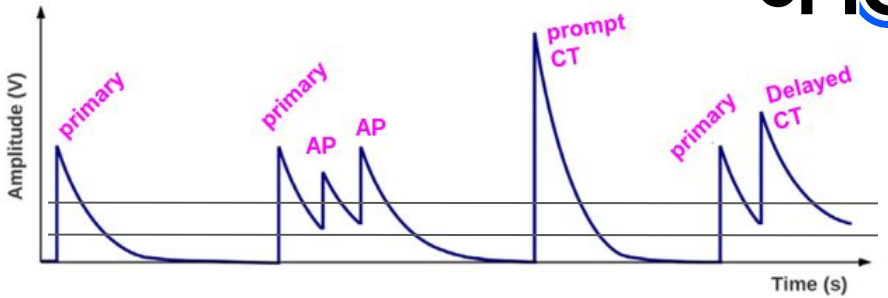
includes contribution for laser-ALCOR synchronization (σ_{sync} = 30 ps) and reference time resolution (σ_{start} = 27 ps)

➔ Better time resolution with **75 µm SPADs**

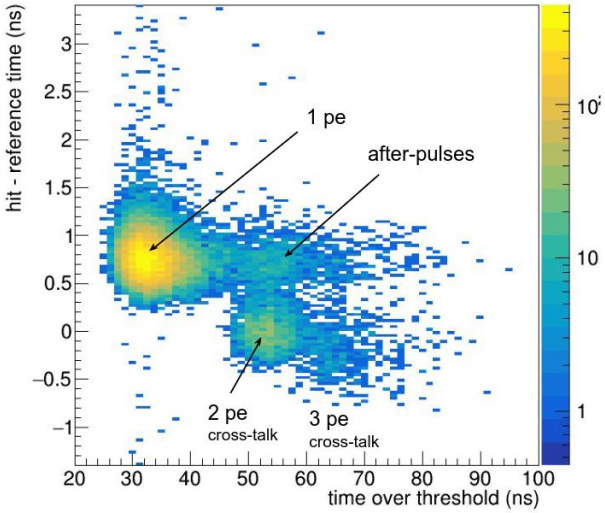
➔ Comfortably below **σ_t = 150 ps** also at low Vbias

Time walk correction

Time walk correction needed to improve overall time resolution → studies with laser setup using ***ToT*** and ***SlewRate*** measurements



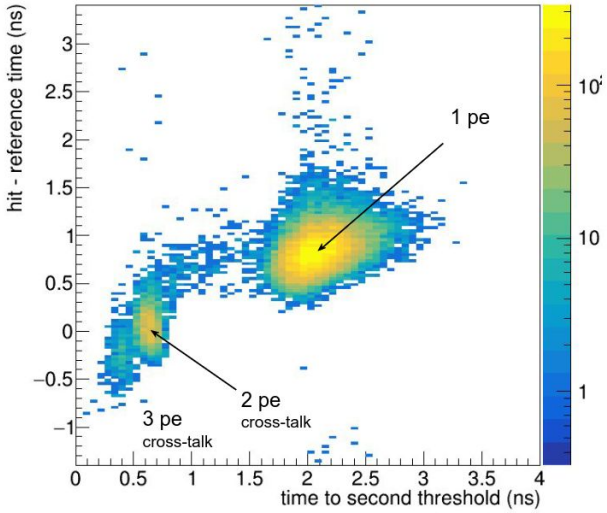
ALCOR ToT mode



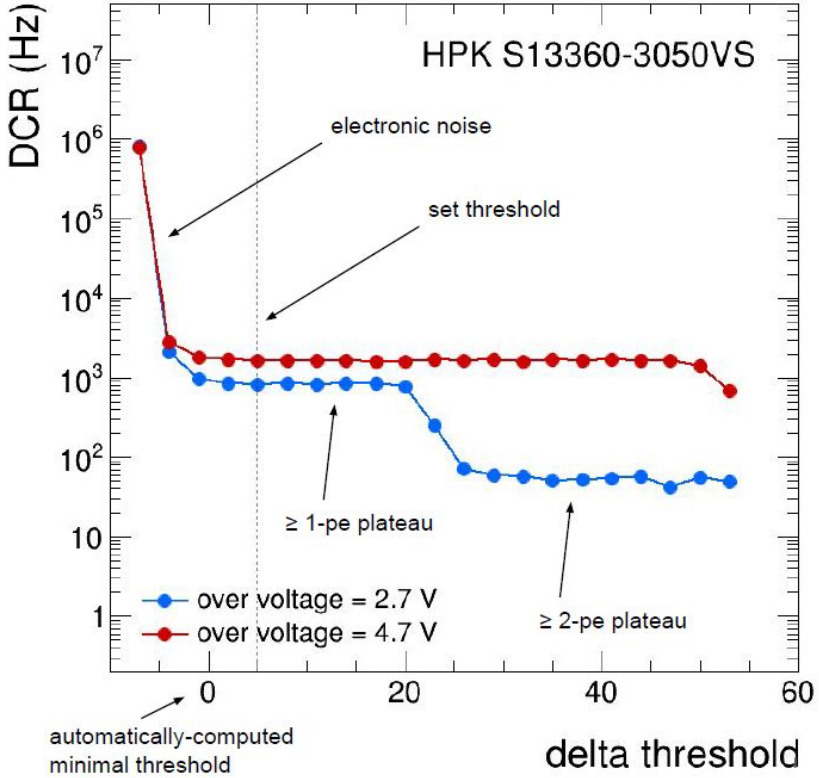
✗ ***ToT mode*** cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

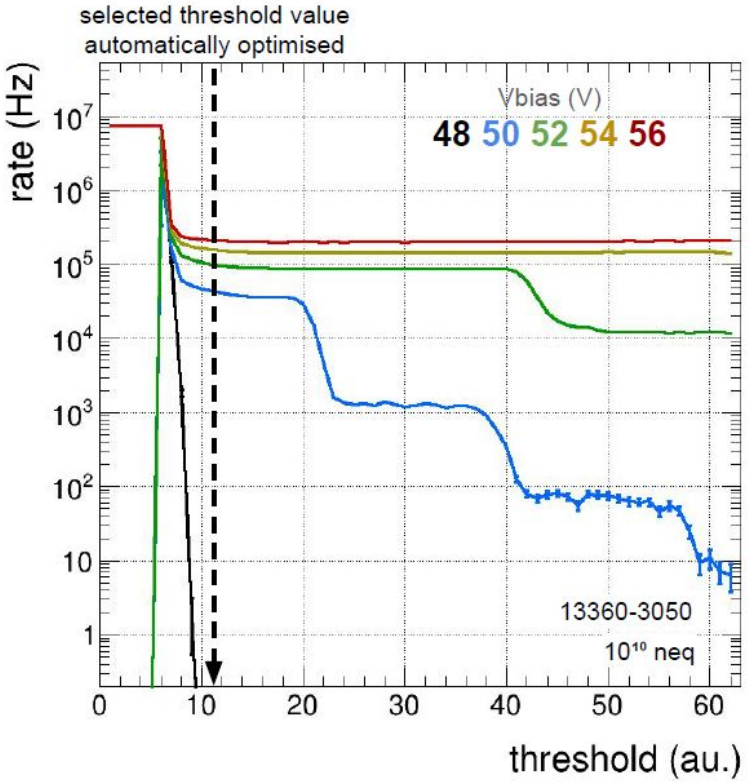
✓ ***SR mode*** provides better separation

ALCOR slew-rate mode



ALCOR threshold scan



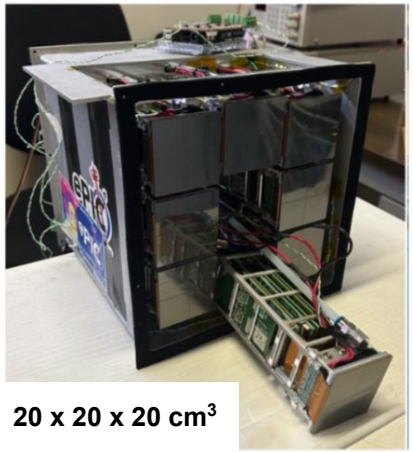


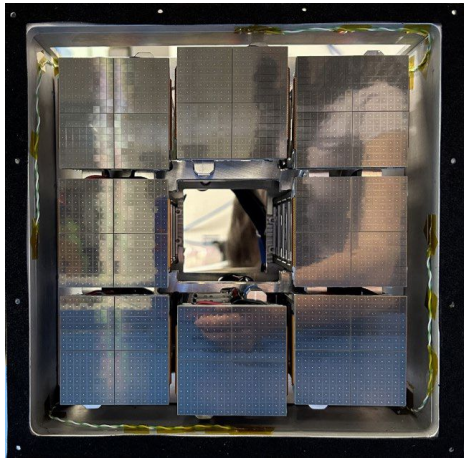
Beam tests at CERN-PS

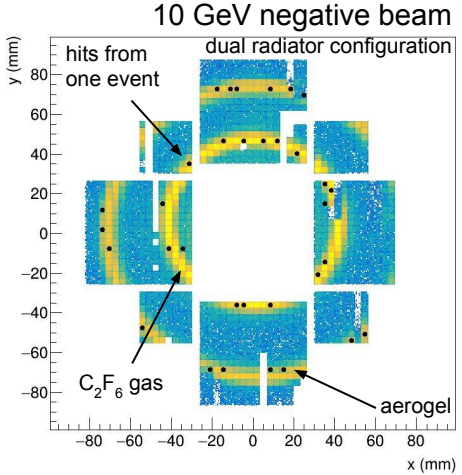
Successful beam tests with prototype **dRICH** and **PDUs** (CERN-PS, October 2023, May 2024)

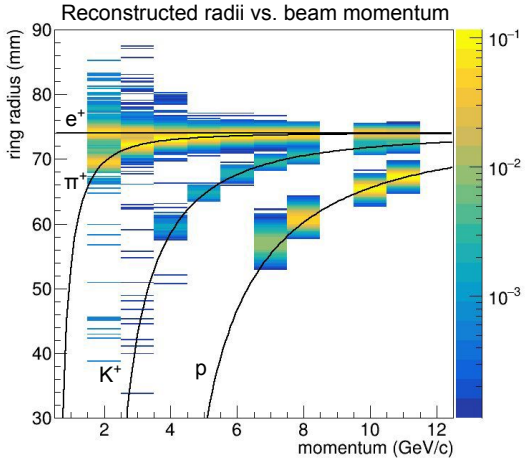
- HPK S13360-3050 and S13360-3075 (3x3 mm^2, T = -30/-40°C)
- 32 FE-DUAL (64 ALCOR-32, **2048 channels**)
- DAQ: Xilinx Kintex 7 KC705

Realistic detector plane based on dRICH PDUs Validated

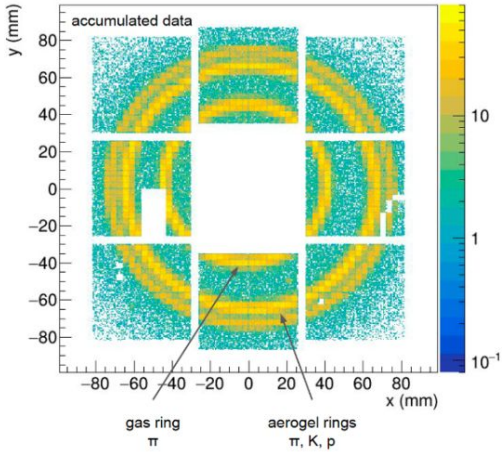


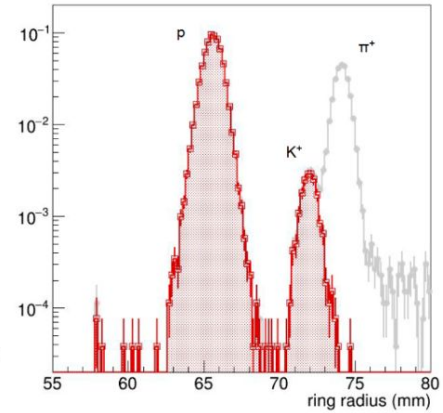






dRICH prototype got the expected performance and radiator interplay





Radiation tolerance

The dRICH-PDUs are in a moderately hostile radiation environment

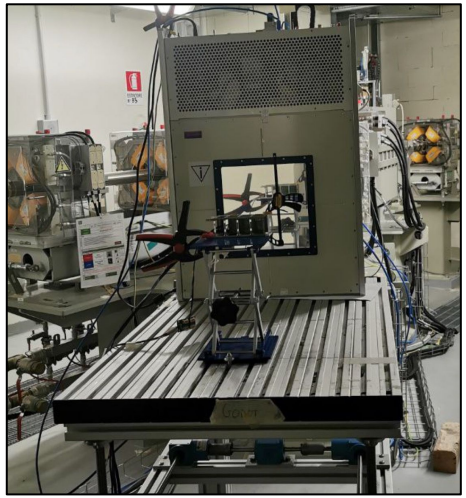
- **Φ (p+n > 20 MeV) = 700 Hz/cm^2**
- **TID ≅ 2.3 krad (for 1000 fb^{-1})**

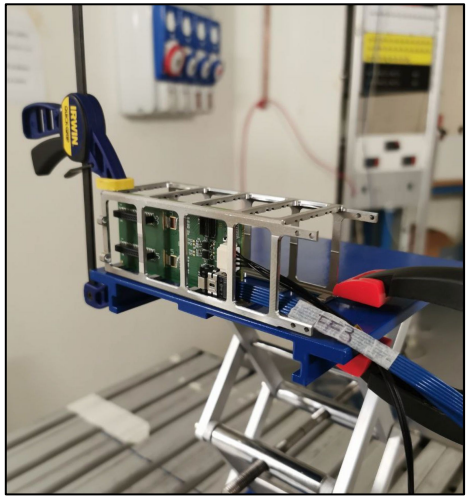
} safety factor of 5 included

➢ Irradiation tests campaign: **SEU/SEL** and **TID tests** at Centro of Proton-Therapy in Trento with **ALCOR-32** in **Jul 2024** and **Dec 2024**

- Beam: 100 MeV proton
- Intensity: 10 - 100 nA
- Runs: typically 600 s
- Fluence collected per run: 10^{11} - 10^{12} p/cm^2

- **Total fluence: 4.64 · 10^{12} p/cm^2** (Jul 2024) and **3.2 · 10^{12} p/cm^2** (Dec 2024)
- **Total TID: 436 krad**





Detailed results presented at the 29th Jan 2025 dRICH Meeting: https://indico.bnl.gov/event/26313/

SEU/SEL results (July 2024)

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR $\sigma = (9.4 \pm 1.8) \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = (7.6 \pm 1.1) \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- **PCR** **$\sigma = (3.3 \pm 0.5) \cdot 10^{-15}$ cm^2/bit** — pixel register → TMR (with auto-correction bug)

SEU due to accumulating bit flips in triplicated registers over time

SEU rate in ePIC:

- dRICH Flux = 140 (h > 20 MeV) / (cm^2 s)
- ALCOR bits: (2048 + 192) = 2240 → ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 · 4480 = 2.2 · 10^7 bits

➢ $\sigma = 3.3 \cdot 10^{-15}$ cm^2/bit → **MTBF** = $9.8 \cdot 10^4$ seconds → every **27 hours**

➢ No latchup events (from power supply currents monitoring)

SEU rate is within the expected manageable levels

SEU/SEL results (December 2024)

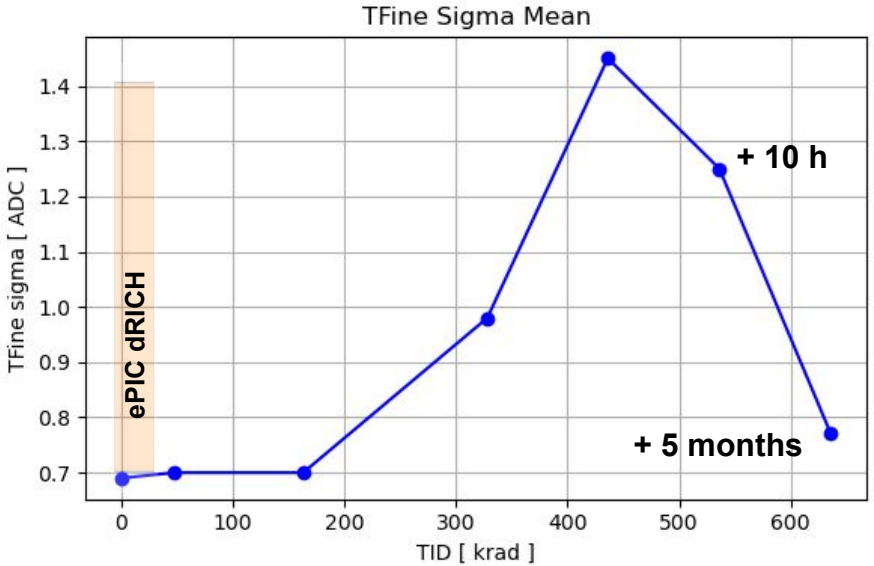
ECCR/BCR/PCR registers checked against SEU (every second), **PCR re-written every 10 seconds to "mask" TMR auto-correction bug**

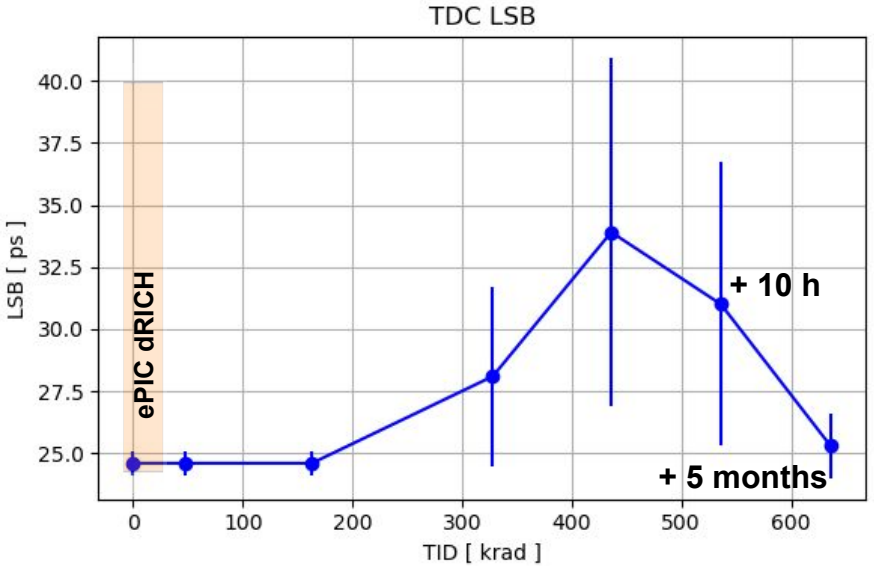
- ECCR $\sigma = 9.8 \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- BCR $\sigma = 6.1 \cdot 10^{-14}$ cm^2/bit — periphery register → no TMR in ALCOR v2.1
- PCR **no SEU detected** — re-written every 10 seconds to avoid TMR auto-correction bug

ALCOR-64: TMR SEU protection added also for periphery registers (used *CERN TMRG tool* for all registers), Hamming code SEU protection for FSMs

TID results - TDC error & LSB

***last two points = 436 krad after 10 hours and 5 months**





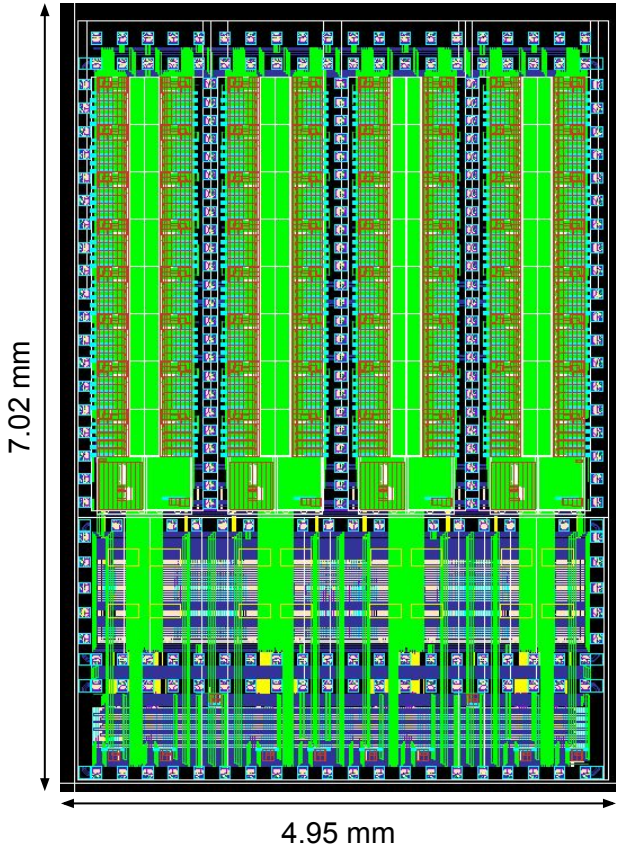
- Technology is sufficiently radiation tolerant to be used in the ePIC dRICH environment
- Similar results w.r.t. irradiation tests performed on another ASIC with same technology [1]
- Also other FEB components will be tested and validated

[1] F. Lenta *et al* 2024 *JINST* **19** C04047, DOI 10.1088/1748-0221/19/04/C04047

ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

ALCOR-64 (ALCOR v3)

- **64-pixel** matrix (8x8) mixed-signal ASIC
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- **Shutter** to inhibit events digitization (asynchronous with ns time window) and **suppress out-of-time SiPM DCR hits**
- Trigger-less readout with fully digital output: **8 LVDS 394 MHz** DDR Tx links
- Flip-chip **BGA package**
- Power consumption **~12 mW/channel**
- **0.11 µm CMOS technology**

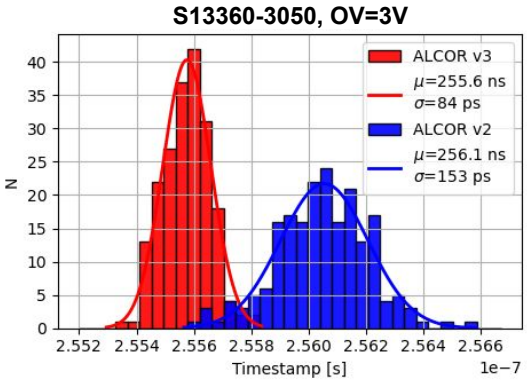


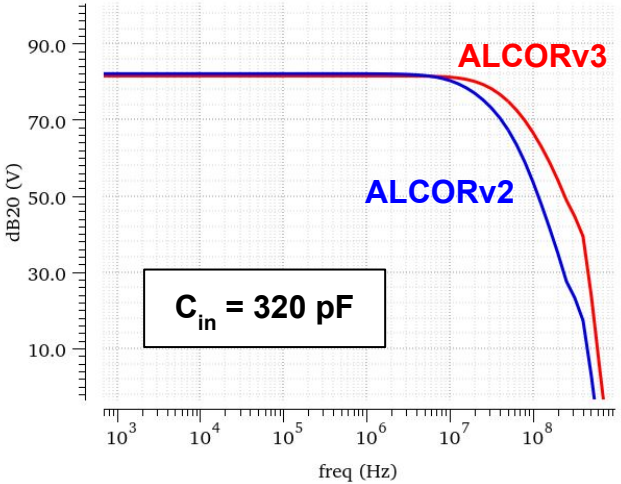
ALCOR v3 - frontend

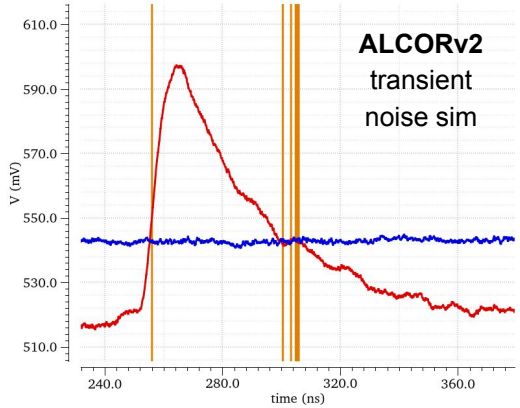
Small revisions on ALCOR FE design

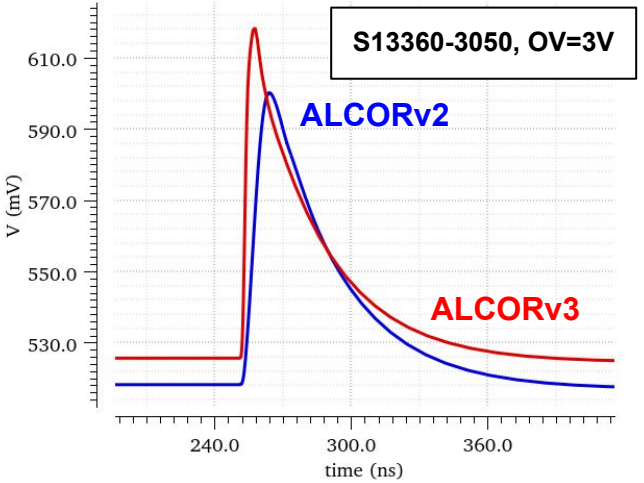
- **Increased amplifier bandwidth** to improve time resolution
  - transient noise simulations
  - Vth = 0.5 p.e.
  - **jitter: 153 ps → 84 ps**

- **Discriminator** with programmable **hysteresis** to avoid re-triggering on slow tail with low thresholds







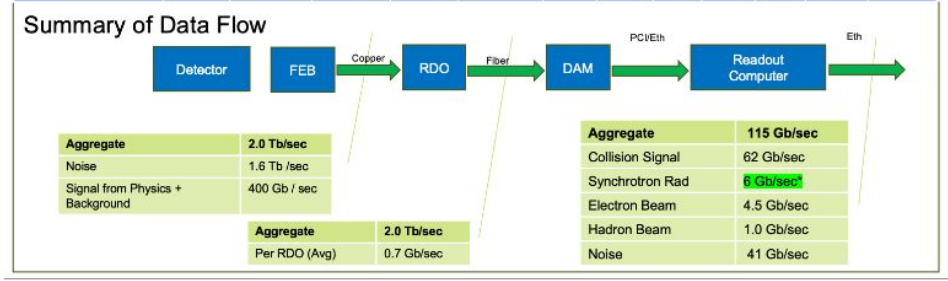


dRICH recap in three slides (III): ePIC throughput

Summary of Channel Counts and Data Flow in ePIC

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					187	4976	323	323	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364		1364	30	50	12
PID Cherenkov			318k		143k	1334	1334	1242	1334	33	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		3.4k					25	289	11	37	8
Lumi		128k	5.1k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**2,661**	**10,234**	**2,393**	**4,113**	**113**	**1,774**	**109**

Summary of Data Flow



Scale of the system:

- **Electronics**
  - ~ 25 detector subsystems
  - ~ 5 Readout Technologies
  - ~ 2500 RDOs (on detector/in racks)
  - ~ 110 DAM boards (DAQ room)
  - GTU (with interface boards)
- **Maximum Data Volume**
  - ~ 2 Tb/sec digitized
  - ~ 115 Gb/sec recorded
- **Online Computing (Echelon 0)**
  - ~200 nodes (DAQ Room/SDCC)

* Synchrotron radiation caveats:
1. Rates are based upon hit rate for all ePIC detectors. In fact, data volumes depend upon specific detector hit (64 bits/hit assumed)
2. Highest Synchrotron radiation / electron beam gas will correspond to lower values for collision signal
3. Plan to analyze by component soon

dRICH
1.3 Tb/s

Note: all detector rates without updated beam background estimates

Slide courtesy: D. Abbott and J. Landgraf

Note
at EIC zero-day (and during all commissioning) throughput will be 10^2 lower

how to approach dRICH throughput?

0 cool down the sensors → -40 C
heal the damage → annealing
optimize overvoltage and choice of the sensors
sensors — INFN-BO/INFN-FE/

1 electronics gated: ALCOR shutter
electronics, clock distribution, RDO — INFN-TO/INFN-BO

2 understand if the event is noise or signal → **deploy ML techniques on DAM**
DAM — INFN-RM

3 understand if the event is noise or signal with a **dRICH interaction tagger** → give a trigger to DAM
INFN-GE

4 get an external trigger from another sub-detector (Forw. HCAL?) → give a trigger to DAM
ePIC

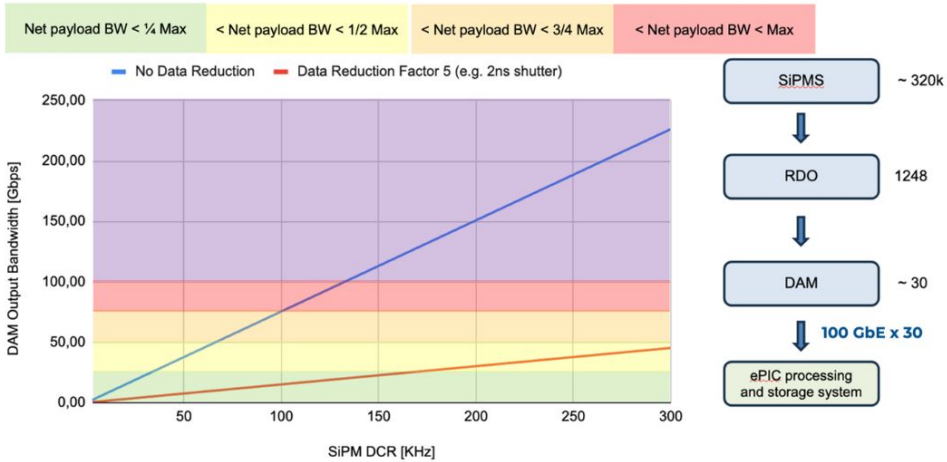
dRICH Interaction tagger: S. Vallarino @EICUG-ePIC 2025

ML for data reduction in DAMs: C. Rossi @RICH2025
dRICH Online Data Filter: C. Rossi @dRICH General Meetings on dRICH Data Filter

ALCOR shutter

ePIC streaming data acquisition system
(no traditional hardware trigger)

- Operation at **0.5 p.e. threshold** → DCR noise up to **300 kHz/channel** (at max SiPM radiation damage)
- Overall data **Reduction Factor of 5** allows us to stay safe up to 300 kHz/channel DCR
- It can be achieved via **shutter**, **NN algorithms**, **external trigger** or a combination of them



- **ALCOR shutter**: “inhibit” pixel digital logic to suppress out-of-gate DCR hits and **reduce data throughput:**

$$\text{Reduction Factor} = \frac{\text{EIC bunch crossing period}}{\text{shutter time window}} = \frac{10.2\ \text{ns}}{t_{shutter}}$$

- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time → **use first period of ePIC data taking to optimize shutter calibration** (electronics and physics contributions)

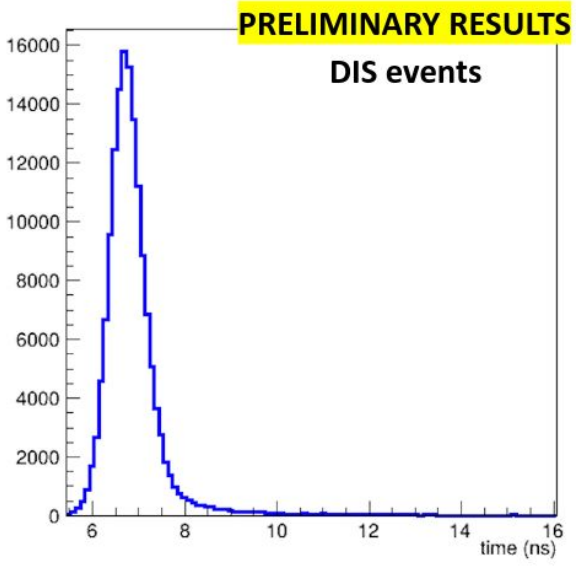
Will the shutter be effective?

Simulations of hit time distribution at dRICH entrance window (before aerogel) within the context of dRICH Interaction tagger studies

- Hit time distribution (primaries) has Gaussian shape + a tail
- Bulk of primary hits lies **within 2 ns** ($\sigma_{pr} \cong$ 260 ps**)**
- added in quadrature time zero jitter (σ_{t0}= 250 ps) + front-end resolution (σ_{FE}= 150 ps)

$$\sigma = \sqrt{\sigma_{pr}^2 + \sigma_{t0}^2 + \sigma_{FE}^2} \approx \text{ 400 ps}$$

- from cumulative distribution 99% of particles included with a shutter window of 5 ns (from 5.5 ns to 10.5 ns → **50% DCR data reduction**)



Full simulation in progress:

→ we don't expect a large spread added by photon emission + propagation (confirmed already by simulation)

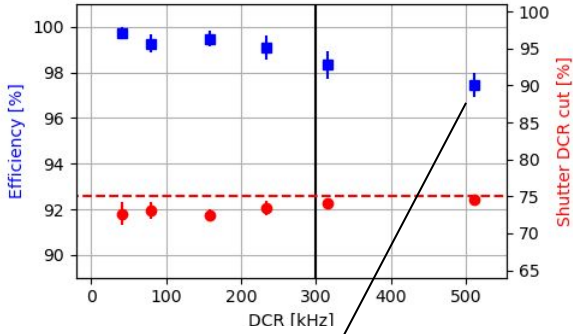
→ impact of time slewing effect to be assessed (could impact with the need of 2 ns additional window – see slide 9)

ALCOR digital

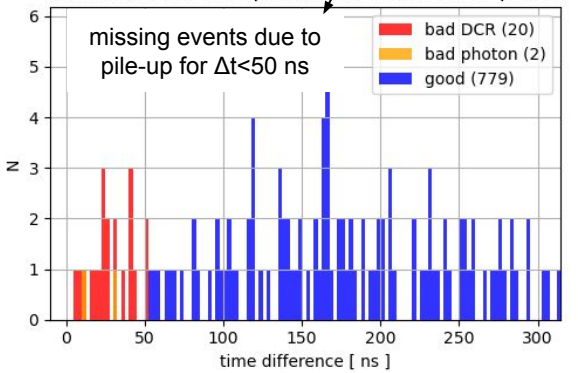
ALCOR shutter simulations

Shutter: periodic test-pulse
width = 2.5 ns, period = 10 ns → R.F. = 4

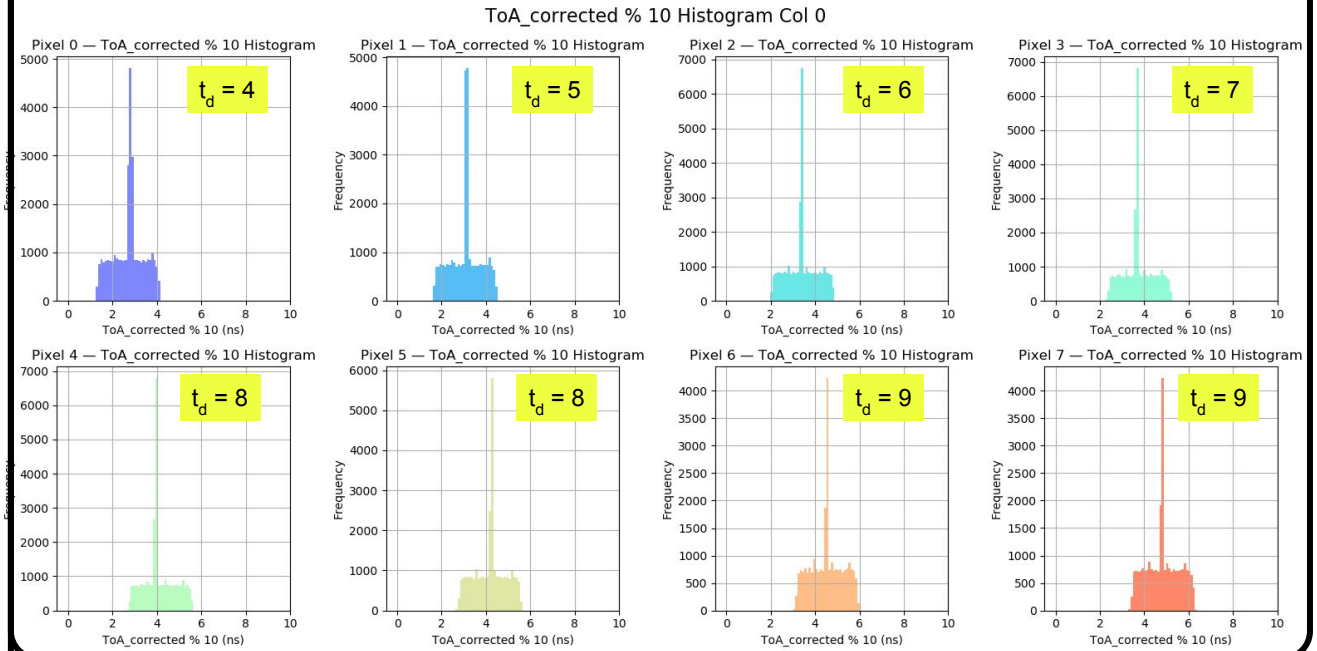
Single-channel mixed-signal sim (including FE time-walk and pile-up effects)



Time difference w.r.t. previous dark-count/real-photon



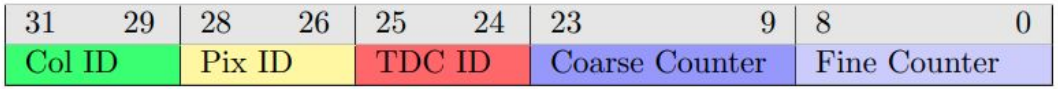
Full-chip digital sim (ideal case) to verify shutter distribution for the whole ALCOR chip: use in-pixel programmable delay chain (4 bits, LSB ≈ 350 ps) to center shutter window for each pixel/column



➔ **FE** (jitter, time-walk, pile-up) and **physics** (real photon signals distribution) contributions **not included in this simulation**

ALCOR v3 - digital interface

- Clock frequency: **394.1 MHz** (4x EIC clock: 98.52525 MHz)
- **8 LVDS Tx links**: one for each column, DDR output at **788 Mb/s**
- Data format
  - **32-bit words** with **8b/10b encoding** (2x event words in ToT/SR mode)
  - Frames with *header* + *data* + *trailer*
  - Frame duration set by *coarse counter roll-over* or *New Orbit reset*



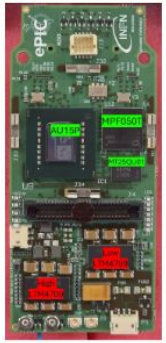
FIFO position	Data (32-bit word)
1	K28.0 (Frame header)
2	Frame number
3 + …	Event words Column X
n	K28.2 (Frame trailer)
n+1	*K28.3 (Status header)*
n+2	*Status words Column X (8x)*
n+10	End of Column status word
n+11	K28.4 (Checksum header)
n+12	CRC value

- External **reset** with 3 different features depending on signal width:
  - 24-31 xCLK: ***Hard Reset***
  - 16-23 xCLK: ***Start*** (Frame Counter = 0 and Coarse Counter = 0)
  - 8-15 xCLK: ***New Orbit*** (Frame Counter +1 and Coarse Counter = 0) → forces a *rollover* condition (ALCOR rollover = 2^{15} clk cycles ≈ 83 μs, EIC orbit period ≈ 12.8 us)
- **Test Pulse**: analogue FE injection and TDC calibration; also used for **shutter** signal
- **SPI** interface for registers configuration

dRICH DAQ building blocks

INFN-TO

- ALCOR-64 design/validation
- FEB design/production
- packaging / test
- radiation tests

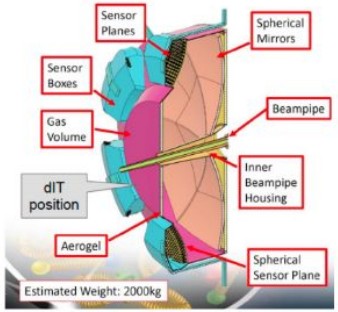


INFN-BO

- RDO design/validation
- RDO design/production
- Test Bench RDO
- RDO – DAM link over VTRx+
- radiation tests

INFN-RM

- DAM “DAQ” firmware
- ML algorithms → neural networks
- RDO – DAM communication
- DAM – GTU communication



INFN-GE

- dIT design/simulation
- dIT test (scint. fibers)
- dIT → validation
- dIT → construction
- dIT to DAM (or to GTU)

Towards full data-push architecture: time ordering

Studies on ALCOR datastream format to understand if we need to optimize data (at RDO level) to help DAM processing (ML algorithms)

ALCOR timestamps are not "immediately" out

- Data from pixels is made available for transmission at TDC *End of Conversion*
- This can introduce some **time-inversion in ALCOR datastream**: hits with longer conversion time are transmitted after hits with shorter conversion time

Pixel TDC conversion defines time required for digitization:

- TDC max conversion time = 1.5 x 128 = 192 clock cycles ≃ 500 ns
- TDC min conversion time = 0.5 x 128 = 64 clock cycles ≃ 170 ns
- Max ΔT = 500 ns - 170 ns = 330 ns (inside ALCOR channel) → down to the column and transmit off-chip

ALCOR data transmission:

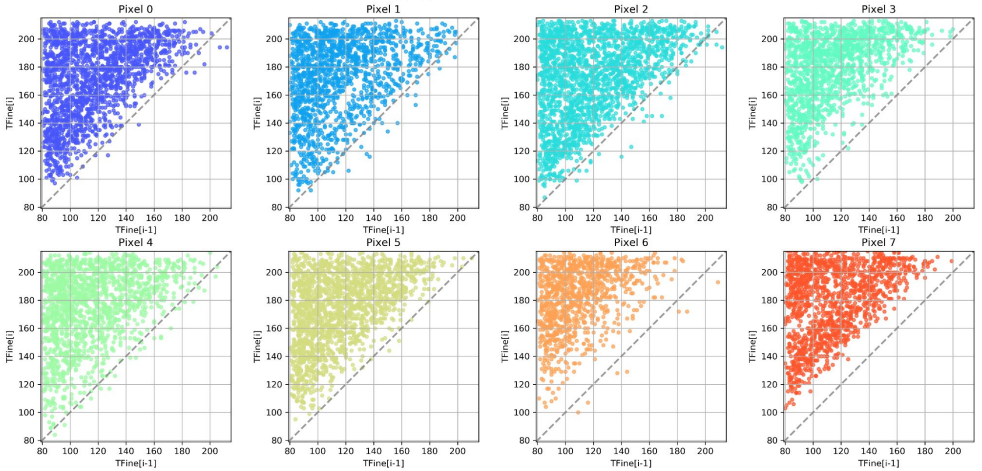
- 1 word: 40 bits → 40 b / 788 Mb/s = 51 ns per event word (we have 8 channels for each Tx link)
- If no other hits in the column, 2 hits (separated by 128 clk cycles in the pixel) are only separated by idle words (K.28.5 "comma" are filtered by RDO)
- Time reference given by ALCOR frame structure → 1 frame for each EIC orbit (12.7886 μs)
- @DCR = 300 kHz/ch → Δt_{frame} = 0.92 * 12.7886 μs → $N_{events} = 8 \cdot DCR \cdot \Delta t_{frame} = 28.3$
- We can expect ~30 event words per frame (no shutter, mean value, 2x in ToT/SR mode, add physics)

ALCOR data time ordering

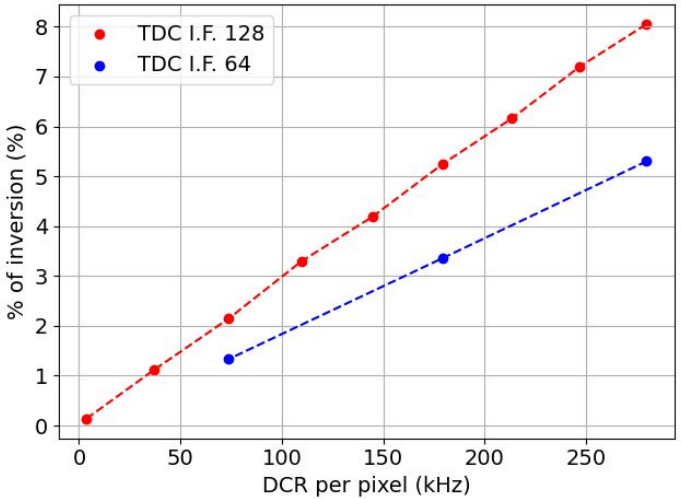
Simulations to study **ALCOR datastream time-order**

- Select data with time inversion: $t_i < t_{i-1}$
- Compare TDC output codes: T_{fine} = conversion time
- Most of **time-inverted data are due to TDC longer conversion time**
- Remaining time-inverted data due to **pixel readout priority along the column**

TDC output for events with timestamp[i] < timestamp[i-1]



Data time-inversion rate



- The inversion rate **increases linearly with DCR**
- Simulations with **TDC interpolation factor (IF) 64 show a lower inversion rate** thanks to TDC lower conversion time
- **Max inversion time ≃ 64 or 128 clk cycles** (according to IF)
- Simulations done with shutter width: 7.5 ns (reduction factor = 1.33)

ALCOR Simulation and Time Ordering: C. Ferrero @dRICH General Meeting on DAQ (25.03.2026)

dRICH data words

DISCLAIMER NOTICE: all this is VERY 

RDO "prepares" data reduction
DAM "does" data reduction

RDO to optimize ALCOR words data format to help DAM processing

- ALCOR event words are **time ordered** inside RDO: buffer events up to 256 CLK cycles inside FPGA
- 2 ALCOR event words (ToT/SR mode) are **merged** by RDO to reduce data throughput and build a full event word

AWORD

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

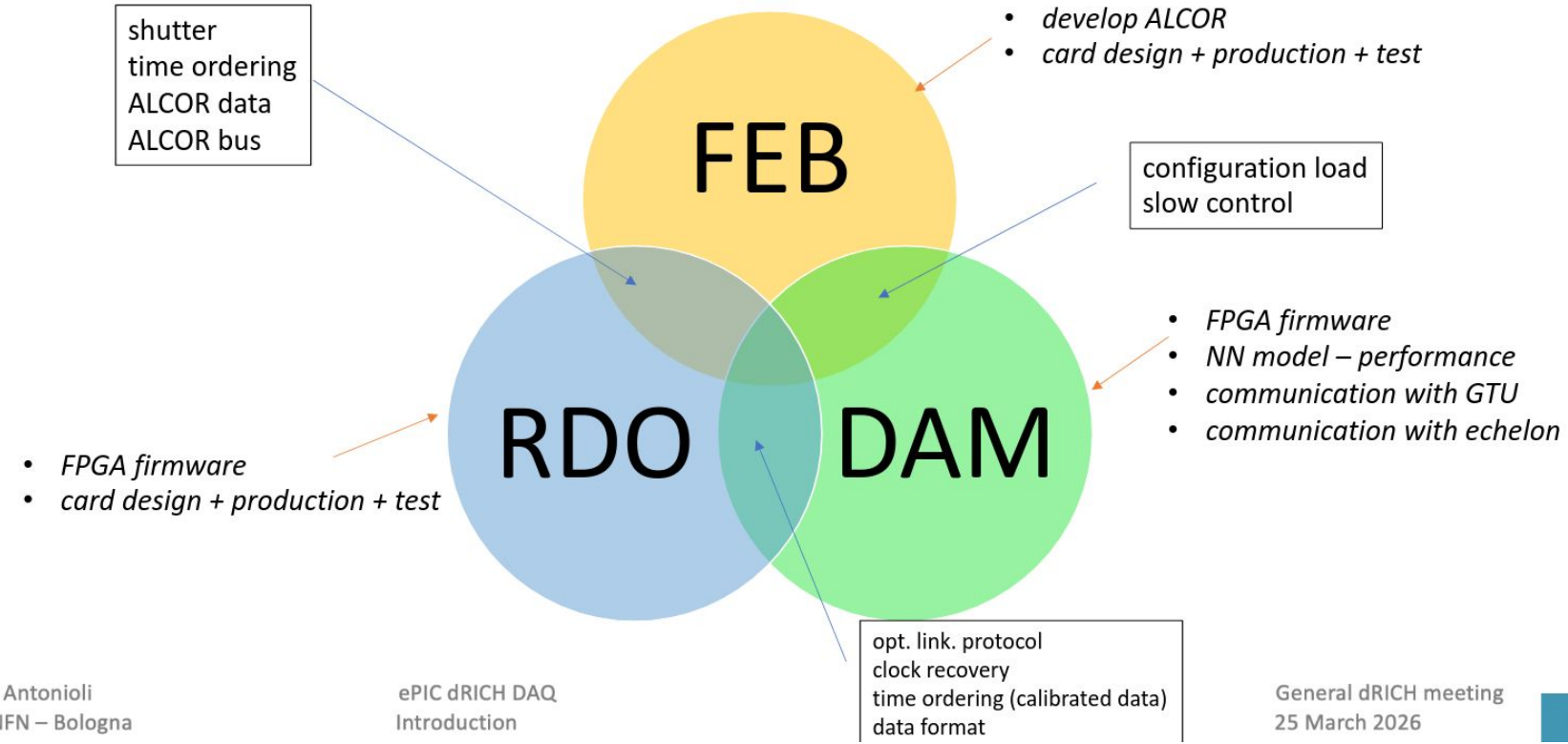
63	62 50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
0	RDO ID	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Column ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

LEADING TIMESTAMP
TRAILING (OR SLEW RATE) TIMESTAMP
dRICH CHANNEL ID
CONTROL

ePIC dRICH DAQ: P. Antonioli @dRICH General Meeting on DAQ (25.03.2026)
Update on the firmware design for the dRICH-RDO card: S. Geminiani @dRICH General Meeting on DAQ (25.03.2026)

dRICH DAQ Working Group

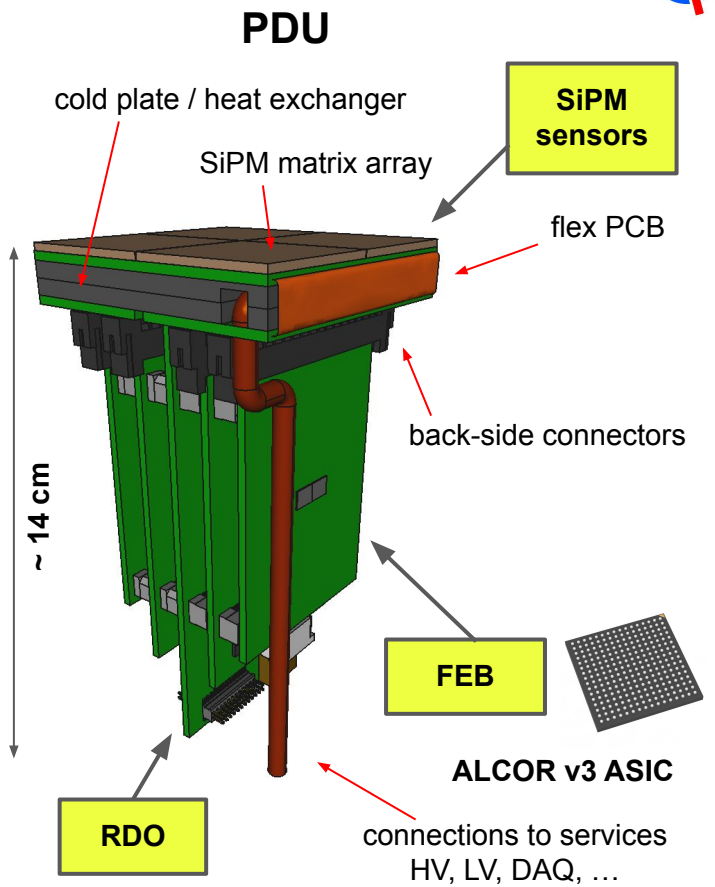
DAQ WG: INFN BO + INFN RM + INFN TO / meeting every 2 weeks / mailing list available to subscribe



dRICH ALCOR FEB

- **4 FEBs** in each PDU (**256** readout **channels**), managed by **1 RDO** (INFN Bologna)
- 2 slightly different versions, they share the ALCOR BUS connector (interface with RDO):
  - ***Master***: internal FEB
  - ***Slave***: external FEB
- FEB designed by INFN Torino, close cooperation with Bologna-Ferrara colleagues to match *RDO design, SiPMs requirements* and *space constraints*
- Design of dRICH electronics (SiPM carrier, ALCOR, FEB, RDO, PDU, detector box, LV/HV services) all done by INFN (BO-FE-TO) → **weekly meetings to keep close cooperation**

✓ **FEB design completed on May 2025**



ALCOR FEB

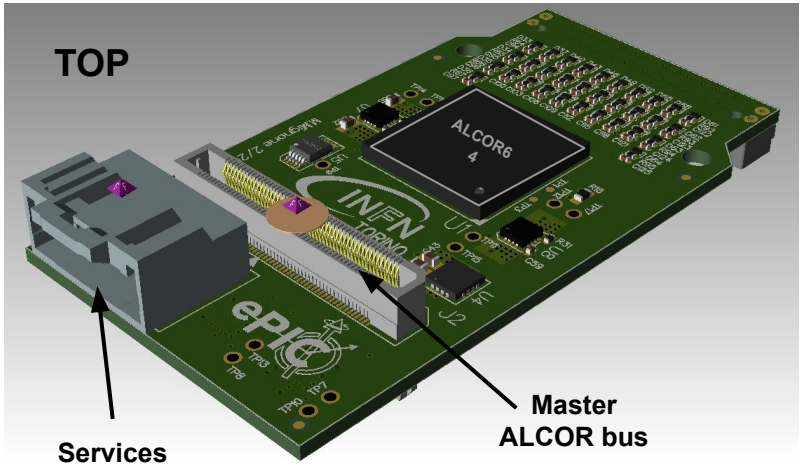
Connectors:

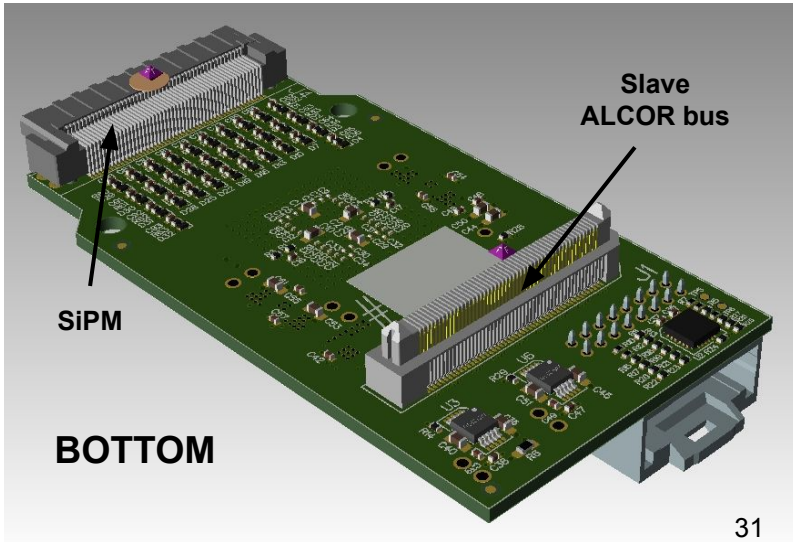
- **Master ALCOR bus** (between RDO and 1st FEB, LVDS signals): *Samtec ERM5-050-04.0-L-DV-TR*
- **Slave ALCOR bus** (between 1st and 2nd FEB, LVDS signals): *Samtec ERF5-050-05.0-L-DV-K-TR*
- **Services connector** (SiPM $V_{bias/annealing}$, ALCOR LV, SiPM NTC sensor, 16 pins, max 2 A each): *Molex 2086591640*
- **SiPM connector** (SiPM signals, V_{bias} and $V_{annealing}$): *Samtec LSHM-150-01-L-RH-A-N-K-TR*

➢ Dedicated PCB section for SiPMs HV routing

- 2 $V_{bias/annealing}$ PCB layers/sections, each serving 32 SiPMs
- **SiPM online annealing**: forward-bias, **I=60-100 mA** to reach **T=150°C** on SiPM matrix board
- FEB to support **T up to 100°C**

- Material: **I-Tera MT40**
- N layers: **10**





ALCOR FEB

Main components:

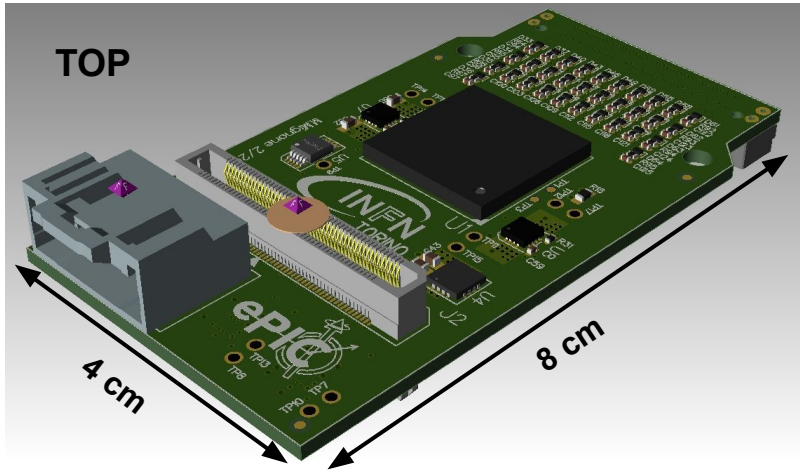
- **Linear Regulators** (2.5 V DVDD_IO, 1.2 V DVDD, 1.2 V AVDD): *Analog Devices ADP1752ACPZ-2.5-R7, ADP1761ACPZ-R7* (V_{in} = 1.4 V and 2.7 V)
- **Current monitors** (before regulators): *Microchip Technology MIC2040-1YMM-TR*
- **I2C to Parallel-Port Expander** (RDO can read/control regulators and current monitors): *Texas Instruments PCF8575RGER*
- **RC high pass filter** (AC-coupling between SiPMs and ALCOR) + **annealing circuitry** (diodes)

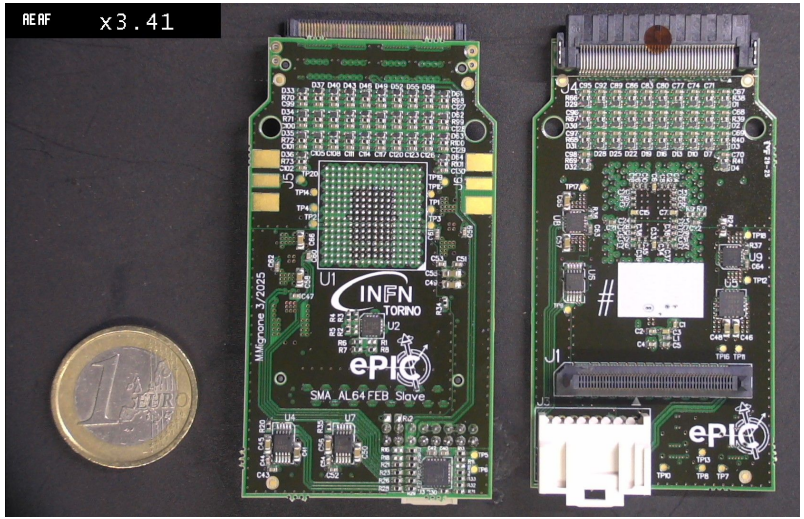
Power segmentation:

- LV: 64 channels
- HV: 32 channels

First FEB samples received on Nov 2025

2 extra SMA debug outputs to probe 2 SiPM channels without ALCOR and test annealing procedure





ALCOR BGA package

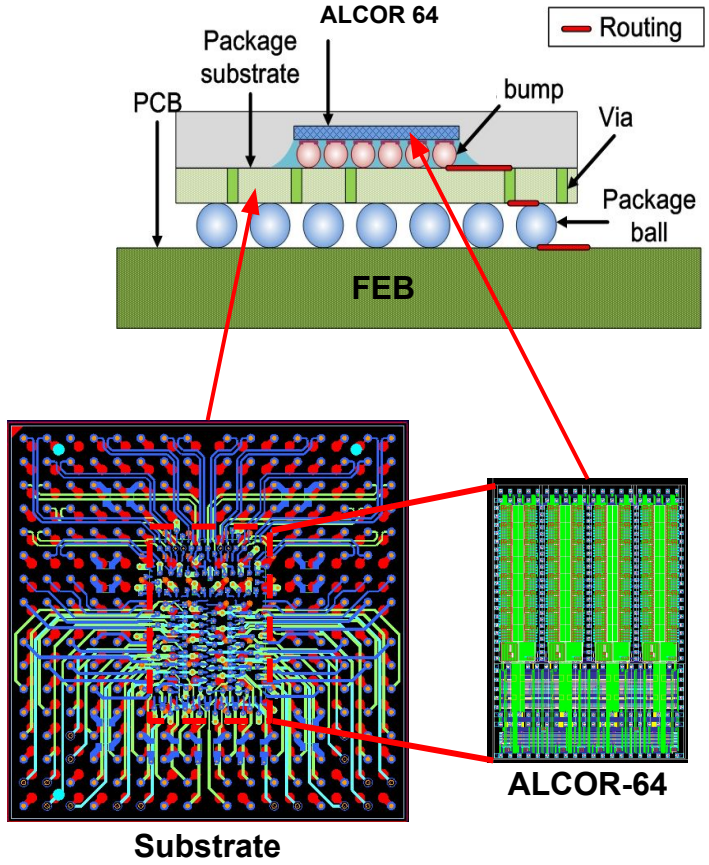
ALCOR-64 → **flip-chip BGA package**

ALCOR-64 fabricated using MPW run:

- Tape-out on Apr 2025
- 60 singulated dies received in Sep 2025, no full wafers
- Some processes for packaging more difficult on single dies

ALCOR-64 packaging managed by vendor located in Singapore providing all services (via different subcontractors):

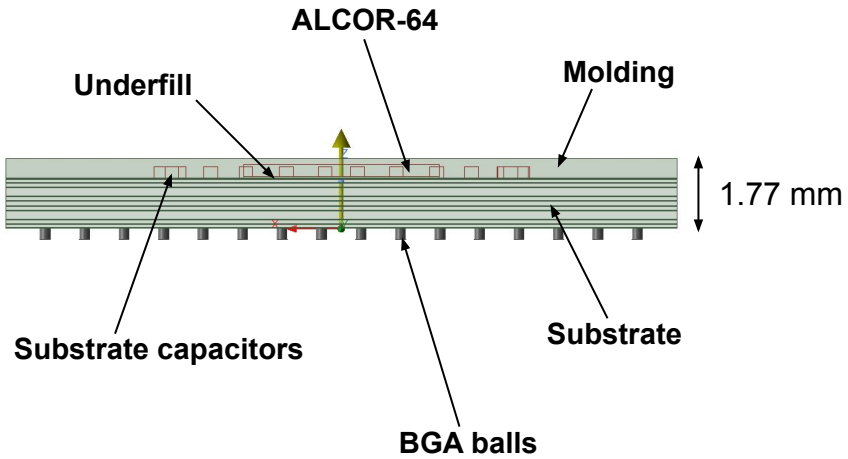
1. **Substrates** production and bumping (substrate design was done by INFN Torino)
2. **UBM** (under-bump metalization) on ALCOR dies
3. **Package assembly**: flip-chip die attach, underfill, molding, balling, etc…

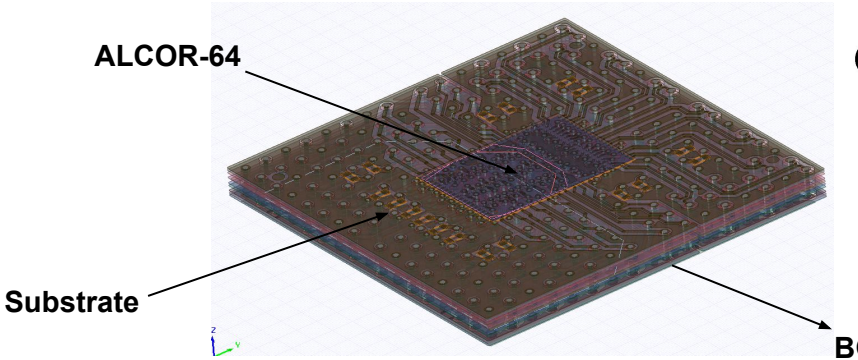


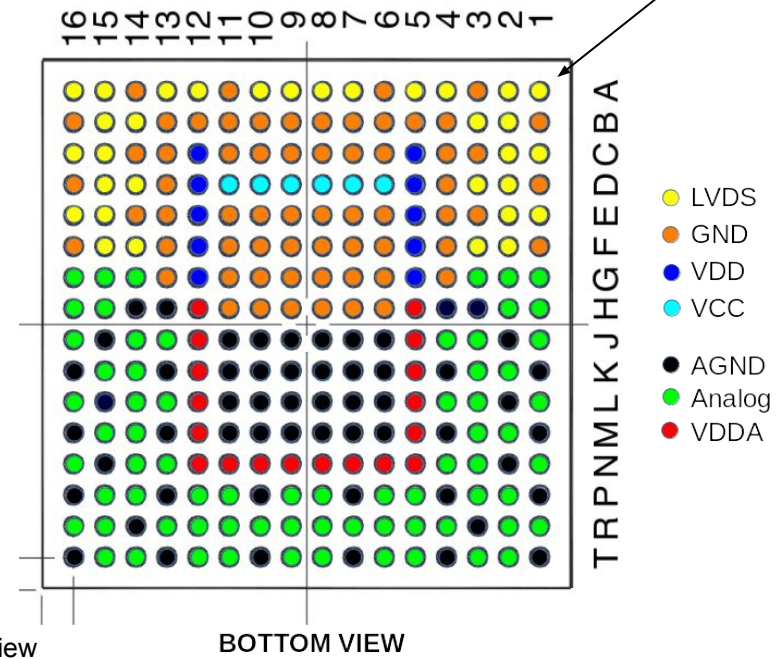
ALCOR BGA package

FC-BGA: flip-chip ball grid array

- BGA 256 (16 x 16)
- Size: 17 mm x 17 mm
- Ball pitch: 1 mm

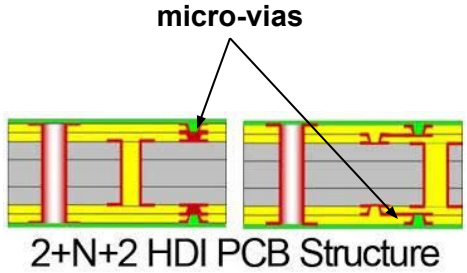


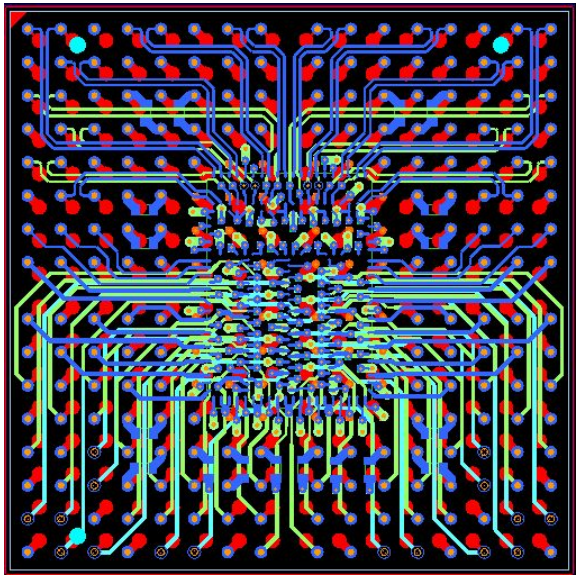


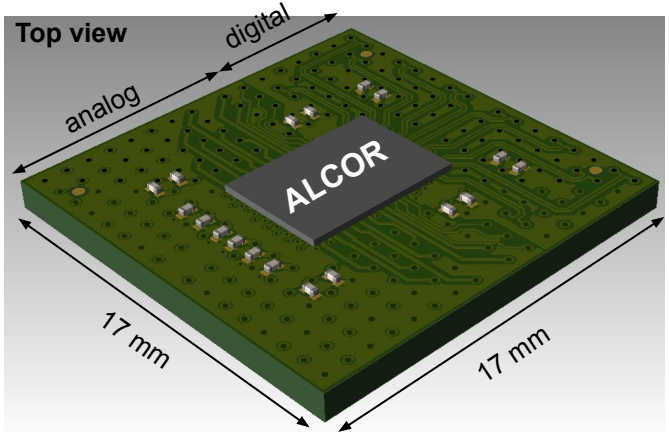


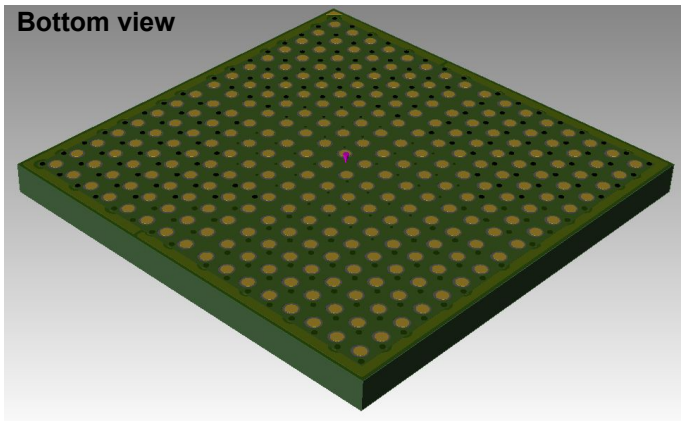
ALCOR substrate

- BGA 256 Ball 17x17mm 1mm-pitch
- BT-Epoxy
- 10 Layers (2+N+2)
- Thickness: 1.27 mm
- Decoupling capacitors (0201)
- Design completed on Jan 2025
- Verification: electrical and thermal simulations

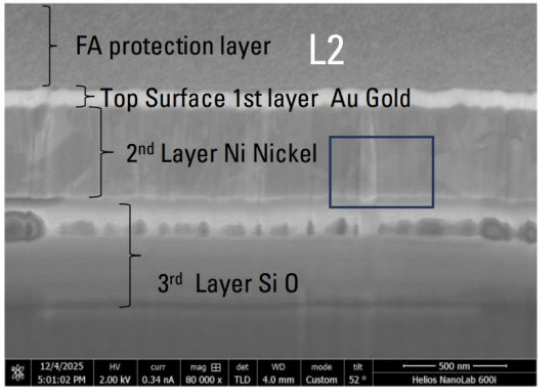






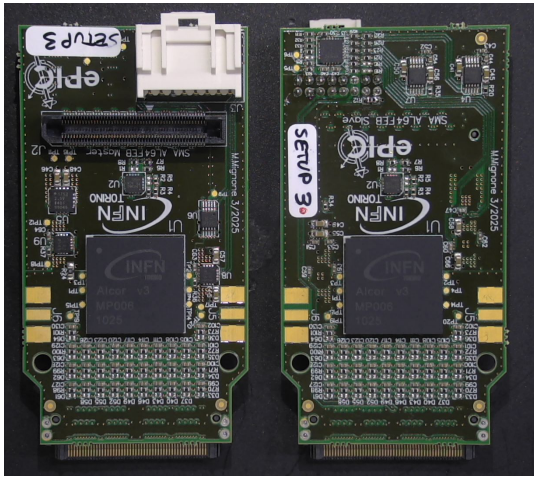


ALCOR-64 packaging status



Nov 2025: 1st Run flip-chip die attach failed due to solder overflow causing short circuits between bump pads

- **FIB dissection + SEM-EDX analysis** (Dec 2025) on one die showed that **UBM layers extend beyond the bump pads**, covering additional areas of the chip surface above the passivation layer
- This metalization **creates a wetting surface** that facilitates solder migration from the substrate-side bumps to the die, leading to **short circuits between adjacent pads**
- UBM process managed by packaging vendor (via different subcontractor)



Jan 2026: packaging vendor confirmed issue on **UBM** and proposed a **recovery solution** (*gold stud bump)* to reduce/avoid solder overflow:

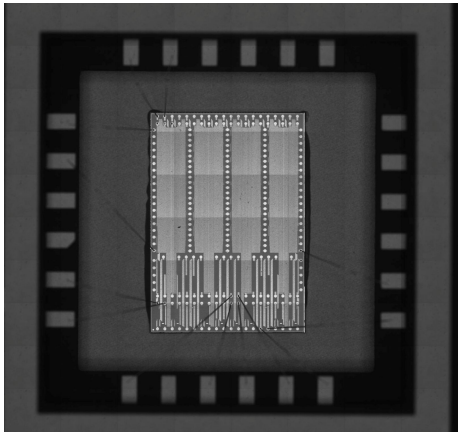
- Completed packaging on 4 ALCOR dies using recovery solution
- BGA devices received in February and assembled on 4 ALCOR FEBs

Mar 2026: Critical issues on all 4 tested devices: many short-circuits and some open-circuit on ALCOR pins

- Short-circuit pins correspond to adjacent bump pads on the chip, this spatial correlation strongly support the hypothesis that the UBM metallization between pads facilitates solder overflow, creating bridges during the reflow process

ALCOR-64 packaging status

Apr 2026: **impedance measurements**, probing directly on the bump pads of the remaining bare dies in Singapore



- Check if open/short circuits are already present before the assembly process
- **Tested dies already underwent the UBM process** (we do not have any untouched dies w/o UBM)
- **Shorts already present**

If situation is not recoverable we need to define the necessary corrective actions and next steps:

- Started discussions for a **new MPW run** and **alternatives for UBM process** → next slide
- This issue introduces an important **delay** in our **schedule** → next slides

ALCOR-64 packaging status

Alternatives for **UBM process** and **new MPW run**

- IMEC informed us that **new Flip-Chip TLR** has been introduced by the foundry this year
  - ✓ Possibility to implement an RDL directly on ALCOR
  - ✓ Simplify BGA substrate and flip-chip assembly → improved reliability and yield
  - ✗ If new pad geometry is required to meet RDL or UBM design rules (checks ongoing), there will be new NRE costs for substrates (also *new substrate design*) and assembly → ongoing discussions with packaging vendor and within the INFN dRICH group
- IMEC informed us that foundry might be able to support Lead-Free **bumping** on our design
  - UBM + bumping
  - Information still very partial, **to be confirmed** → more infos from foundry and IMEC expected this week: Flip Chip (Pilot vs MPW, costs, lead times, in-house/OSAT)
- Timeline: UMC MPW runs on **July 10th** and **September 11th**

ALCOR Tentative Timeline

- **FEB** and **ALCOR** are part of **INFN IKC**
- The whole production batch will be delivered in Italy for QA and integration

ALCOR-64 new MPW run

- Fabrication: Q3-Q4 2026
- Packaging: Q1-Q2 2027
- Testing: Q2-Q4 2027

ALCOR-64 production

- Fabrication (18 wafers): Q1-Q2 2028
- Packaging: Q3-Q4 2028
- Testing and FEB assembly: Q4 2028 - 2029

DISCLAIMER NOTICE: Timeline is **PRELIMINARY** and needs to be **discussed within the dRICH Project**

- ➢ **Dedicated meeting in Torino next week** discuss about updated schedule (how to fit this delay inside our project timeline) and how to cover extra costs for new MPW
- ➢ **Expected iteration with INFN referees following Torino meeting**

➔ PDU modules and detector boxes assembly: 2029-31

➔ Contingency time exhausted due to ASIC delay, but still on schedule

➔ Fully assembled detector boxes will be shipped to BNL to arrive ~1 yr before installation (Oct '32)

ALCOR QA/QC

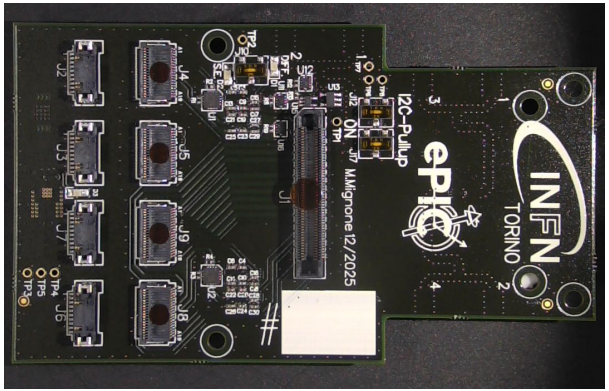
QA is organized to allow essential acceptance tests on 100% of components plus in-depth sample characterization (1-2%)

- **Acceptance tests**: power-on, current absorption, configuration, data alignment, TDC scan, Vth scan
- **In-depth sample characterization**: SiPM DCR scan, laser measurements (jitter, shutter)
- FEB adapter card has been developed to test FEB standalone (also without RDO) → next slide
- Different options are currently being evaluated: **in-house testing** (parallel QA stations in different INFN sections) or **external company** (previous experience for the CMS ECAL HL-LHC upgrade ASIC: 80k LiTE-DTU chips successfully tested by Microtest)
  - N. FEBs: 4992 → N. ALCOR: 4992 (increase number to include production phase risk mitigation)
  - 7000 ALCOR → 85% yield → 5950 ALCOR
  - Testing time: 8 min. → 50 ASIC per day → 250 ASIC per week
  - 7000 / 250 = 28 weeks → parallel setups to reduce overall test time (or external company)
- After **ALCOR/FEB validation**, FEB will be moved to **PDU assembly line**: FE electronics tested again after being integrated inside PDU (4 FEBs + 1 RDO + SiPM matrices)

ALCOR QA/QC

Adapter board to **read 2 FEBs using commercial FPGA**:

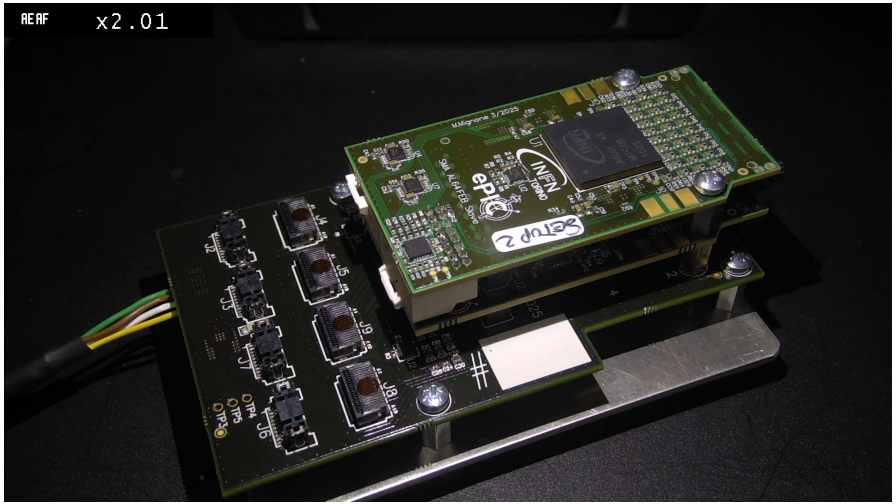
- ALCOR BUS connector: interface towards **1 Master FEB** and **1 Slave FEB**
- FEBs need also I2C power (2.5 V) and control signals (from ALCOR BUS)
- FireFly connectors: **4 FireFly** towards commercial FPGA to support readout up to 2 FEBs



➢ This setup allows **testing 2 FEBs in parallel**, thus reducing total test time for **mass production QA**

➢ 4 boards received on Mar 2026

➢ Now starting design of **socket test-board**



Summary

- ALCOR is a **64-channel mixed-signal ASIC** adopted for the readout of the **SiPM sensors** for the **ePIC dRICH** detector
- **ALCOR-32** has been extensively used within the dRICH Collaboration in the last 5 years: several laboratory and beam tests demonstrated the ALCOR-based readout capability to measure single photons with good time resolution and rate capability
- **ALCOR-64** includes all features and specifications required for the ePIC dRICH:
  - 64 channels, BGA package, shutter, 394.08 MHz clock frequency
  - **Packaging issues** introduce an important delay in our schedule
  - Discussions ongoing to find alternative UBM process and preparation for new MPW run
- dRICH **ALCOR FEB** and **QA/QC test-boards**:
  - First FEB samples received on Nov 2025
  - Annealing and temperature tests can be performed also without ALCOR-64
  - FEB adapter card to test FEBs standalone has been developed and produced
  - Design of socket test-board to be started soon

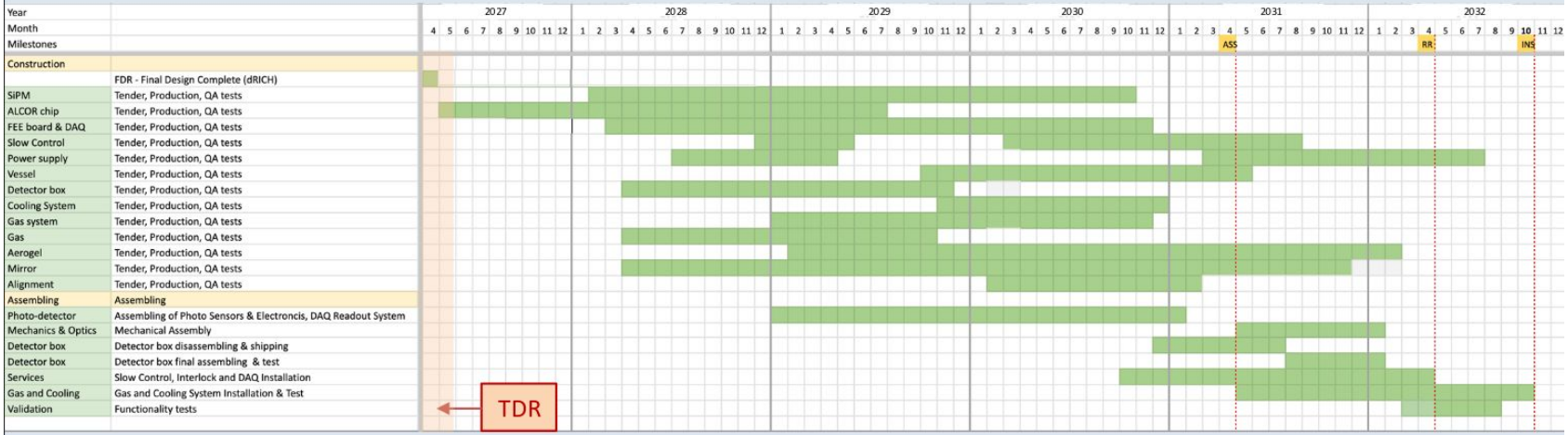
Backup Slides

Construction Plan

A construction and QA plan is outlined accounting for lead, assembling and commissioning time

Details on Backup 31-32

Recomm. (DAC): Present at least a vague timeline for the project at the next DAC review.



CD-2: Validate ALCOR-64, RDO design
Validate real-scale prototype mechanics
Study detector box engineering
Define baseline integration and maintenance plan
Work out a baseline cooling & gas sytem

CD-3: Optimize component performance
Complete component integration
Finalize cooling & gas system
Detail detector integration and maintenance

Stage 1: Procurement for the PDU components (asics, SiPM, carrier, FEB, RDO…)
Anticipate mirror and gas procurement to reduce risk

Stage 2 : Central 2-3 year for the detector box assembling before delivery to BNL
Aerogel production after engineering optimization
Gas system after BNL authority approval

Stage 3: Mechanical structures
Assembling and completion of services
6 months of contingency and functionality tests

Timeline is based of following assumptions:
- CD2 is at summer 2026 (last quarter of FY26)
- CD3 is at the end of 2027 (first quarter of FY28)
- dRICH installation is on Oct 2032

Summary of ALCOR specs for the dRICH detector

Function	Digitization from SiPMs with 1 p.e. sensitivity
Mode	Single-photon tagging or time and charge
Tech Node	110 nm CMOS
Channels	64 (8x8), dual polarity
Cdin	<1 nF
Digitization	20-40 ps TDCs, ToA + ToT; Timing < 150 ps
Shutter	Width: 2 - 3 ns, programmable latency
Input Rate	<2.4 MHz (up to 5 MHz on single channel)
Clock	394.08 MHz operation from BX 98.52 MHz
Links	788 Mbps LVDS, SPI configuration
Power	12 mW/ch
Package	BGA
Rad Tolerance	Radiation hard

→ 788 Mbps / (40 bits * 8 pixels) = 2.4 MHz
(assuming no extra control words)

Summary of key differences between ALCOR versions

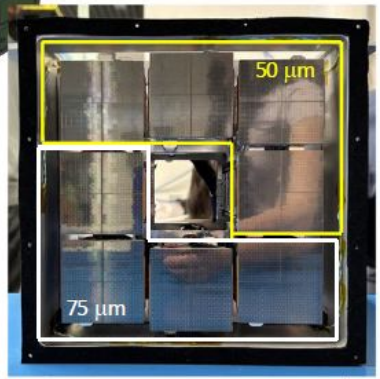
	ALCOR-32	**ALCOR-64**
Channels	32	64
Die size	4.95 x 3.78 mm^2	4.95 x 7.02 mm^2
Assembly	Wire-bonded on PCB	FC-BGA package
Clock frequency	320 MHz	394.08 MHz
Time resolution	< 200 ps	< 150 ps
Shutter	synchronous, width > 100 ns	asynchronous, width > 2 ns
SEU protection	only pixels	pixels + EoC
Dataframe duration	2^{15} clock cycles	2^{15} clock cycles or user defined
Power consumption	10 mW/ch	12 mW/ch

towards construction

2022
electronics v1

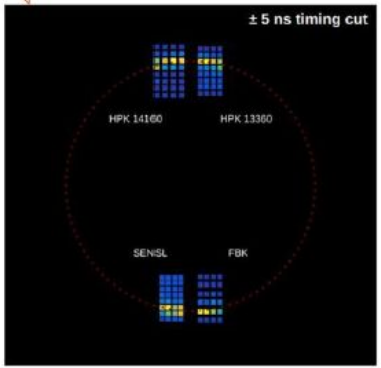
2023
electronics v2

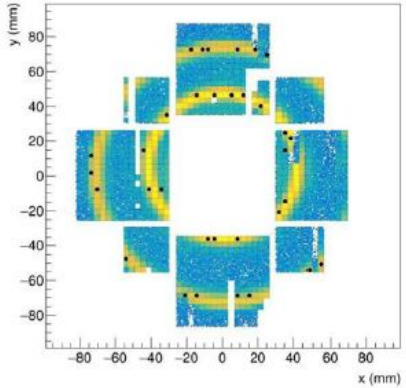
2024
electronics v2.1

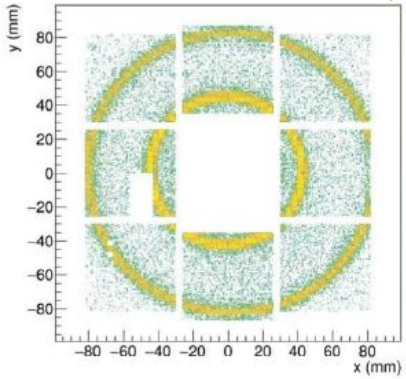


2025/26
electronics v3

ALCOR 32 ch







Full size engineering test article

2025 + SiPM carrierv3 + RDO

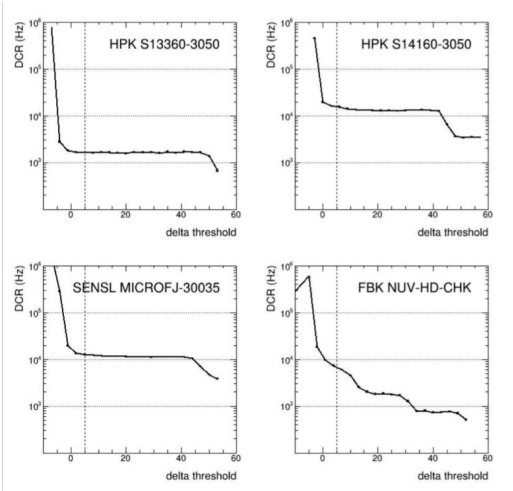
2026 + ALCOR 64ch + FEB 64

ALCOR v1

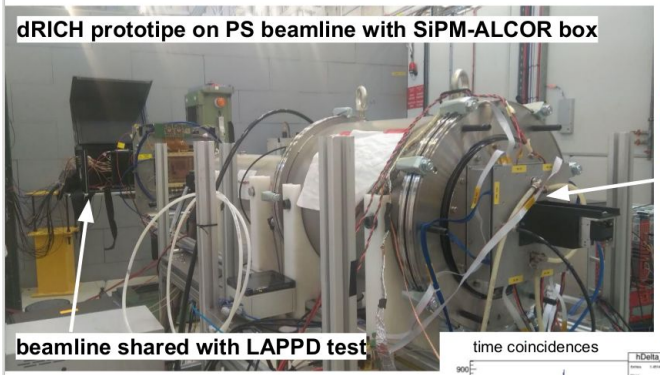
Developed by INFN for the readout of SiPMs at 77K, in the framework of Darkside (Dec 2019)

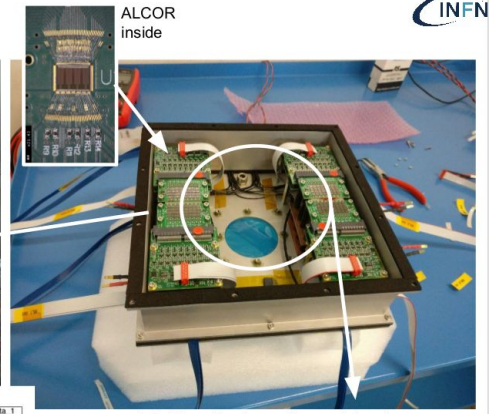
- Pixel matrix layout to explore solutions towards the development of an active silicon interposer for the integration of large area SiPMs for future massive frontier LAr Dark Matter Experiments

Extensively used within the EIC dRICH Collaboration during 2021-2022

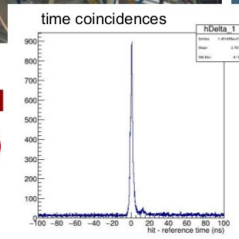


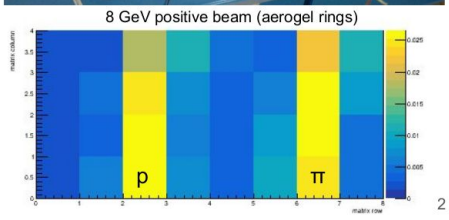
2022 test beam at CERN-PS





successful operation of SiPM
irradiated (with protons up to 10^{10})
and annealed (in oven at 150 C)





ALCOR v2

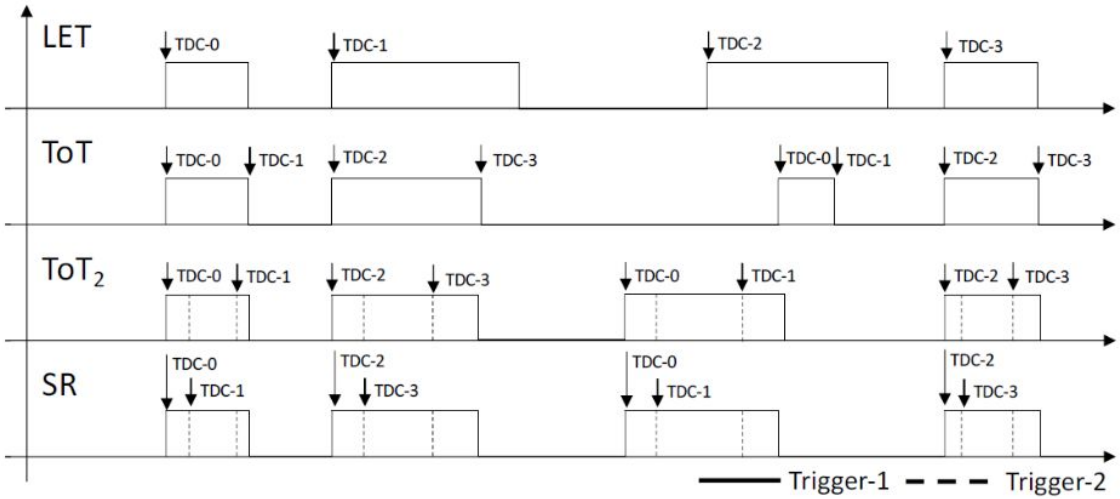
ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in **June 2023**
- First version developed for ePIC, includes new features targeted for EIC dRICH and bug fixes:
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for single photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polarity
- Successfully validated in **2023 beam test**: 20 FE-DUAL (40 ALCOR v2.0, **1280 channels**)

ALCOR v2.1

- INFN internal engineering run, chips received in **Jan 2024**
- Version currently used, includes small bug fixes w.r.t. ALCOR v2
- Very high number of chips available to increase instrumented area for dRICH prototype and assemble other test setups
- Successfully validated in **2024 beam test**: 32 FE-DUAL (64 ALCOR v2.1, **2048 channels**)

ALCOR pixel operating modes



4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

Each mode can be set to:

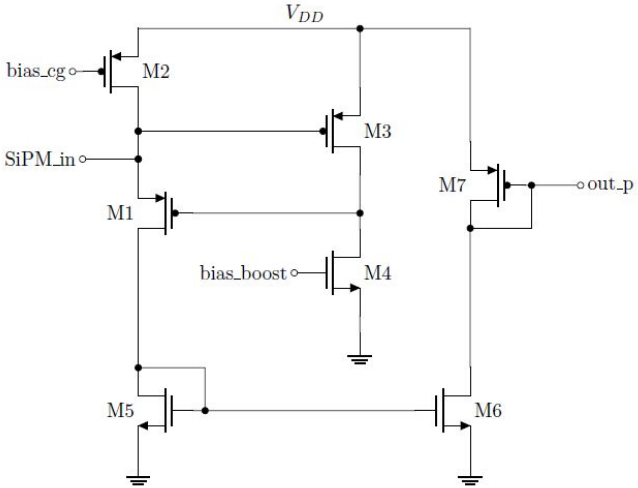
- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

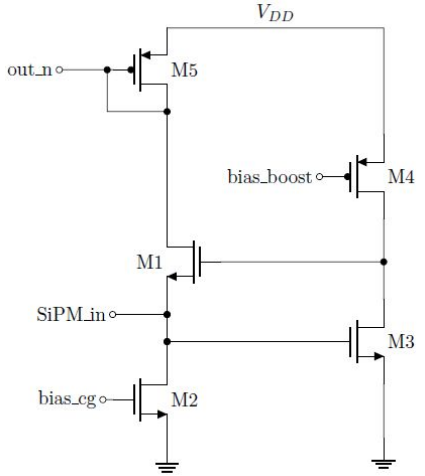
Each pixel can also be disabled

ALCOR Front-End

Input stage

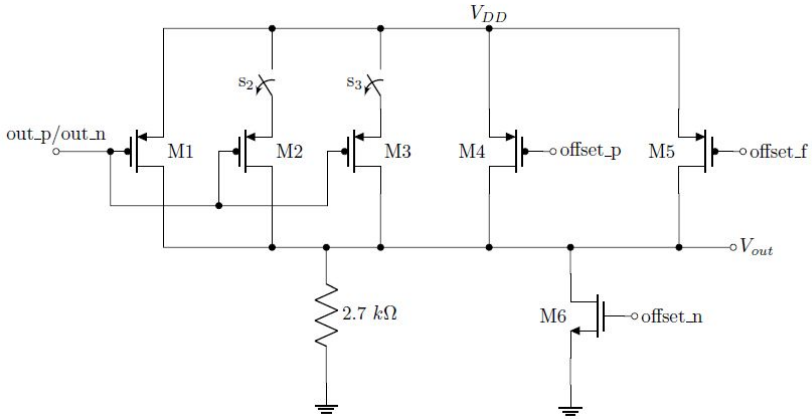
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω





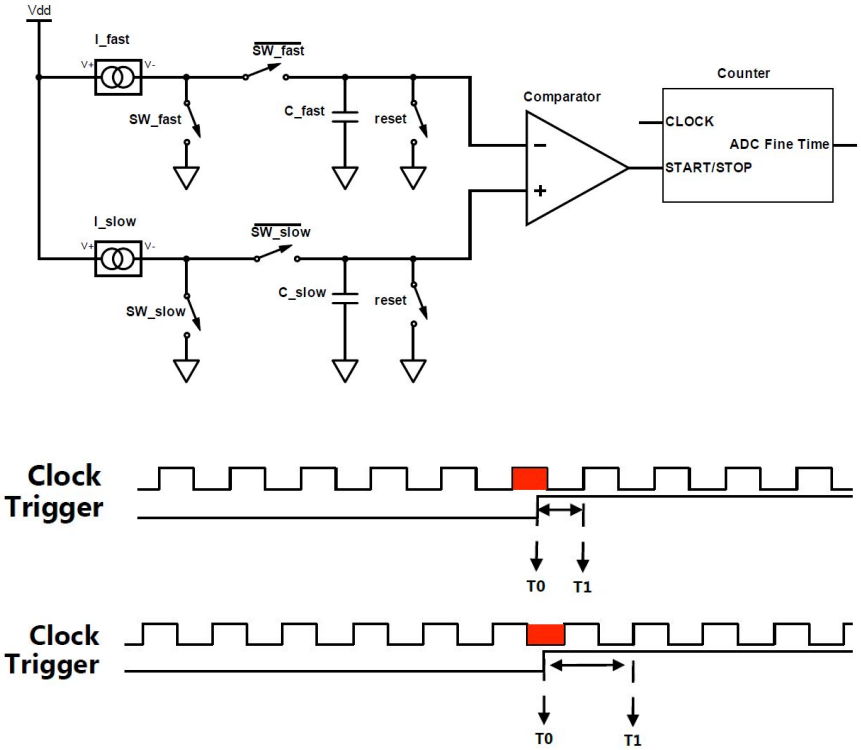
Output stage

- TIA gain: 2.7 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)



Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Time conversion performed by **TDC** based on **analogue interpolation** (9-bit fine time):
  - ***fast ramp***: constant current to charge C_{fast} → measure phase between event trigger and clock
  - ***slow ramp***: smaller constant current to charge C_{slow} → counts clock cycles until C_{slow} and C_{fast} are equal
- I.F. 64 or 128 → LSB = 20-40 ps @394 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [160, 500] ns
- 4 TDCs per pixel for **event derandomization**



Power consumption

Estimated power consumption: **< 1.2 W/chip**

ALCOR requires 3 different power supplies

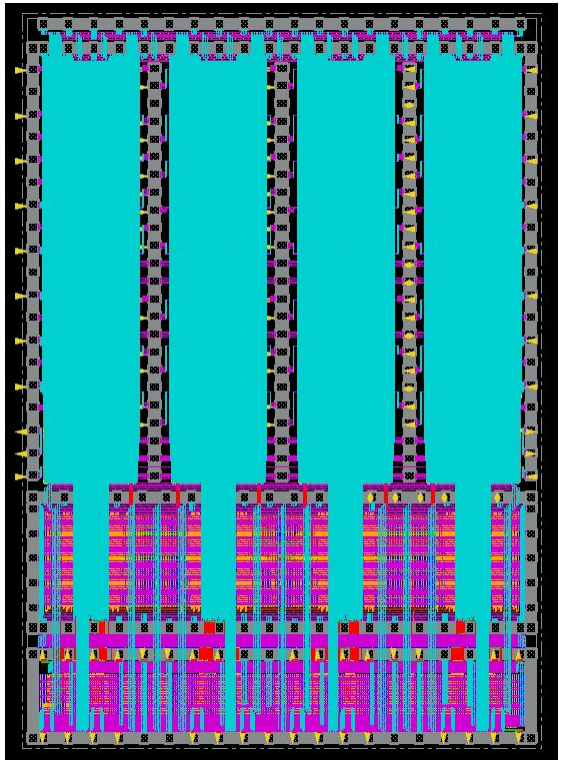
- **AVDD**: **1.2 V** analogue core (480 mW)
- **DVDD**: **1.2 V** digital core (330 mW)
- **DVDDIO**: **2.5 V** digital IOs (170 mW)

Generated on the FEB using LDO linear regulators (V_{in} = **1.4 V** and **2.7 V**)

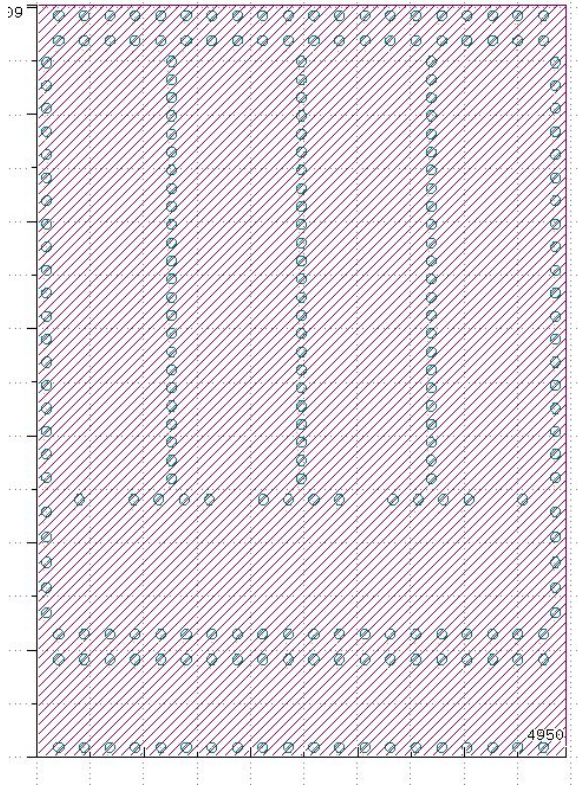
ALCOR v3

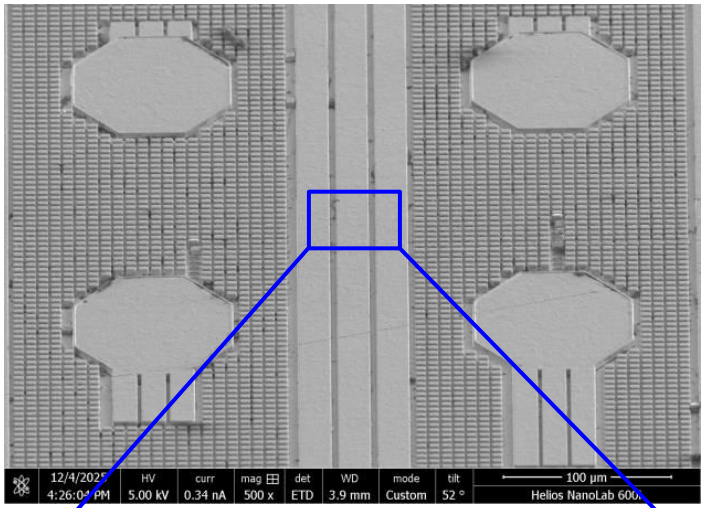
- ALCOR-64:
  - 7.02mm x 4.95mm
  - 234 PADs
- No dedicated redistribution layer (**RDL**) available in UMC 110nm technology
  - ASIC bump pads geometry not uniform
  - fan-out to BGA balls done on the interposer/substrate
- Bump pads pitch:
  - ~170 µm (analog inputs)
  - ~215 µm

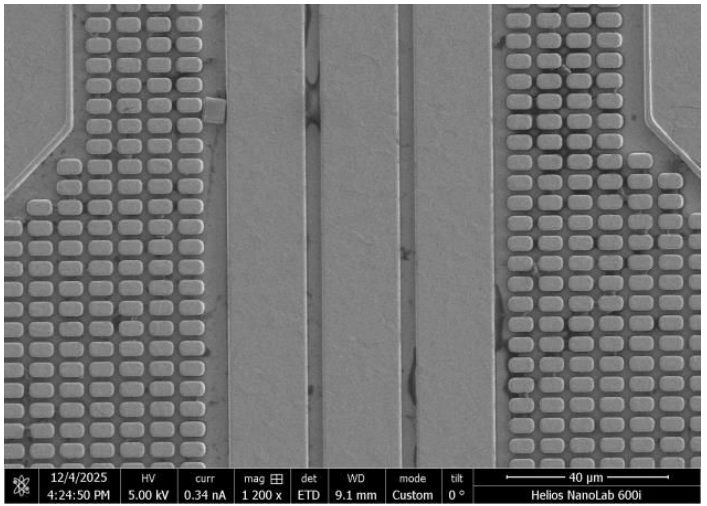
ALCOR-64 top layout



ALCOR-64 bump pads

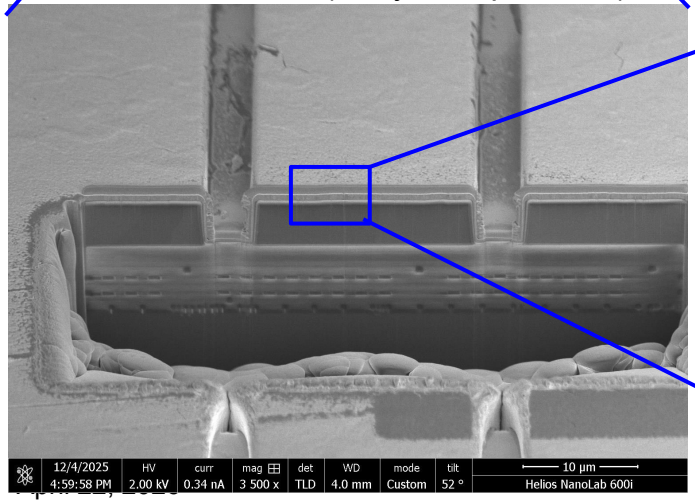




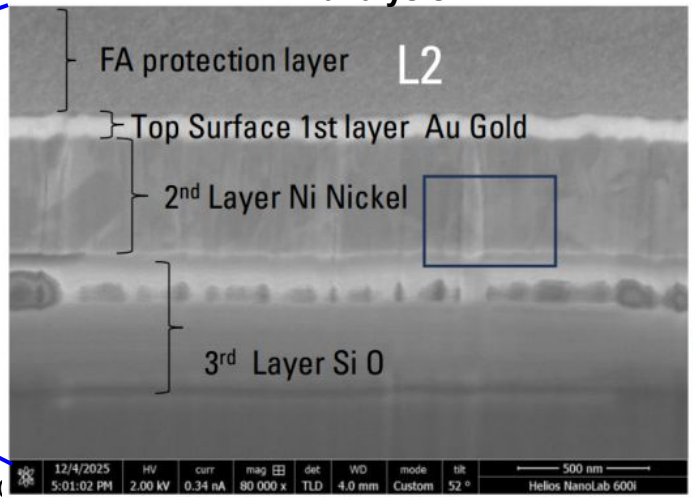


Results from investigation carried out by packaging vendor

FIB dissection (away from pad area)



EDX analysis

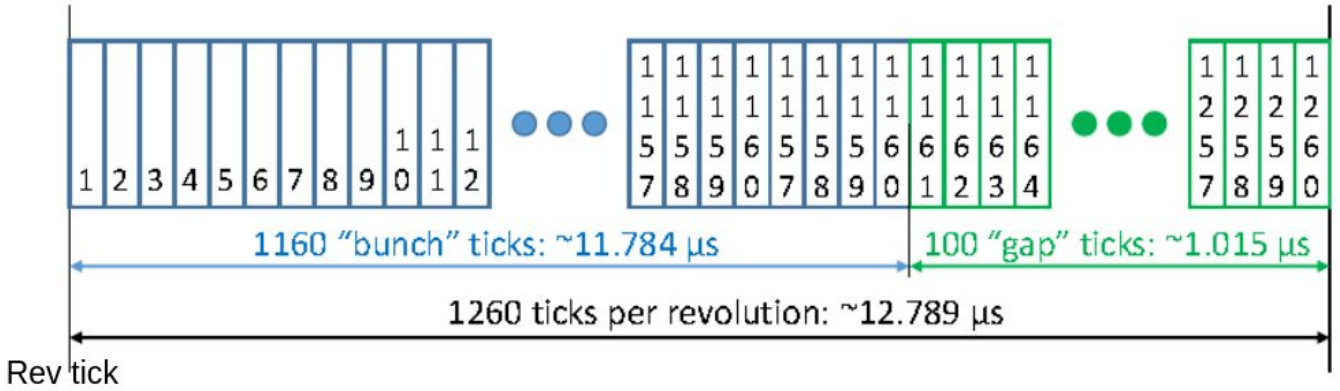


Au and **Ni** layers are from **UBM process** and they are above chip passivation layer, in an area away from bump pads

This shows that we have exposed metals between pads

EIC beam structure and bunch crossing timing

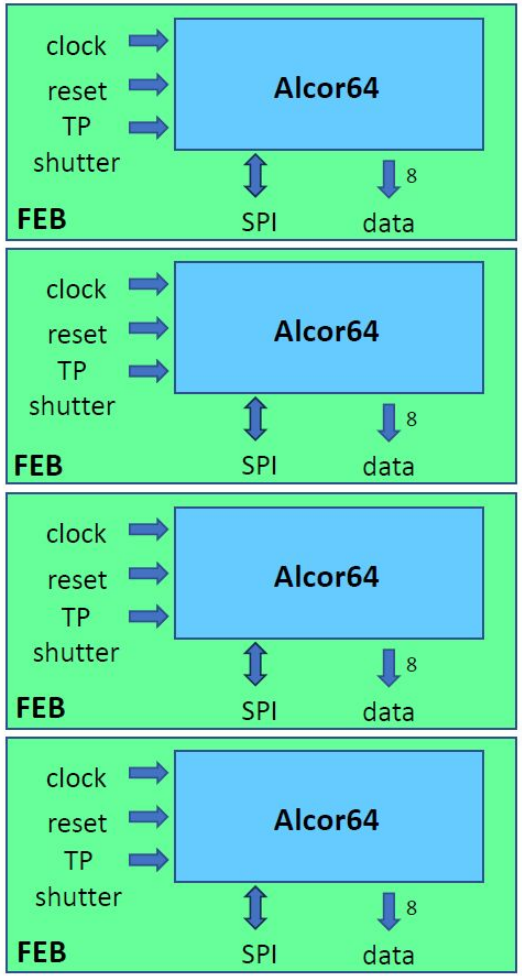
- Beam structure repeats every ~12.7886 µs
  - → Revolution frequency: ~78.195 kHz
- 1260 clock ticks in each revolution
  - → Clock period: ~10.14968 ns, frequency 98.52525 MHz ⟶ **ALCOR shutter frequency**
  - → 1160 filled "bunch" ticks, may be not all filled with particles
  - → 100 "gap" ticks without particles ⟶ **use for frame reset**

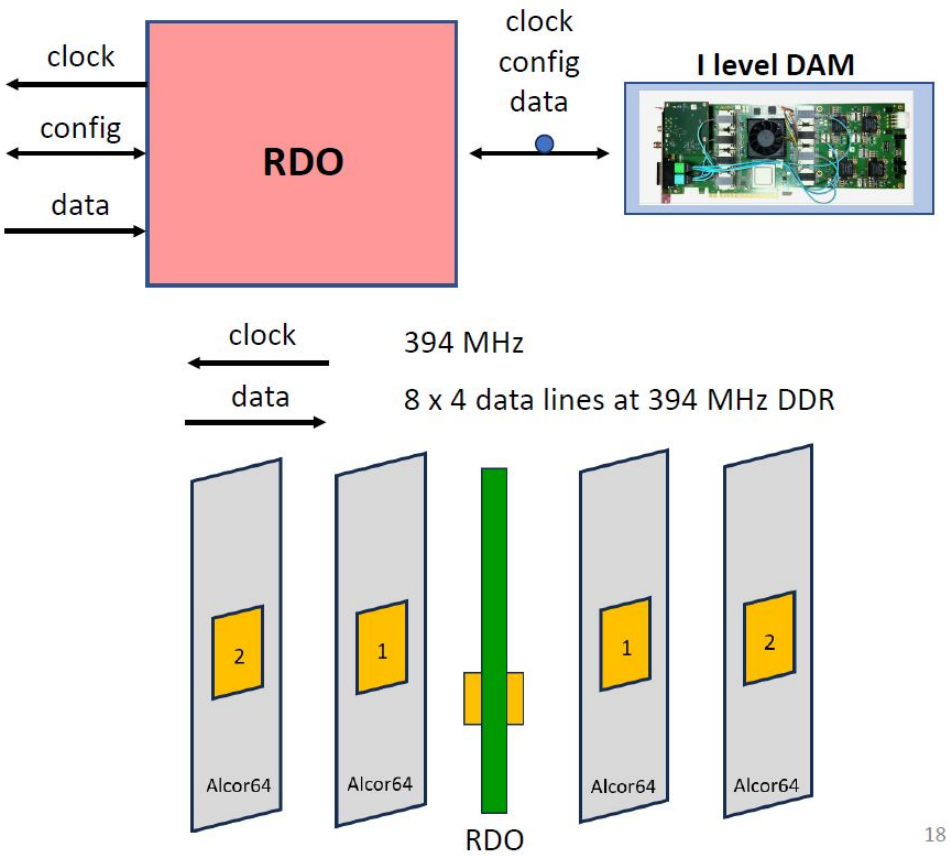


dRICH output bandwidth

- Without data reduction with a 100 kHz DCR we are close to DAM bandwidth limit
  - A data reduction factor 5 allows us to stay safe up to the 300 kHz limit
  - Data reduction factor five can be achieved via shutter or provided by NN or ext. trigger or a combination of them.

Readout concept: 4 Alcor64



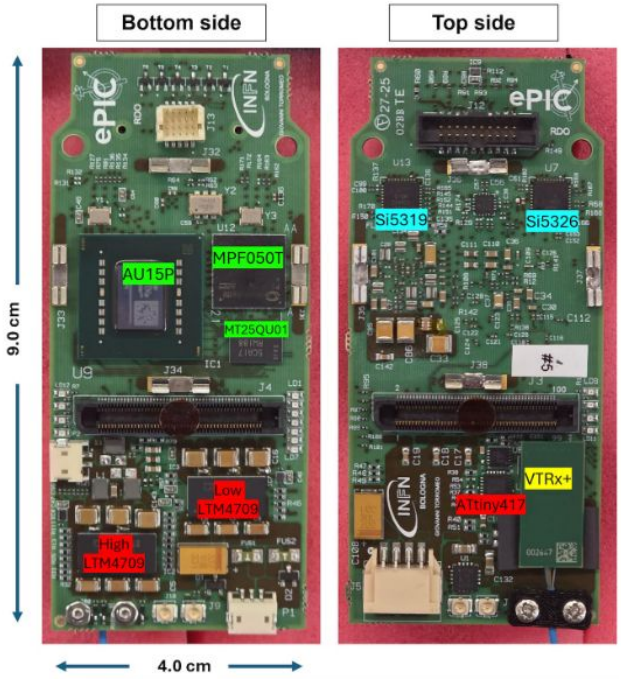


dRICH DAQ building blocks

FEB

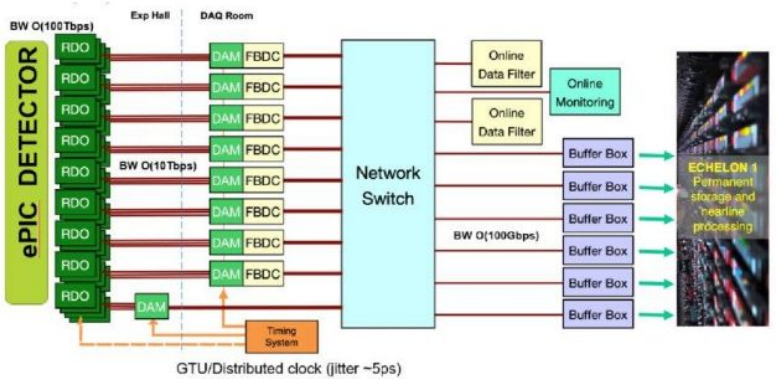
ALCOR-64

RDO



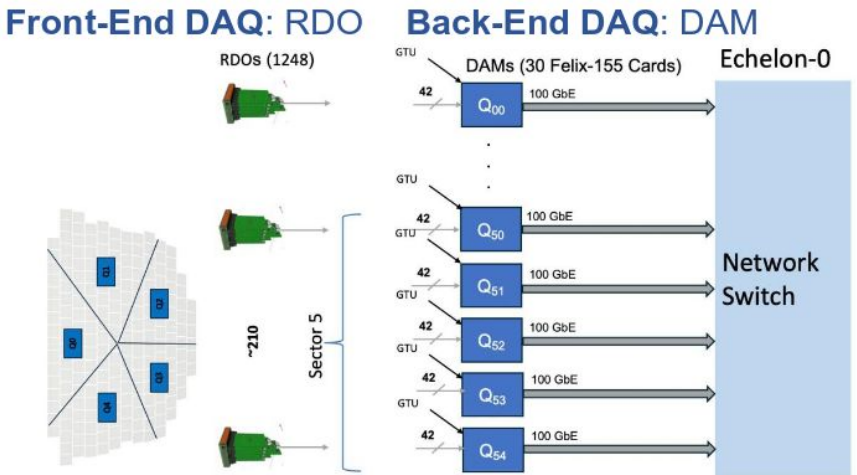
FLX-155

RDO/DAM role in ePIC and dRICH PDU



Data Aggregation Module (DAM)

- Implemented on Felix-155 board (INFN Rome)
- Aggregates data from 42 RDOs and transmit them to the ePIC buffering system (Echelon 0) through 100 GbE links.
- Provides computational capability for data handling and reduction



DAM Status: O. Frezza @dRICH General Meeting on DAQ

dRICH DAQ Working Group

Recent talks:

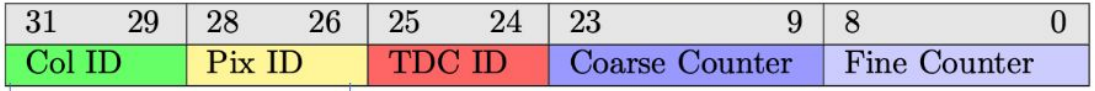
- dRICH Interaction tagger: S. Vallarino @EICUG-ePIC 2025
- RDO: P. Antonioli @EICUG-ePIC 2025
- RDO rad. tests: S. Geminiani @TWEPP2025
- ML for data reduction in DAMs: C. Rossi @RICH2025
- dRICH DAQ: towards a full push-data architecture: P. Antonioli @SRO XII – Dec 2025
- dRICH DAQ from ALCOR to DAM: F. Lo Cicero @ePIC meeting – Jan 2026

- ePIC dRICH DAQ: P. Antonioli @dRICH General Meeting on DAQ – Mar 2026
- ALCOR Simulation and Time Ordering: C. Ferrero @dRICH General Meeting on DAQ – Mar 2026
- Update on the firmware design for the dRICH-RDO card: S. Geminiani @dRICH General Meeting on DAQ – Mar 2026
- DAM Status: O. Frezza @dRICH General Meeting on DAQ – Mar 2026
- dRICH Online Data Filter: C. Rossi @dRICH General Meeting on dRICH Data Filter – Apr 2026

ALCOR data (raw) and ePIC data (I)

ALCOR hits "event word" are timestamps

accelerator BC: bits 23 – 11



3 bits to identify the column (LVDS TX lane) [0 to 7]

3 bits to identify the pixel [0 to 7]

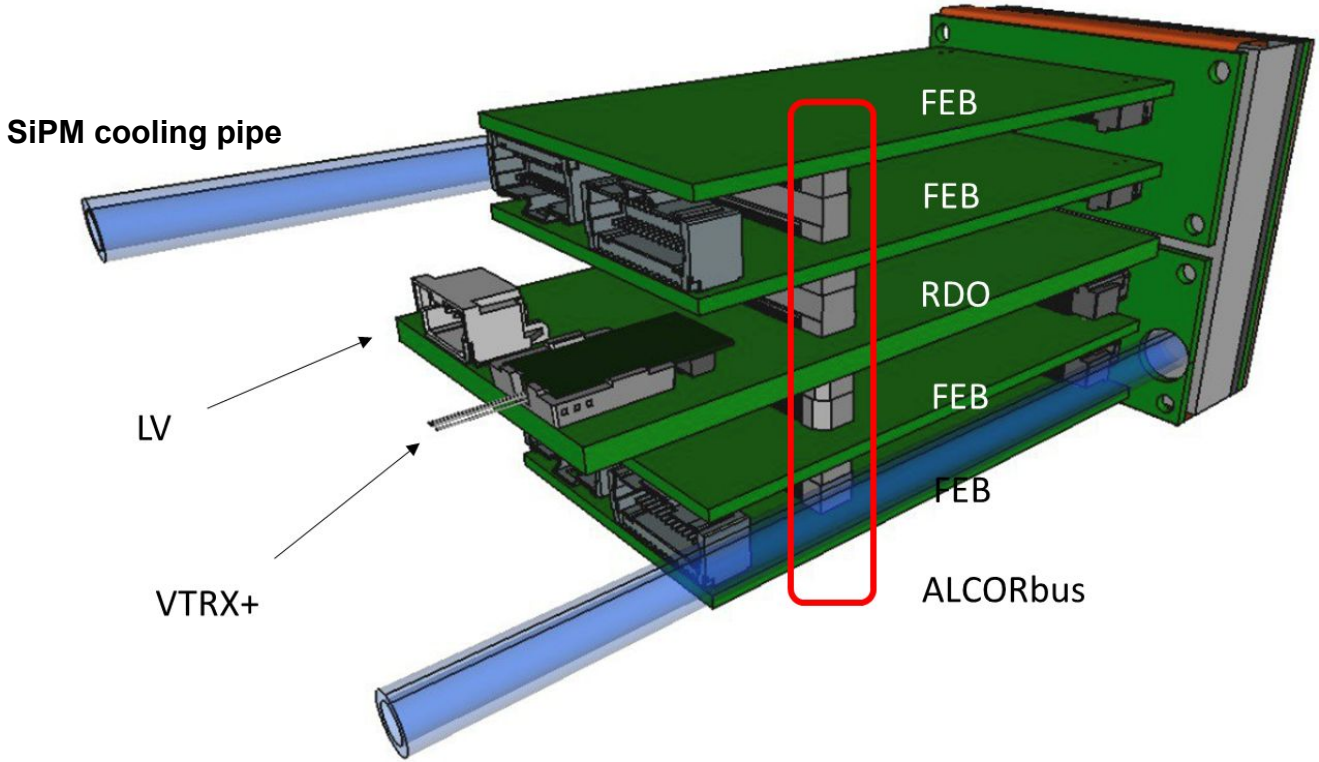
4 TAC TDC IDs: 2 bits
→ 2 TDCs for leading edge
→ 2 TDCs for trailing/slew rate

these nine bits are the fine measurement of the TDC
you can reach 20-40 ps LSB at 394 MHz.
Calibration needed → can't be used at DAM level "as it is"

394 MHz → coarse counter LSB 2.54 ns (currently 320 MHz → 3.125 ns)
15 bit coarse counter (0x7FFF = 32767)

Coarse counter expires every 83.228 μs > 12.78 μs (EIC orbit)
At each EIC orbit we get a RevTick signal from DAM (main EIC "synch")
→ this trigger a coarse counter reset and a frame structure injected in data flow

dRICH photodetector unit (PDU)



SMA-annealing FEB

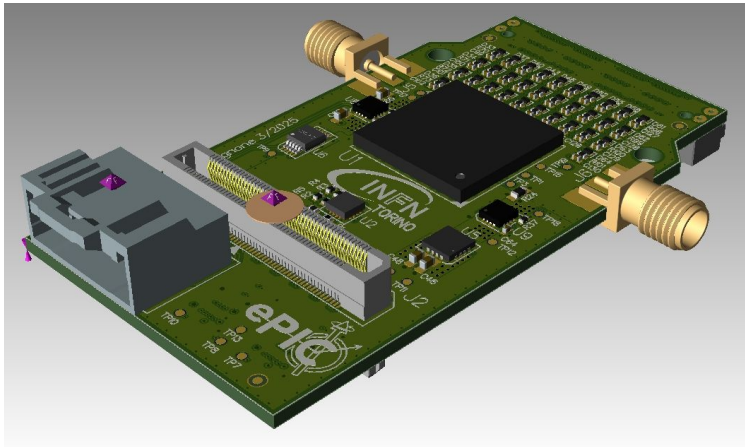
FEB prototype to test SiPM annealing

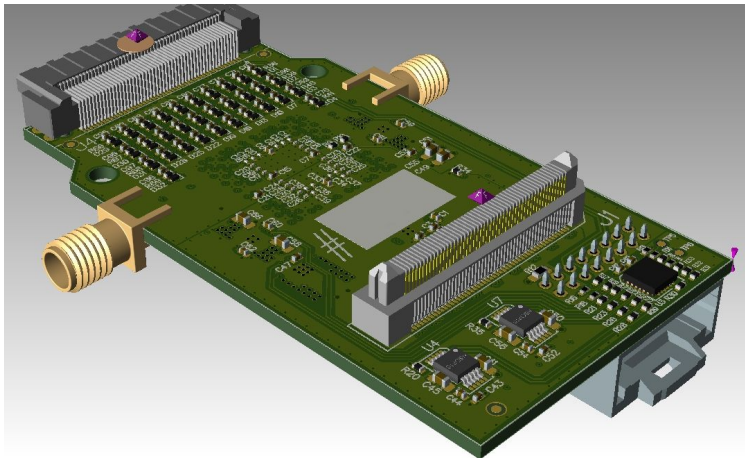
- like final FEB, with all annealing circuitry
- added **2 SMA connectors** to inspect SiPM signals (ALCOR inputs) on scope → initially can be used also without ALCOR-64

Goals:

➔ test **realistic dRICH annealing electronics**

➔ study annealing process details and provide critical guidance for the final engineering and important reference data for **simulation of heat-dissipation** and the **design of the cooling system**





Annealing + AC coupling circuit

AC coupling circuit

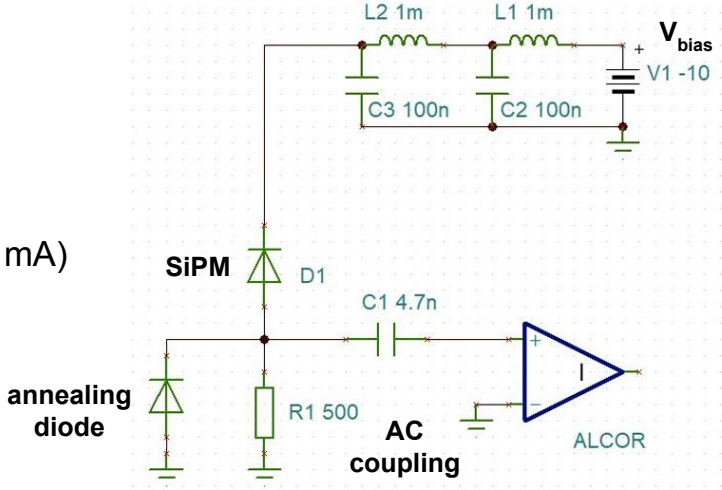
- cut SiPM signals tail
- protect ALCOR input from SiPM current during annealing

Annealing diode

- provide path to ground for SiPM annealing current (up to 100 mA)
- trade-off between C_{in} and power

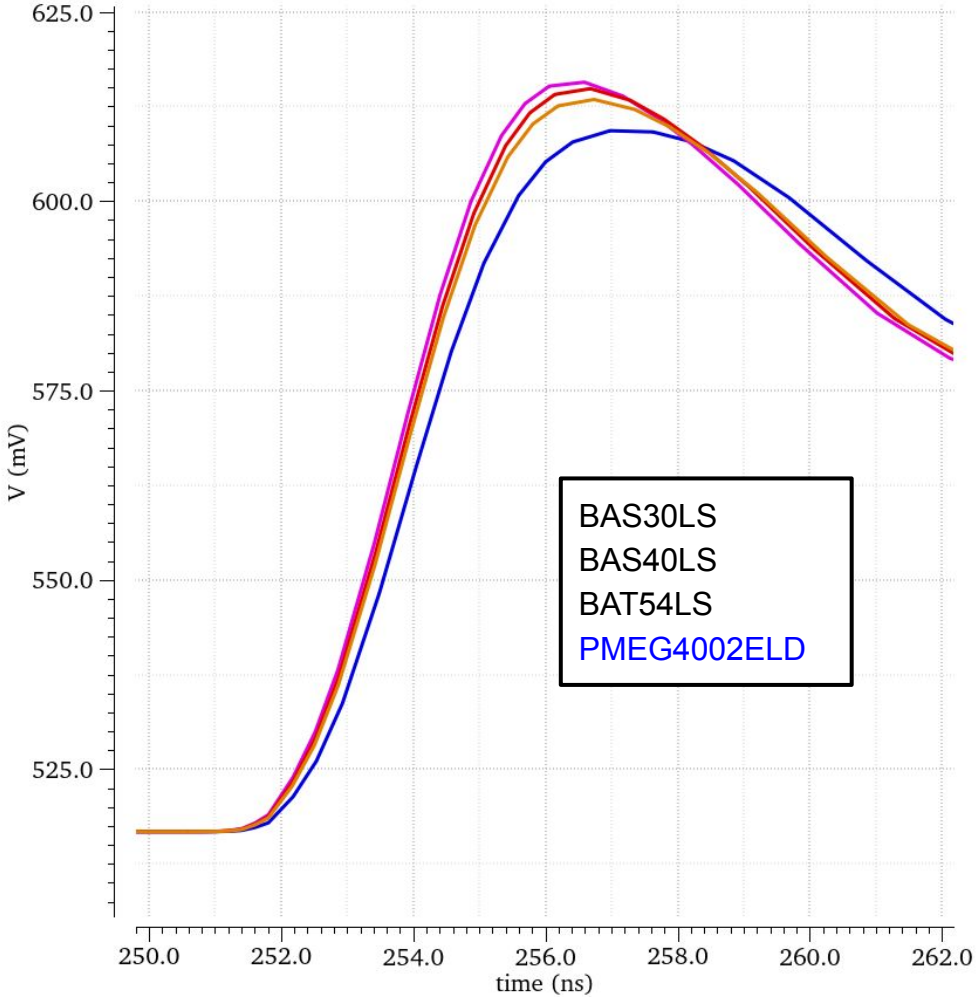
FEB prototype production

➔ select 2 different diodes but keep same footprint:
SMD0402, SOD882BD package



Annealing diodes survey:

BAS30LS	C = 2 pF	V_f = 0.85 V	→	P = 51 mW	(I_f = 60 mA)
BAS40LS	C = 5 pF	V_f = 0.68 V	→	P = 41 mW	(I_f = 60 mA)
BAT54LS	C = 10 pF	V_f = 0.48 V	→	P = 29 mW	(I_f = 60 mA)
PMEG4002ELD	C = 14-20 pF	V_f = 0.30 V	→	P = 18 mW	(I_f = 60 mA)



ALCOR + ann. diodes simulations

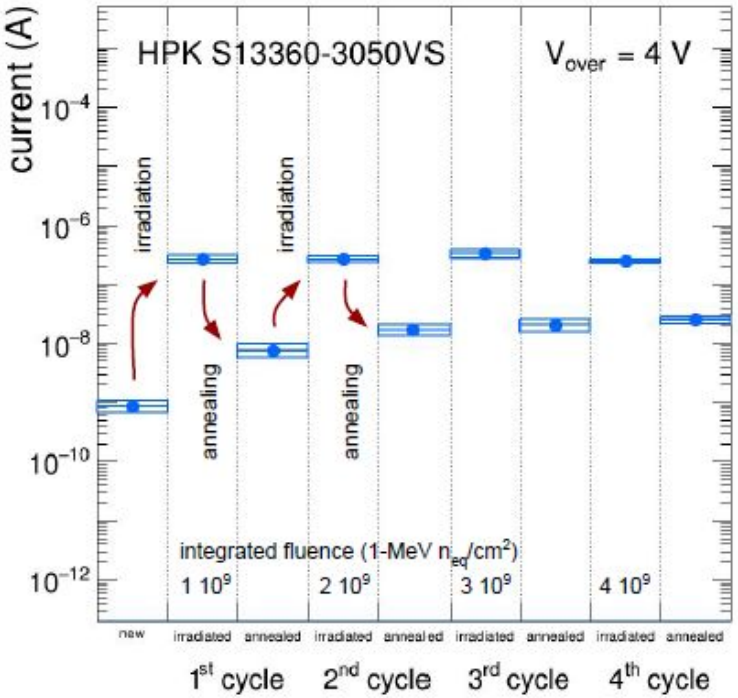
Test input line capacitive loading due to diode capacitance

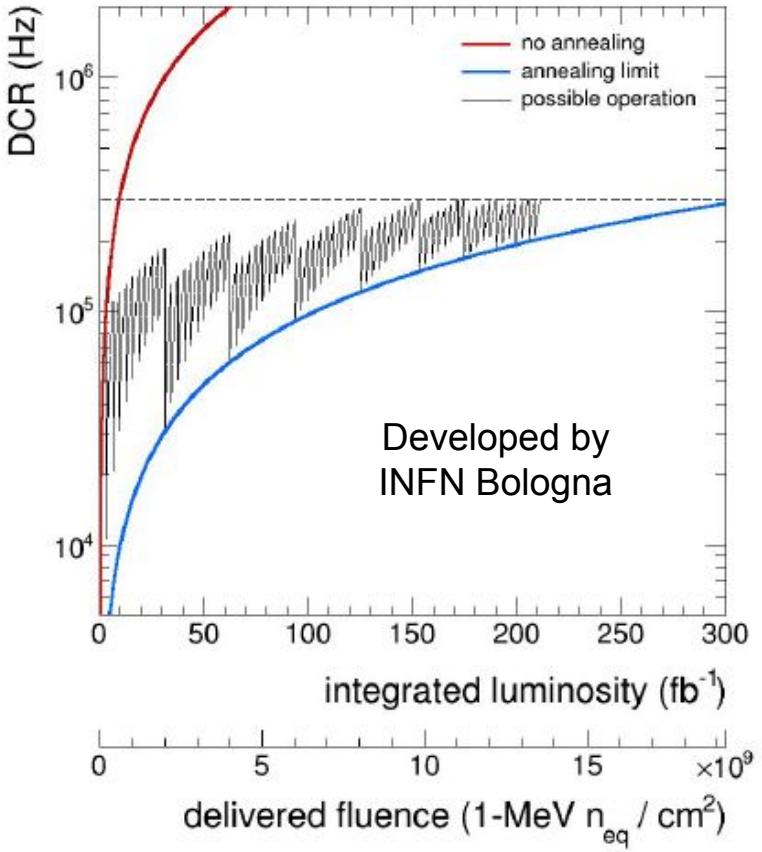
Larger C diode slightly reduces signal slope and thus time resolution (<10%)

Proposal for FEB prototypes (master + slave):

- 3+3 FEBs with **PMEG4002ELD**
- 3+3 FEBs with BAT54LS
- 1+1 FEBs without diodes

SiPM annealing model





Shutter mixed-signal simulation

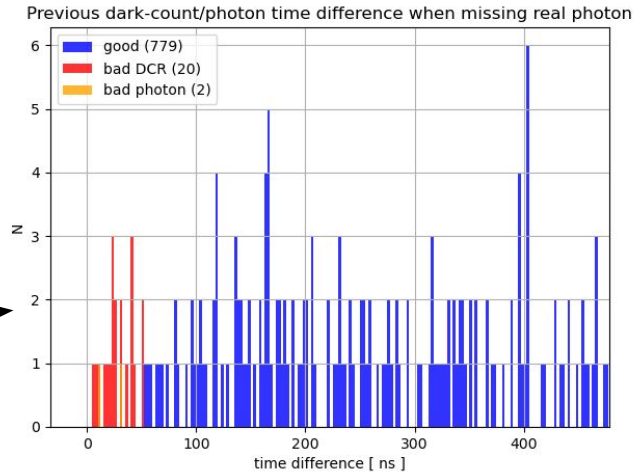
Shutter: periodic test-pulse (width = 2.5 ns)

Spectre netlist simulates different SiPM SPADs:

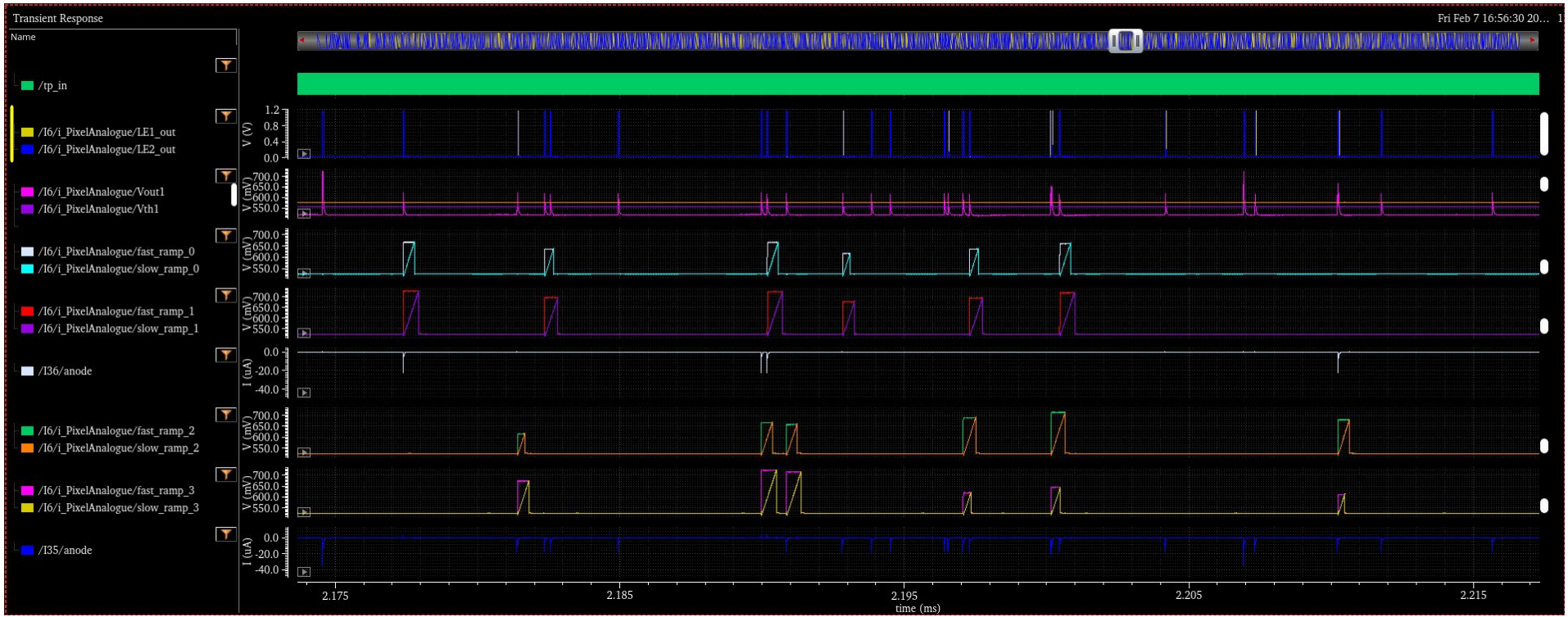
- Each **SPAD** is modeled with a current pulse generator, each with a different period
- **Real photons**: current pulse generators are synchronized with the shutter signal
- **Dark-count signals**: current pulse generators are not synchronized

Decode data, calibrate TDCs (from DCR asynchronous signals), extract ToA, compare with input netlist to evaluate shutter efficiency:

```
Total simulation time = 19532690.640 ns
Total number of dark counts = 10006
Dark count rate = 512.269 kHz
Dark counts cut by shutter: 8411
Dark counts passed through shutter: 1595
Shutter cut: 84.06%
Good events: 842
Missing events: 22
Efficiency: 97.45%
```



Shutter mixed-signal simulation (SlewRate mode)



Shutter efficiency vs DCR (mixed-signal sim)

- Shutter width = 2.5 ns
- Input rate = 20 kHz
- Sim time = 20 ms

Ongoing: digital simulations (with improved DCR and photons signals model) to verify shutter distribution for the whole ALCOR chip and provide better statistics

Total simulation time = 19427451.802 ns Total number of dark counts = 3082 **Dark count rate = 158.641 kHz** Dark counts cut by shutter: 2546 Dark counts passed through shutter: 536 **Shutter cut: 82.61%** Good events: 388 Missing events: 2 **Efficiency: 99.49%**	Total simulation time = 19996870.504 ns Total number of dark counts = 6325 **Dark count rate = 316.299 kHz** Dark counts cut by shutter: 5286 Dark counts passed through shutter: 1039 **Shutter cut: 83.57%** Good events: 412 Missing events: 7 **Efficiency: 98.33%**	Total simulation time = 19532690.640 ns Total number of dark counts = 10006 **Dark count rate = 512.269 kHz** Dark counts cut by shutter: 8411 Dark counts passed through shutter: 1595 **Shutter cut: 84.06%** Good events: 842 (was 40 kHz) Missing events: 22 **Efficiency: 97.45%**
Total simulation time = 19989730.664 ns Total number of dark counts = 811 **Dark count rate = 40.571 kHz** Dark counts cut by shutter: 650 Dark counts passed through shutter: 161 **Shutter cut: 80.15%** Good events: 409 Missing events: 1 **Efficiency: 99.76%**	Total simulation time = 19962950.756 ns Total number of dark counts = 1604 **Dark count rate = 80.349 kHz** Dark counts cut by shutter: 1309 Dark counts passed through shutter: 295 **Shutter cut: 81.61%** Good events: 413 Missing events: 3 **Efficiency: 99.28%**	

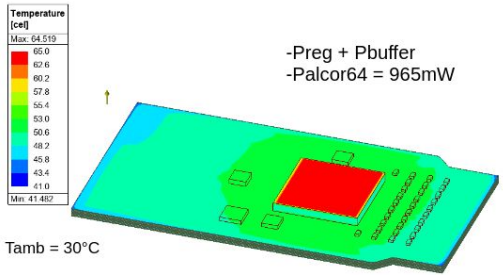
Thermal simulations (preliminary)

Preliminary thermal simulations of one FEB board during **normal operations** and while performing **annealing** embedded in a static T = 30°C ambient

Note: this is a first and simplified simulation of the board without air circulation and without taking into account other heat sources and the complexity of the surrounding environment

- first guidance on the possible **temperature profiles**
- useful to put **requirements** on **dRICH box cooling**
- valuable to **compare** with simplified **test benches**

Normal mode (ALCOR ON)



-Preg + Pbuffer
-Palcor64 = 965mW

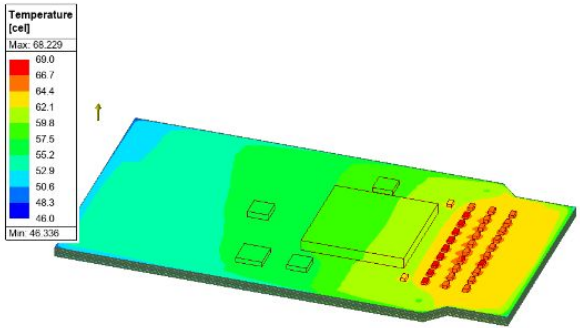
Tamb = 30°C

-BGA
Tj = 64.8 °C

-PCB(Top):
Tmax = 53°C
Tmean = 50°C

-PCB(Bot):
Tmax = 52.7°C
Tmean = 50°C

Annealing mode (V_f = 0.43 V @70°C x 60 mA → 26 mW)



Tamb = 30°C

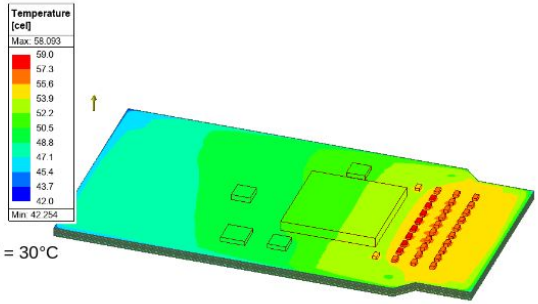
-DIODI:
64 x 26 mW
Tmax = 68°C

-BGA:
Tmax = 61°C
Tmean = 59°C

-PCB(Top):
Tmax = 67°C
Tmean = 57°C

-PCB(Bot):
Tmax = 68°C
Tmean = 57°C

Annealing mode (V_f = 0.30 V @55°C x 60 mA → 18 mW)



Tamb = 30°C

-DIODI:
64 x 18 mW
Tmax = 58°C

-BGA:
Tmax = 53°C
Tmean = 52°C

-PCB(Top):
Tmax = 58°C
Tmean = 51°C

-PCB(Bot):
Tmax = 58°C
Tmean = 51°C