ALCOR-64 REVIEW

DETAILS ON THE DIGITAL CIRCUITS

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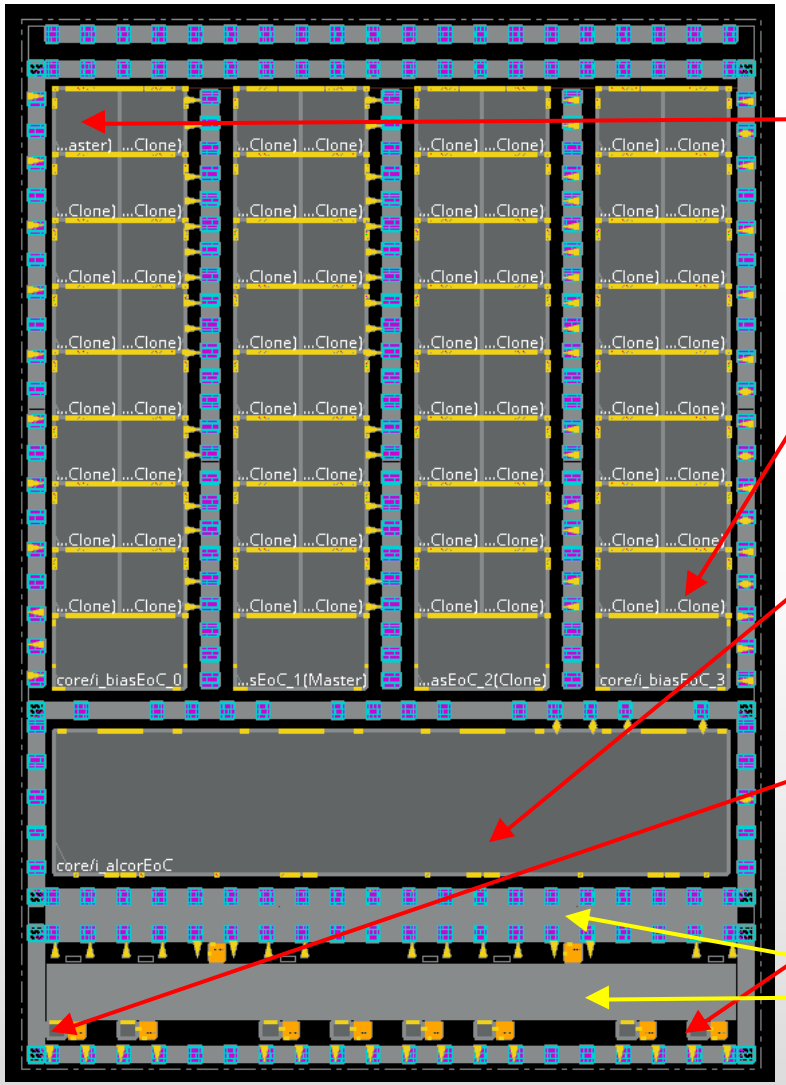
Digital blocks



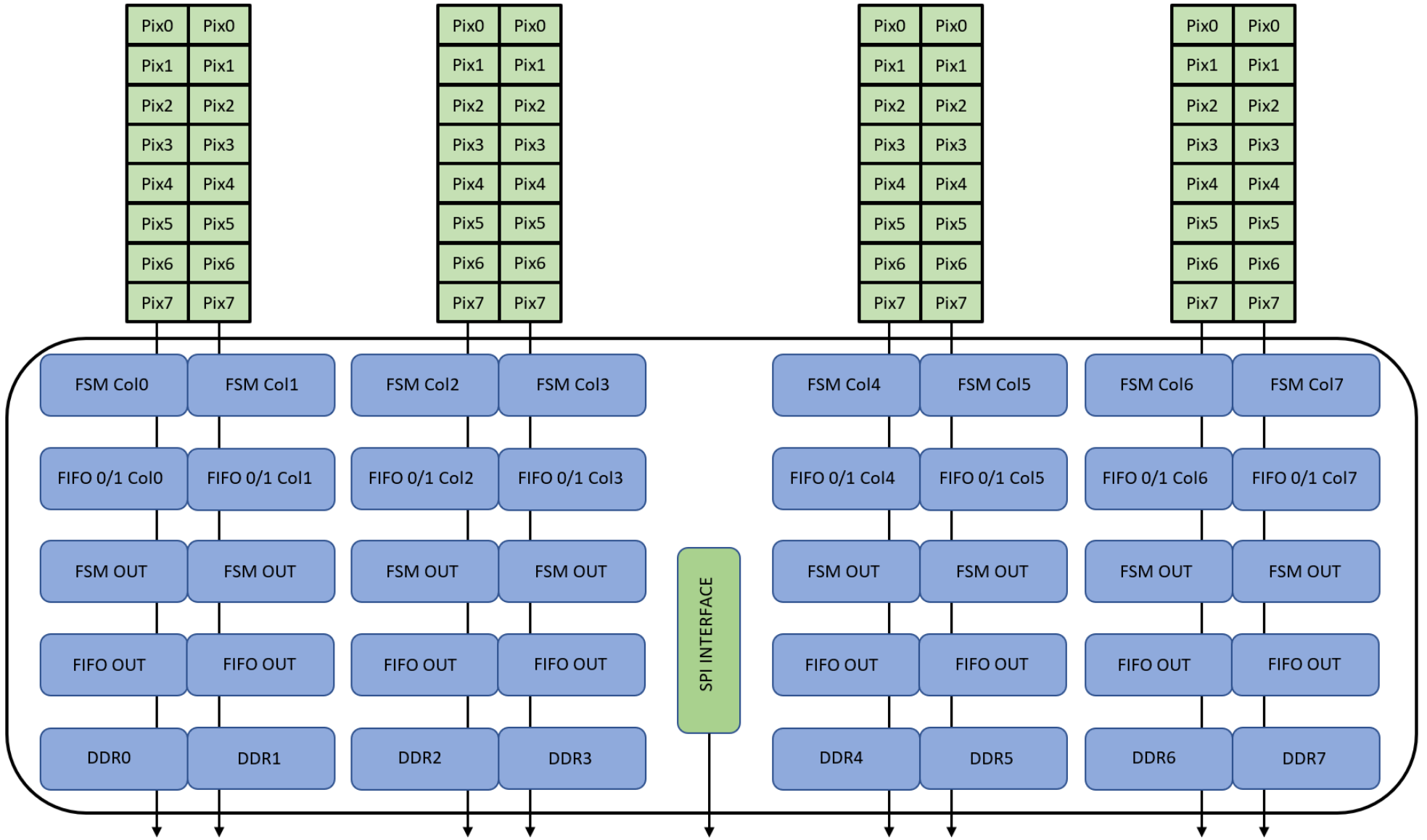
Pixel x 64

End Of Column + SPI
(8 replicated readout circuits)

DDR x8

Standard cells area for digital repeaters

Block Diagram



Digital Pads

- Differential LVDS signals for all of them
- CLOCK
- Reset (3 different functions)
- Test Pulse / Digital Shutter
- DATA Out (x8, DDR serializers)
- SPI interface
- CLOCK Out (programmable option for external synchronization)
- Digital Power (Core, 1.2 V)
- Digital Power (I/O, 2.5 V)
- Digital Ground

Design methodology

- Top level implementation "digital on top":
  - Floor planning
  - Block connections
  - Top Level Power and Signal Routing
- Created partitions: DDR, EoC and Pixel
- Development of each partition
  - RTL
  - Synthesis
  - PnR
  - Digital Simulation
- Assembling top level design for digital analysis
  - Digital simulations (full chip)
  - Digital Power Analysis (full chip)
- Mixed signal simulations performed on the single pixel
- Final tape-out, DRC and LVS with Virtuoso and Calibre

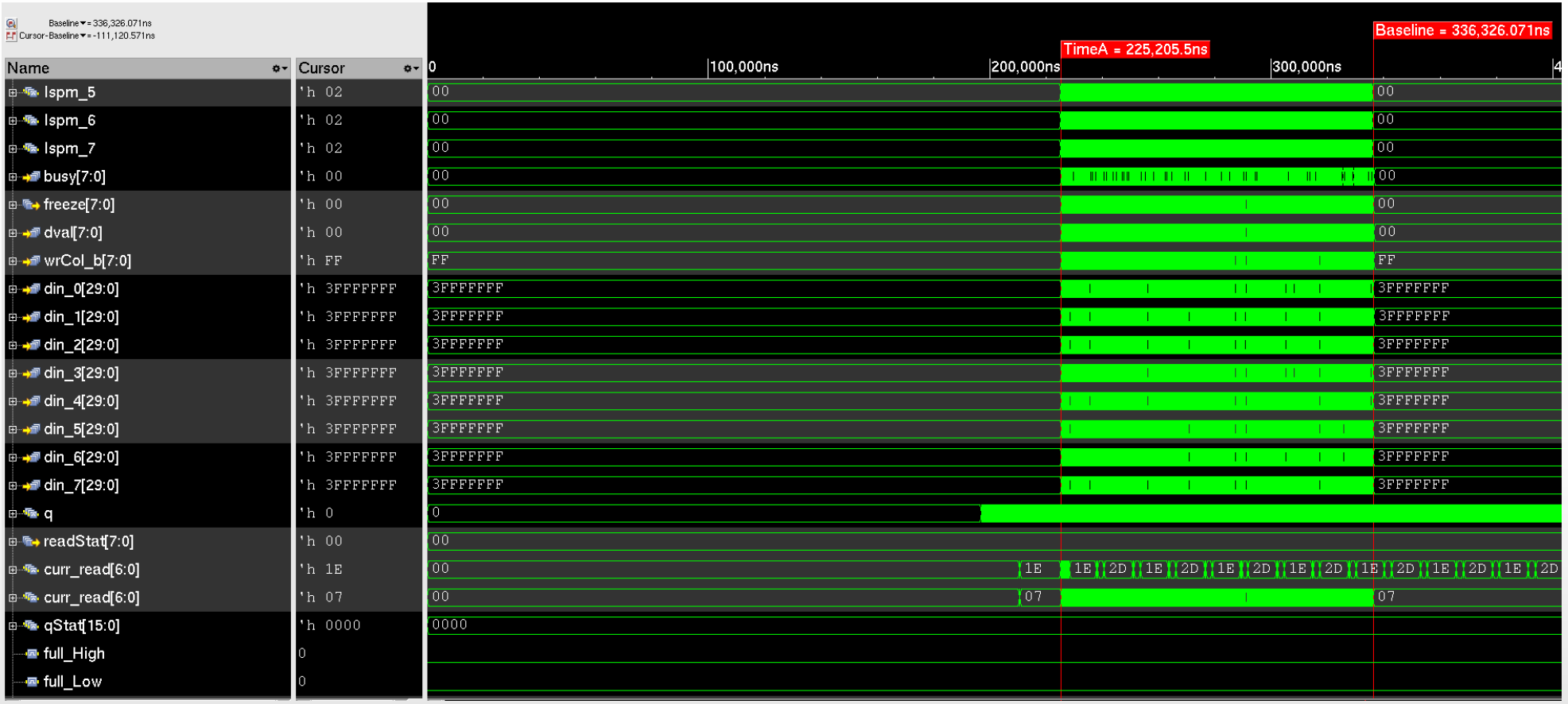
SEU Protection

- Pixel digital
  - Configuration registers: TMR with voting and self-correction
  - FSMs: Hamming Code (Single Error Correction)
- EoC
  - Reset FSM: TMR with voting and self-correction (to add TMR at counters used by FSM)
  - Readout FSMs: Hamming Code (Single Error Correction)
  - Configuration registers: TMR with voting and self-correction
- SPI:
  - TMR with voting and self-correction around the main SPI Shift Register (no the Shift Register itself)

Data rates

- Data words width are 32-bits
  - LE mode 1 data word per hit
  - TOT/SR modes 2 data words per hit
  - Headers/Trailers inserted for each frame (see later)
  - Optional Status Words
- 394.1 MHz clock frequency (4x EIC clock: 98.52525 MHz):
  - DDR with 8b10b encoding: 788 Mb/s, after 8b10b decoding => ~19.6 Mhits per column
  - 2.4 Mhits per pixel in LE mode
  - 1.2 Mhits per pixel in TOT/SR modes

Data rates



- Full chip post pnr simulations: data rates up to 16 MHz per column without loss (data with headers and without status words)
- 2 MHz per pixel (leading edge mode)

Reset operations

- Reset signal with 3 different features depending on the signal width:
  - 24-31 xCLK: Hard Reset
  - 16-23 xCLK: Start (Frame Counter = 0 and Coarse Counter = 0)
  - 8-15 xCLK: New Orbit (Frame Counter +1 and Coarse Counter =0).
- A single FSM (TMR protected) manages the incoming reset signal
- First frame sent after EoC configuration
- New orbit forces a rollover condition (ALCOR rollover = 2^{15} clk cycles ≈ 83 μs, EIC orbit period ≈ 12.8 us)
- Reset latency. Reset command is decoded at the end of its cycle. Reset distribution inside the chip adds more latency because there are synchronizer circuits inside the EoC and Pixel logic. So, Coarse Counter reset is performed 12 clks after the reset signal is de-asserted (30 ns)

Data Format

31 29	28 26	25 24	23 9	8 0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter

- 32-bit event world encapsulated between Header/Trailer in frames for each rollover/orbit
- Data stream includes also K codes, which are 8b10b embedded symbols providing additional information
- Optional status words from pixels (programmable feature for debug)
- 32-bit CRC for each frame

Data format

8b10b valid codes			
Code	Hex	Use	Notes
28.0	1C	Frame header	New Coarse Counter frame
28.1	3C	Align Comma	Forced from SPI configuration
28.2	5C	End of frame header	Coarse Counter rollover or End of Frame
28.3	7C	Status header	Next words are Status
28.4	9C	CRC header	Next word is CRC
28.5	BC	Idle comma	EoC output FIFO is empty
28.6	DC	Not used	Not used
28.7	FC	Do not use	Can interfere with align comma

FIFO position	Data
1 (FPGA first received)	K28.0 (Frame header)
2	Frame number (16 bit)
3..	Pixels Event Words
..	..
n	K28.2 (End of frame header)
n+1	K28.3 (Status header)
n+2	Pixels Status Words (x8)
n+10	End of Column status word
n+11	K28.4 (Checksum header)
n+12	CRC value
n+13	K28.0 (New Frame header)

Table 5: Data stream with data events and status words.

FIFO position	Data
1 (FPGA first received)	K28.0 (Frame header)
2	Frame number (16 bit)
3..	Pixels Event Words
..	..
n	K28.2 (End of frame header)
n+2	End of Column status word
n+3	K28.4 (Checksum header)
n+4	CRC value
n+5	K28.0 (New Frame header)

Table 6: Data stream with data events without status words.

Pixel Status Words								
	31..29	28..26	25..20	19..16	15..12	11..8	7..4	3..0
pix 7	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 6	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 5	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 4	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 3	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 2	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 1	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt
pix 0	Col ID	Pix ID	Lost Ev	Lost TDC1	Lost TDC2	Lost TDC3	Lost TDC4	SEU Cnt

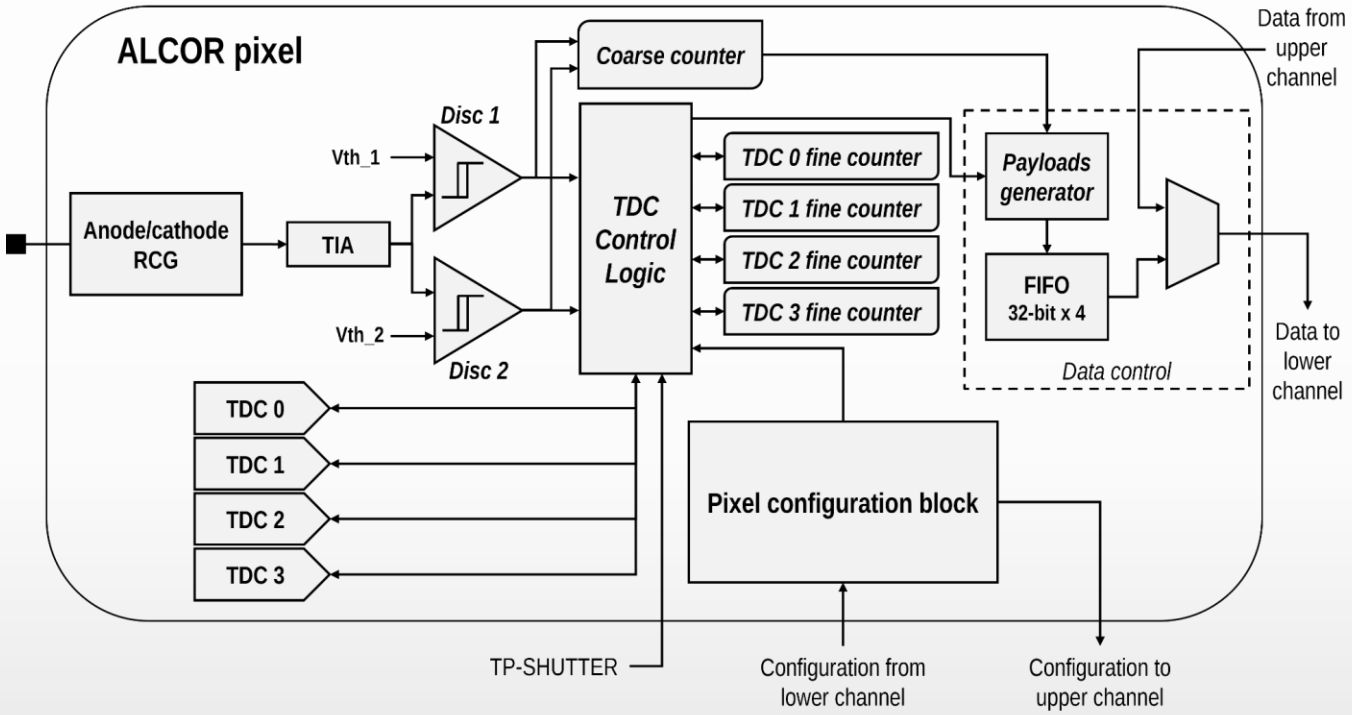
EoC Status Word in case of Coarse Counter Rollover			
	31..24	23..16	15..0
	EoC OUT FIFO loss	EoC IN FIFO loss	0x7FFF

EoC Status Word in case of Start or New Orbit request			
	31..24	23..16	15..0
	EoC OUT FIFO loss	EoC IN FIFO loss	Last value of Coarse Counter

Table 7: Status words.

More details on how to operate the chip available in the ALCOR-64 User Guide

Pixel Digital blocks



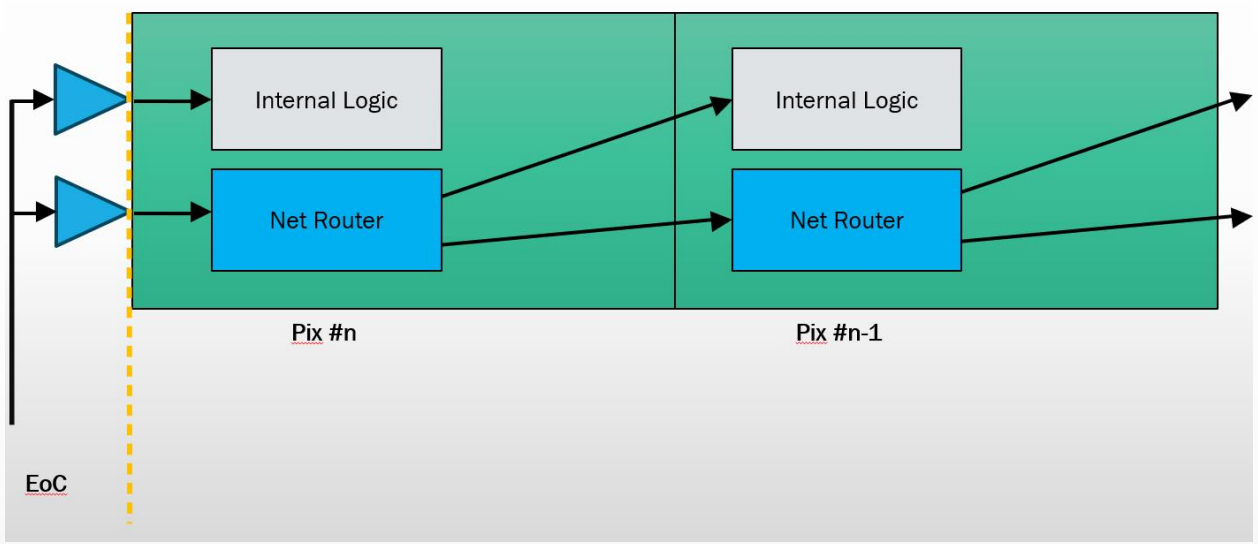
- TDC control logic (x4) with counters (Coarse Counter x1, Fine Counters x4)
- FSMs to handle the four operation modes:
  - LE
  - TOT
  - TOT2
  - SR
- Output data buffer (depth = 4)

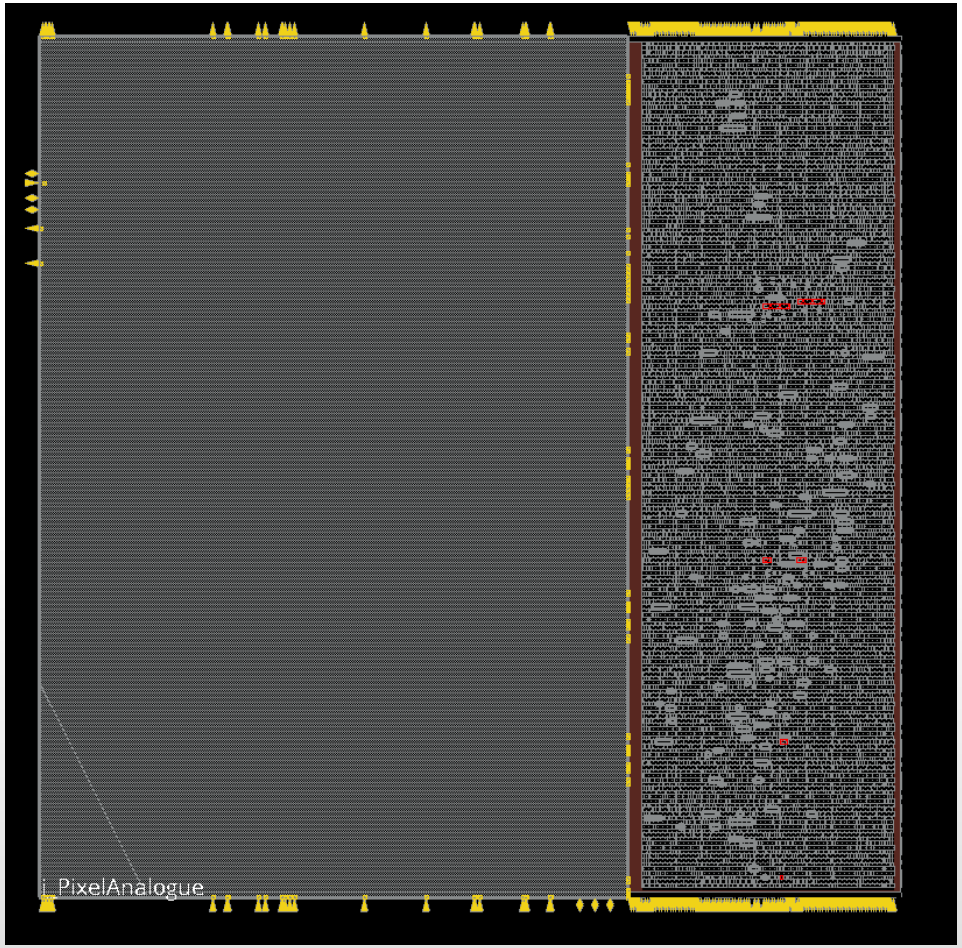
- Output data buffer read and write logic (FSM x2)
- Digital Shutter
- Configuration registers (16-bit x4)

Pixel-to-Pixel routing

- The routing of all the signals between the End of Column logic and the pixel matrix, has been done buffering every connection from pixel to pixel to avoid the use of very long nets requiring strong and large drivers
- To reduce the delay between one pixel and the next, the most critical signals - Clock, Test Pulse, and Reset - are distributed along the column (from bottom to top) with manually optimized routing and a controlled number of buffers
- More specifically, each of these signals is duplicated at both the input and the output of every pixel. One branch drives the internal logic of the pixel, while the other branch continues to the next pixel
- The “net router” is made up of a dedicated chain of buffers that ensures these signals are transferred with minimal delay
- As a result, the total propagation delay between the first and the last of the 8 pixels is around 2 ns under typical operating conditions

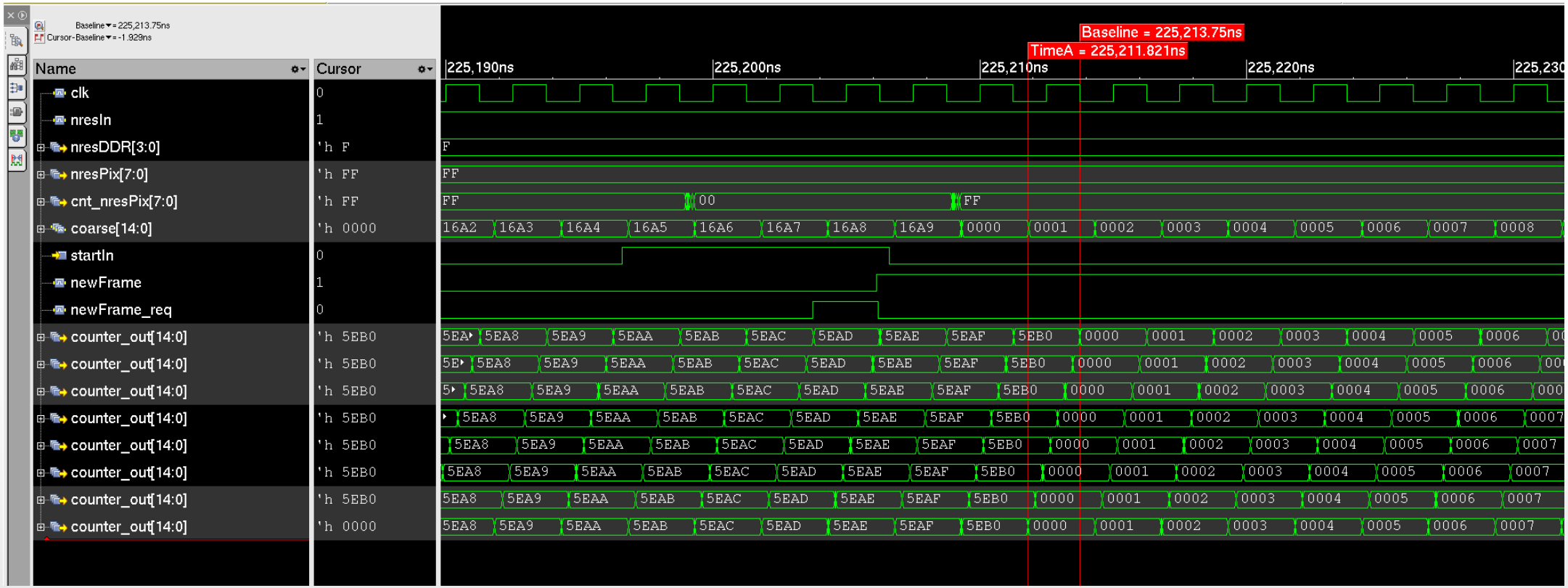
Net Router





- Pixel to pixel signal propagation
  - Automatic tree for most of them
  - Dedicated routing for TP, Start, Reset and CLK (Net Router component)

Reset distribution

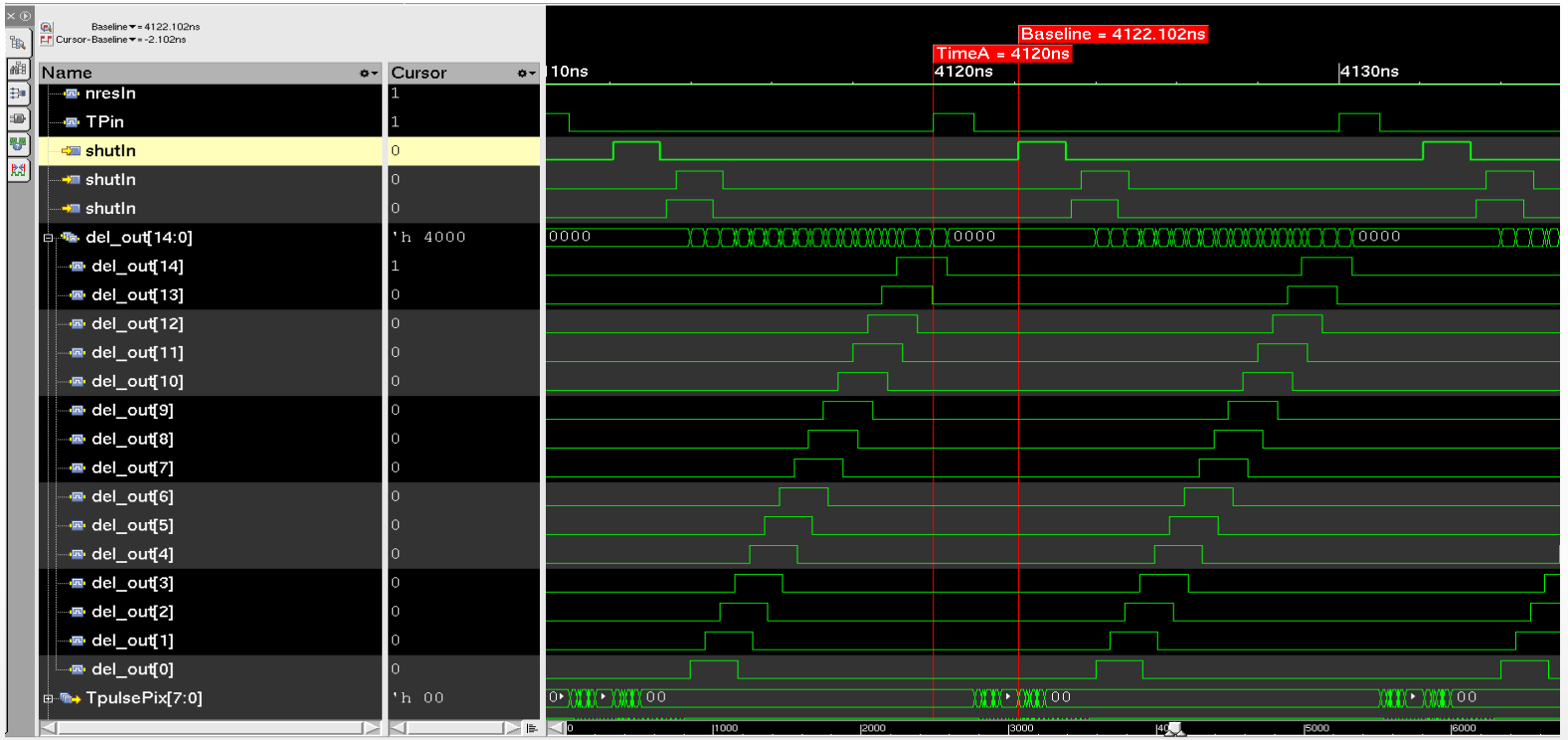


Less than 2 ns along the Pixel Column (post pnr simulation, TYP corner)

Digital Shutter

- Expected DCR below 300 kHz (with online annealing cycles on SiPM)
- Digital Shutter “inhibit” pixel digital logic to suppress out-of-gate DCR hits and reduce data throughput (~10.2 ns bunch crossing, ~300 ps bunch length)
- The external Test-Pulse is used as enable for the analogue trigger
- The minimum width of this timing window can be of the order 2-3 ns
- Each pixel implements a programmable delay chain to set the proper shutter timing window
- 4 configuration bits allow you to choose 16 steps from 0 to 15 delays
- Each delay step is approximately 350 ps (TYP corner)
- Additionally, the End of Column circuits allow you to choose a programmable delay, on the shutter signal, to adjust the skew between columns (16 steps from 0 to 15, each step approximately 100 ps)
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time. Use first period of ePIC data taking to optimize shutter calibration

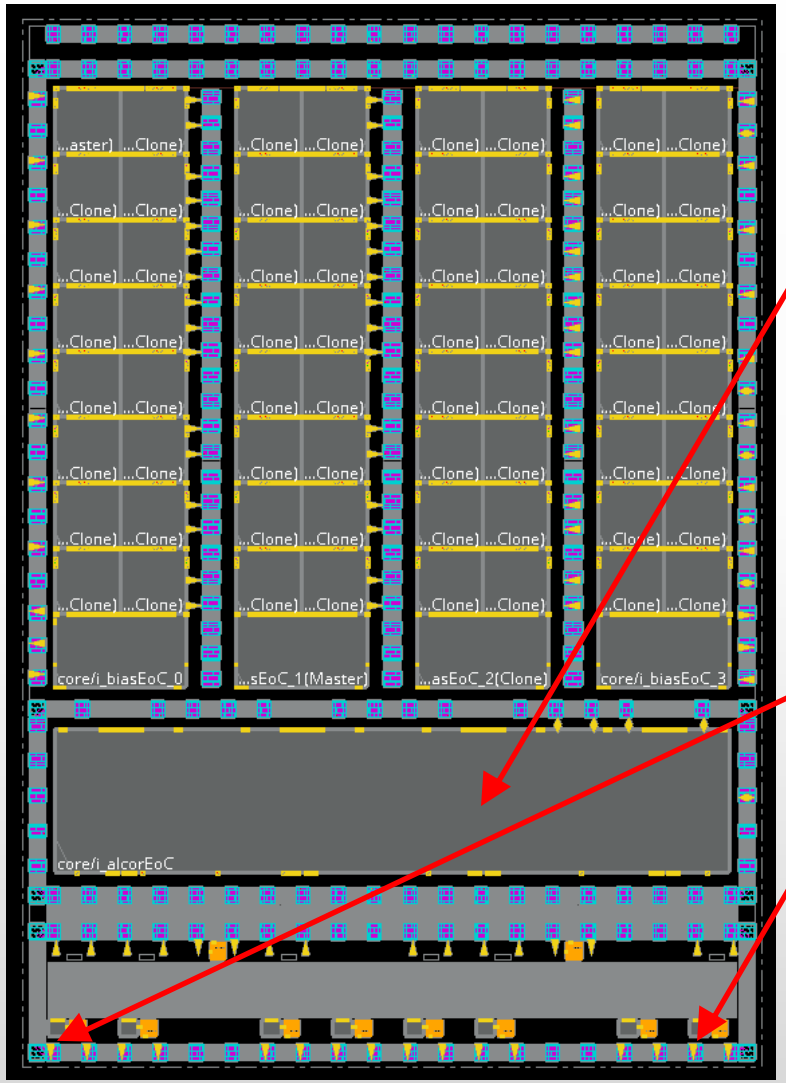
Test pulse distribution (TYP)



- External TP -> Shutter Pixel 7 Column 0 : 2.1 ns
- External TP -> Shutter Pixel 0 Column 0 : 3.67 ns
- External TP -> Shutter Pixel 0 Column 7 : 3.39 ns

- Row delta time : 1.53 ns
- Column delta time : 240 ps
- In pixel correction : 5.08 ns (360 ps each step)
- EoC correction (between columns) : 1.3 ns (each step 92 ps)

End of Column - DDR

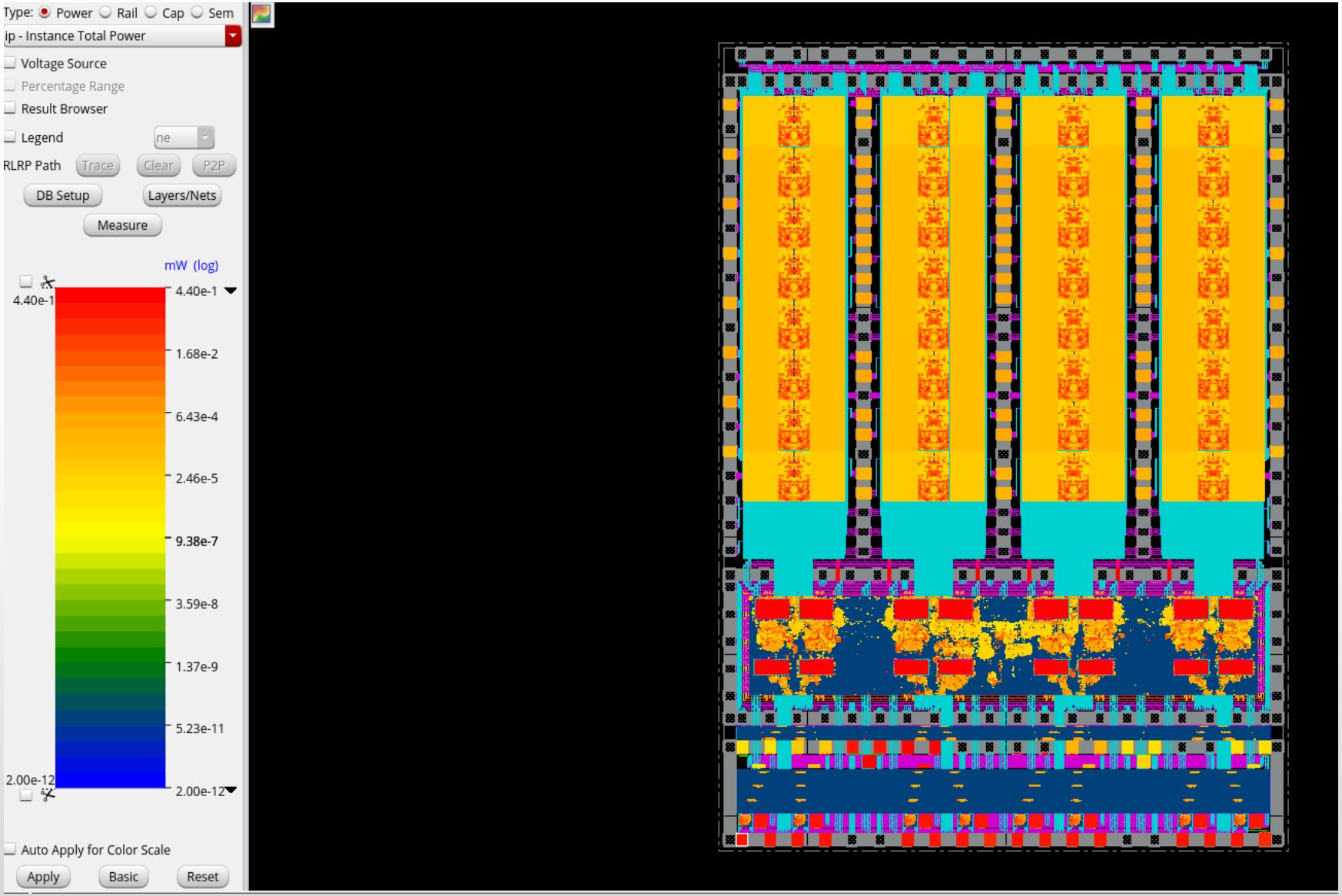


- End of Column
  - Pixels readout (one independent readout per column. 8 columns)
  - Signal and power distribution
  - Configuration Interface (SPI up to 20 MHz, 24-bit)
  - Status Registers through SPI
- DDR serializer
  - 8 LVDS serial out with 8b10b encoding
  - Data rate according to specifications is 788 Mb/s (design validated at 800 Mb/s)
  - 32-bit parallel interface to the End of Column block

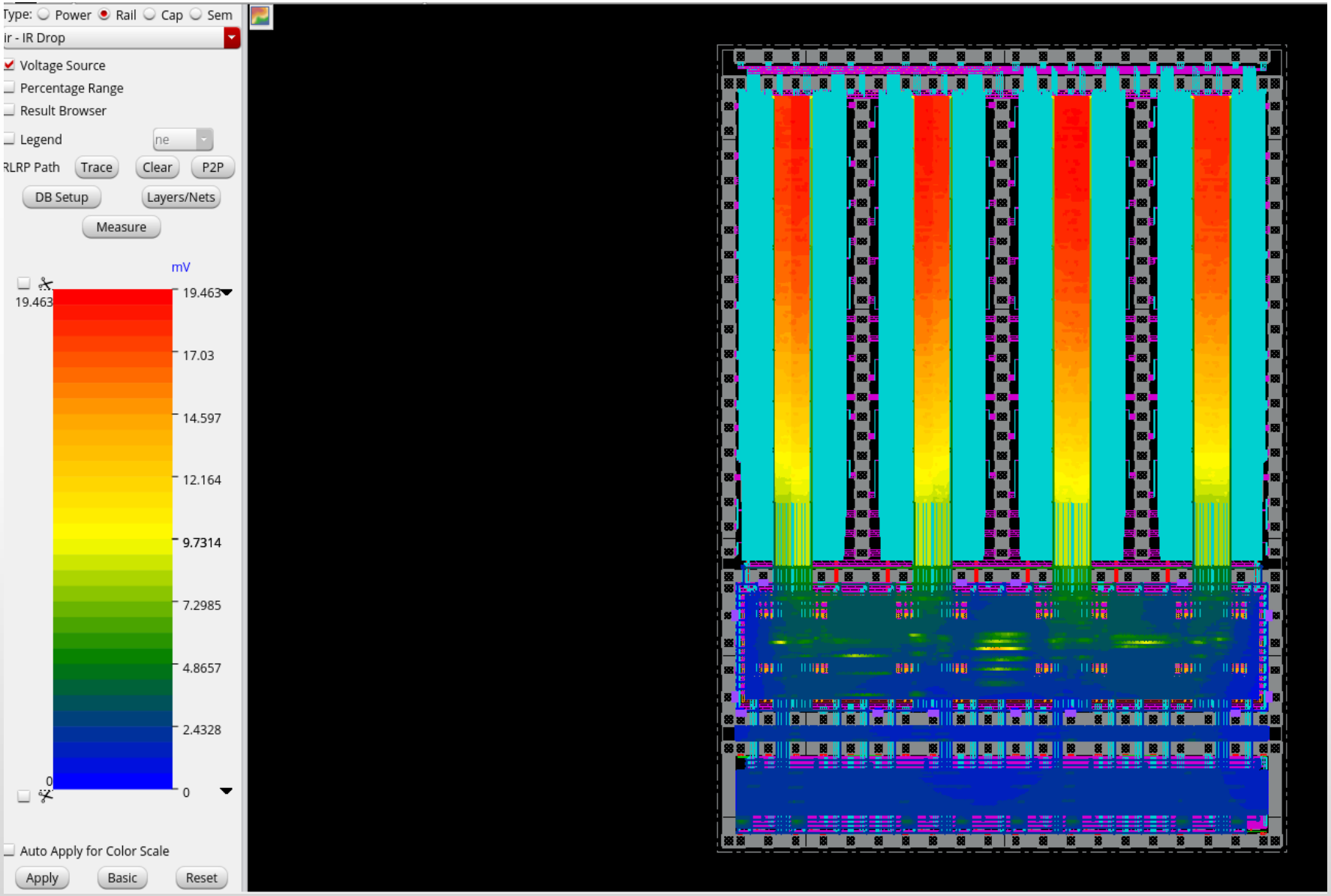
Power analysis

- Analysis done with VCD file form post pnr simulation at 400 MHz clock
- DVDD/DGND (1.2 V core)
- Testbench with all pixels enabled and data rate 10.84 MHz per column
- Total power consumption (digital core):
  - Total power 322 mW (200 mW internal 122 mW switching)
  - EoC 31.6 mW (17.75 mW internal, 13.86 mW switching)
  - Pixel 4.37 mW (2.78 mW internal, 1.59 mW switching)
  - ddr_reg 1.14 mW (0.7 mW internal, 0.44 mW switching)
- Estimated power consumption full chip 1.2 W (Digital + Analogue + Bias)

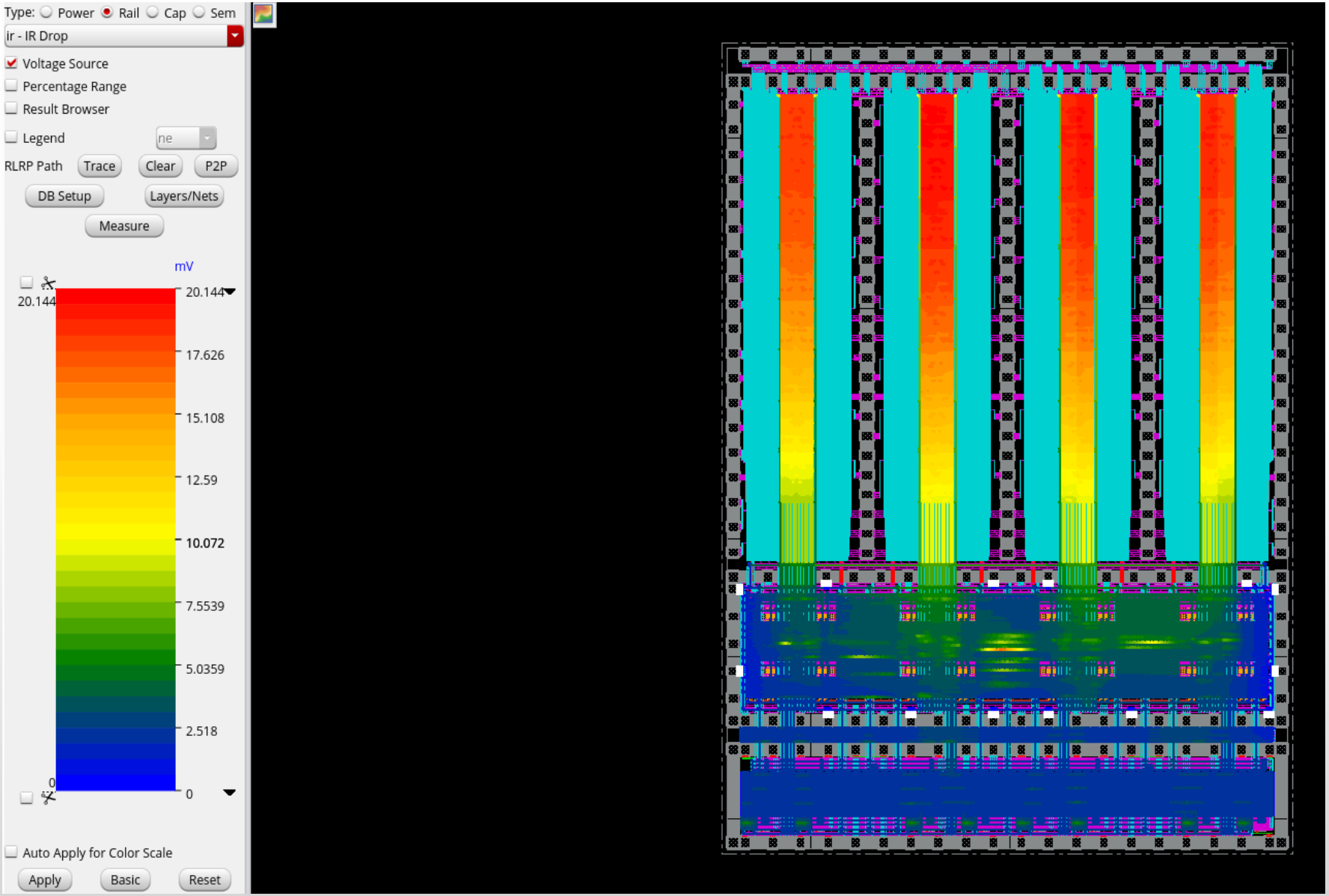
Instance power



DVDD IR drop


Type: Power Rail Cap Sem
ir - IR Drop
Voltage Source
Percentage Range
Result Browser
Legend
ne
RLRP Path
Trace
Clear
P2P
DB Setup
Layers/Nets
Measure
mV
19.463
19.463
17.03
14.597
12.164
9.7314
7.2985
4.8657
2.4328
0
0
Auto Apply for Color Scale
Apply
Basic
Reset

DGND drop


Type: Power Rail Cap Sem
ir - IR Drop
Voltage Source
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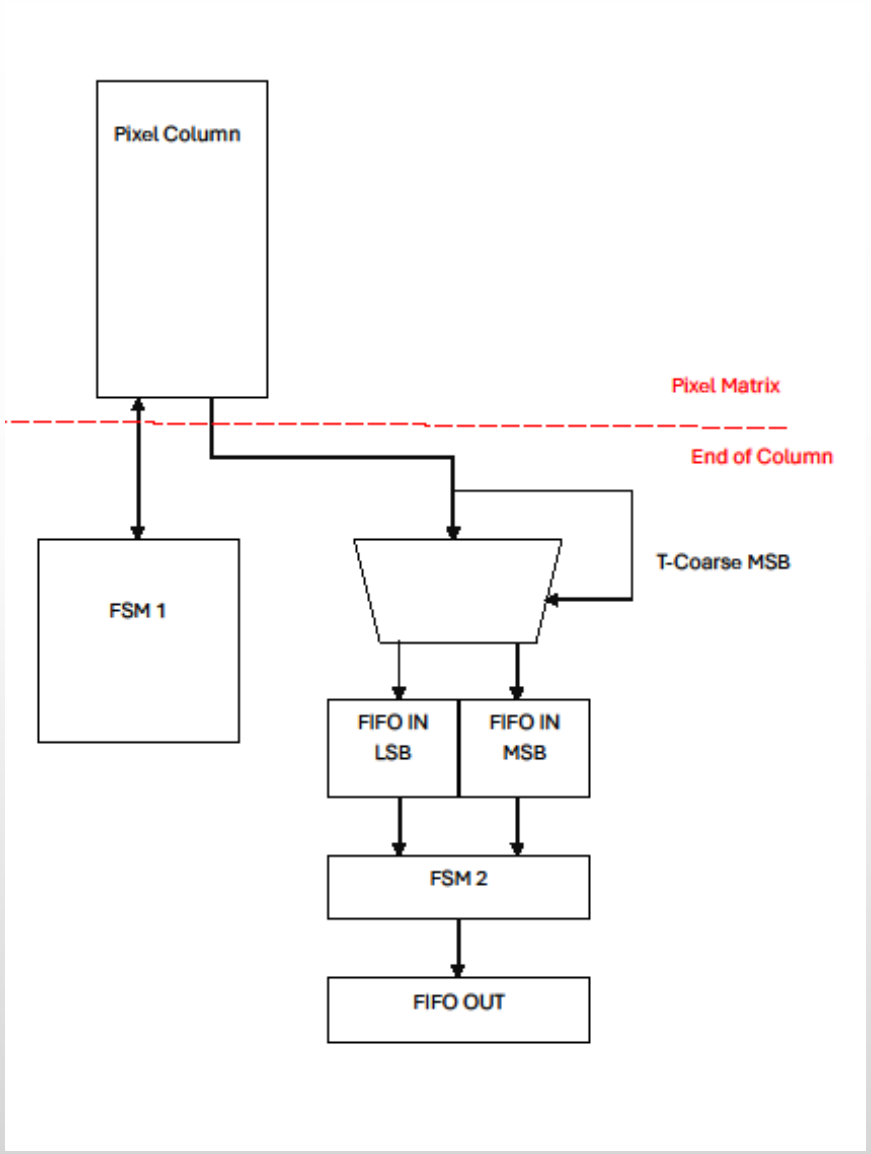
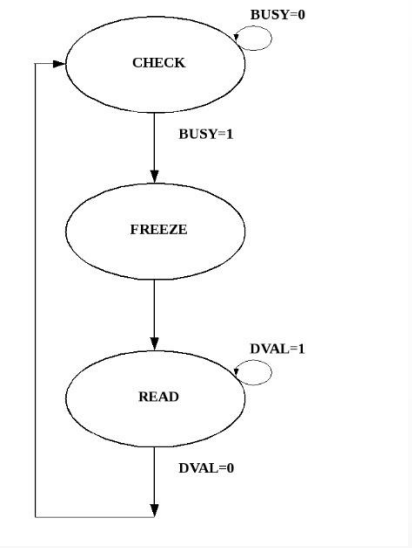
P2P
DB Setup
Layers/Nets
Measure
mV
20.144
20.144
17.626
15.108
12.59
10.072
7.5539
5.0359
2.518
0
0
Auto Apply for Color Scale
Apply
Basic
Reset

Thank you

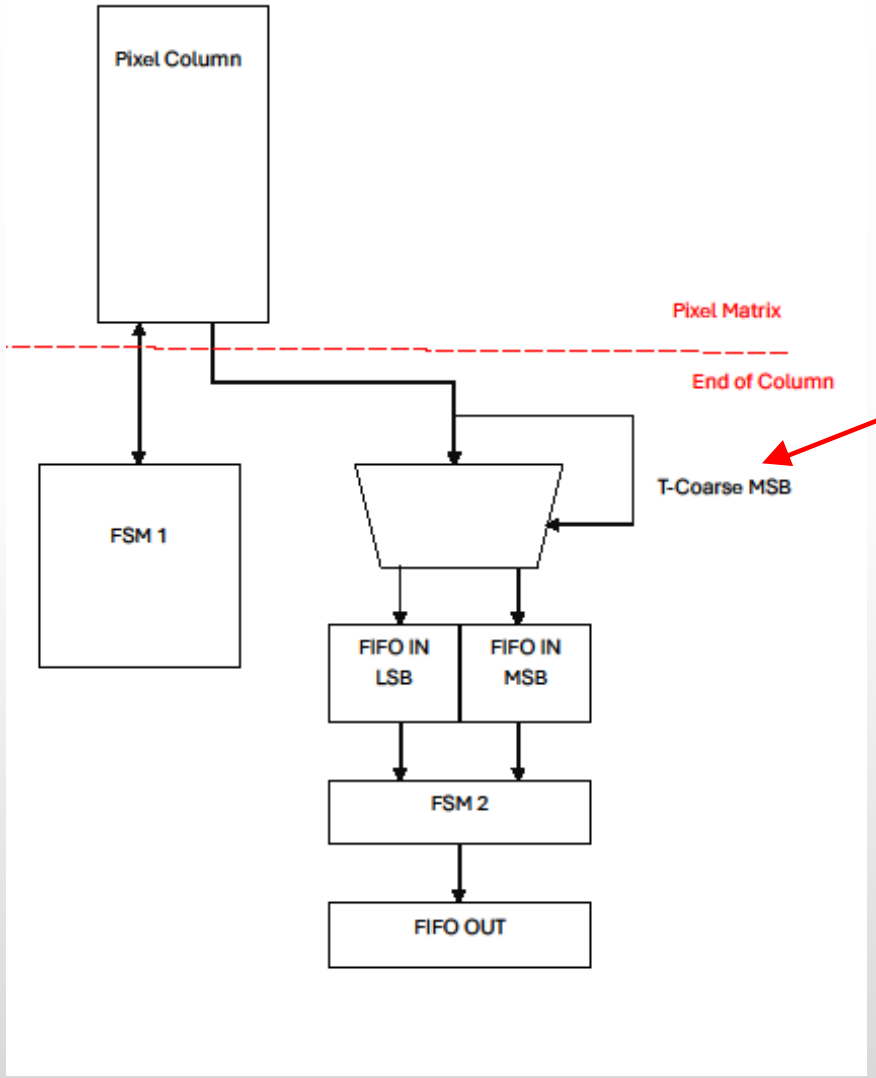
EoC readout





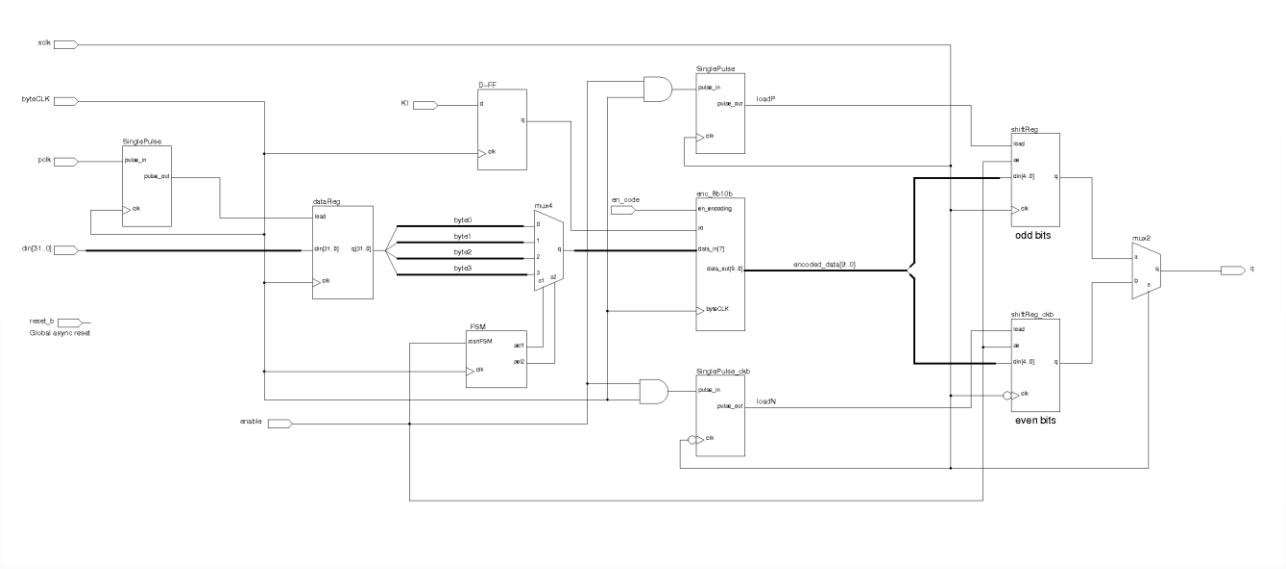
- The EoC controller has one dedicated FSM for each column and performs the scan of the column to read only pixels which have valid stored data
- When the EoC FSM1 detects the Busy condition it changes to the Freeze state
- The Freeze signal enables the Data Valid flag (DVAL) in every pixel, taking a snapshot of the pixel occupancy in this moment.
- EoC state machine initiates the readout where only pixels having stored data take the ownership of the bus, pushing data to the EoC from top to bottom
- Each pixel reset its DVAL flag at the end of Read operation
- EoC state machine leaves the Read state only when the DVAL signal, propagated through the column, is released
- A second FSM writes encoded data to the output FIFO connected to the DDR serializer

Start - New Orbit - Rollover



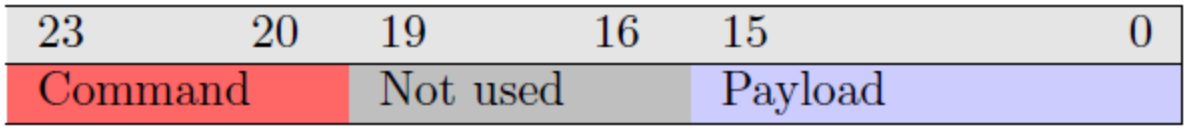
- After configuration:
  - Start Frame counter
  - Start FSMs
  - Write Header 0x1C1C1C1C
  - Write Frame Number
- To separate Frames the logic adds an extra MSB here and this is forced by Rollover, Start or New Orbit request
- Read LSB FIFO until rollover or Start or New Orbit (MSB Coarse + 1 = 1) and FIFO LSB not Empty
- Wait for timeout (9-bit counter at clk/2)
- Read MSB FIFO until rollover or Start or New Orbit (MSB Coarse + 1 = 1) and FIFO MSB not Empty
- Wait for timeout
- Each time writes Rollover code, Status words (if enabled) CRC and Trailer
- FIFO IN: 64+64 x 32
- FIFO OUT: 128x33 (one extra bit for K-code)

DDR output register



- The use of one DDR (Double Data Rate) serializer per column and the clock frequency of 394 MHz, guarantees a maximum throughput of 788 Mb/s per column
- To achieve a DC-balanced output, data are encoded following the 8b/10b protocol (effective bandwidth 630 Mb/s after decoding)
- The input stage of the serializer consists of the 32-bit data register
- The Finite State Machine (FSM), performs the byte selection, from byte 0 to 3, to send to the 8b/10b encoder
- Encoded data are split in even/odd bit position and sent to the shift registers
- Parallel to serial conversion is performed by two different shift registers, one for even bits (triggered by the falling edge of the clock) and the other one for odd bits (triggered by the rising edge of the clock)
- The two serial data streams are multiplexed to the DDR output and the selection is done by the clock signal itself

SPI Interface



Value	Action
(RW)000	Read/Write Pointer Register
(RW)001	Read/Write Data Register addressed by the Pointer
(RW)010	Read/Write SPI Status Register
0110	EoC Rad Error Register Reset
1110	EoC Rad Error Register Read
0111	EoC Status Register Reset
1111	EoC Status Register Read

- SPI serial clock frequency can be set up to 20 MHz
- SPI words are composed by 4-bit commands followed by 4 unused bit and 16-bit payload. Bit 16 to 19 have been inserted to give time to the receiver to decode the 4 command bits
- Most significant bit indicates the read/write operation
- Five registers have a direct access from the SPI interface and read/write operations are performed by one transaction only: Pointer, Data, Status and RAD error registers
- Other registers should be addressed by the Pointer Register, so that a read/write operation requires two transactions: the first one to set the Pointer and the second one to read or write the Data Register
- To reduce the number of transactions required for the whole ASIC configuration, the SPI interface implements the auto increment address mode for both write and read operations. Bit 15 of the Pointer Register is reserved for this purpose and when it set to 1 the Pointer value increments every SPI data transmission
- 272 configuration registers and 3 status registers